Title	***Reference Design Report for a 150 W Power Factor Corrected LLC Power Supply Using HiperPFS™-4 PFS7625H and HiperLCS™ LCS702HG***
Specification	100 VAC – 300 VAC Input; 39 V – 54 V at 0 – 2.75 A Output (Constant Current)
Application	LED Streetlight
Author	Applications Engineering Department
Document Number	RDR-648
Date	September 2, 2020
Revision	1.4

Summary and Features

- Integrated PFC and LLC stages for a very low component count design
- Continuous mode PFC using low cost ferrite core
- High frequency (120 kHz) LLC for small transformer size.
- >94% full load PFC efficiency at 115 VAC
- >94% full load LLC efficiency
  - System efficiency 89% / 92% at 115 VAC / 230 VAC
- Start-up circuit eliminates the need for a separate bias supply
- On-board current regulation, PWM dimming, and LLC inhibit

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Important Notes:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. All testing should be performed using an isolation transformer to provide the AC input to the prototype board.
Since there is no separate bias converter in this design, ~280 VDC is present on bulk capacitor C19 immediately after the supply is powered down. For safety, this capacitor must be discharged with an appropriate resistor (10 k / 2 W is adequate), or the supply must be allowed to stand ~10 minutes before handling.

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1 Introduction

This engineering report describes a 39 V to 54 V, 150 W reference design for a power supply for 100 VAC to 300 VAC LED street lights and other high power lighting applications. The power supply is designed with a constant current output in order to directly drive a 150 W LED panel at 46 V (nominal, 39 V min, 54 V max).

The design is based on the PFS7625H for the PFC front end with a Qspeed LXA03T600 output diode and a LCS702HG for the LLC output stage.

Figure 1 – Top View.

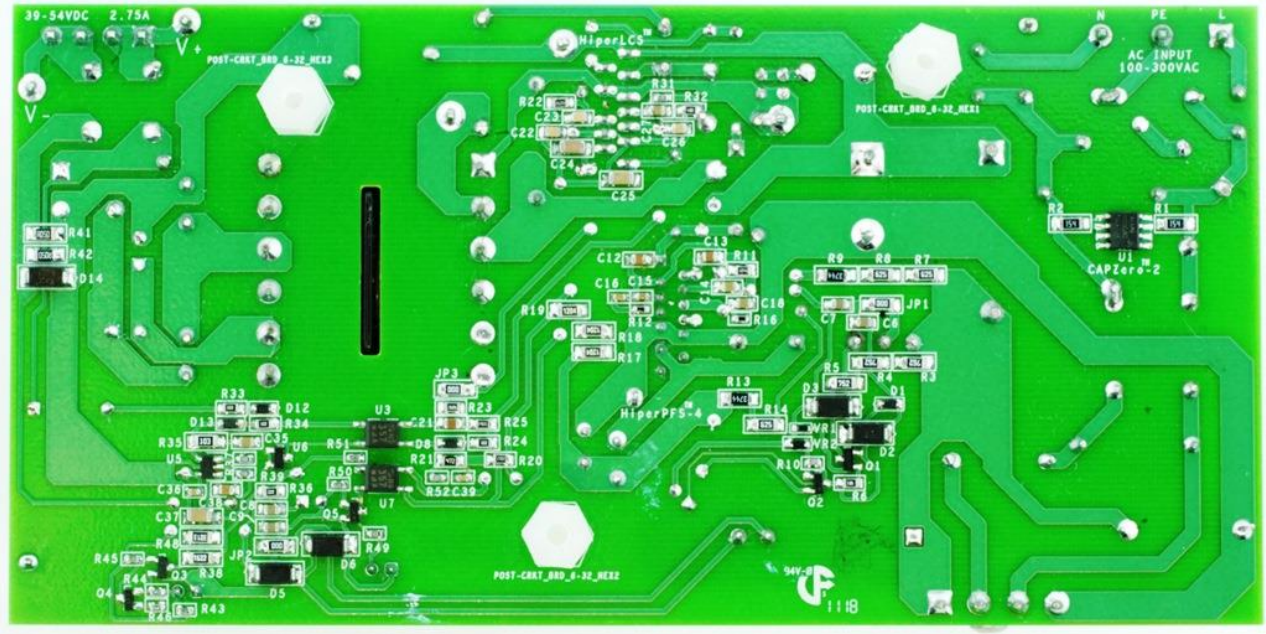

Figure 2 – Bottom View.

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2 Power Supply Specification

The table below represents the minimum acceptable performance for the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	$\mathbf{V_{IN}}$	100		300	VAC	3 Wire Input.
Frequency	$\mathbf{f_{LINE}}$	47	50/60	64	Hz	
Power Factor	**PF**	0.9				Full Load, 277 VAC.
Main Converter Output						
Output Voltage	$\mathbf{V_{LG}}$	39	46	54	V	46 VDC Nominal – test with LED Load or LED emulator (see sections 7 & 8) Output voltage defined by LED load – protected against no load.
Output Ripple	$\mathbf{V_{RIPPLE(LG)}}$			300	mV_{PK-PK}	20 MHz Bandwidth
Output Current	$\mathbf{I_{LG}}$	0.00	2.75		A	Constant Current Supply Protected for No-load Condition.
Total Output Power						
Continuous Output Power	$\mathbf{P_{OUT}}$		150		W	
Peak Output Power	$\mathbf{P_{OUT(PK)}}$			N/A	W	
No-Load Input Power				<0.5	W	Tested with LLC inhibited via inhibit input
Efficiency						
Total system at Full Load	η_{Main}		89.5 92		%	Measured at 115 VAC, Full Load. Measured at 230 VAC, Full Load.
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Safety		Designed to meet IEC950 / UL1950 Class II				
Surge						1.2/50 μs Surge, IEC 1000-4-5,
Differential		4			kV	Differential Mode: 2 Ω.
Common Mode		4			kV	Common Mode: 12 Ω.
Ambient Temperature	$\mathbf{T_{AMB}}$	0		60	°C	See Thermal Section for Conditions.

3 Schematic

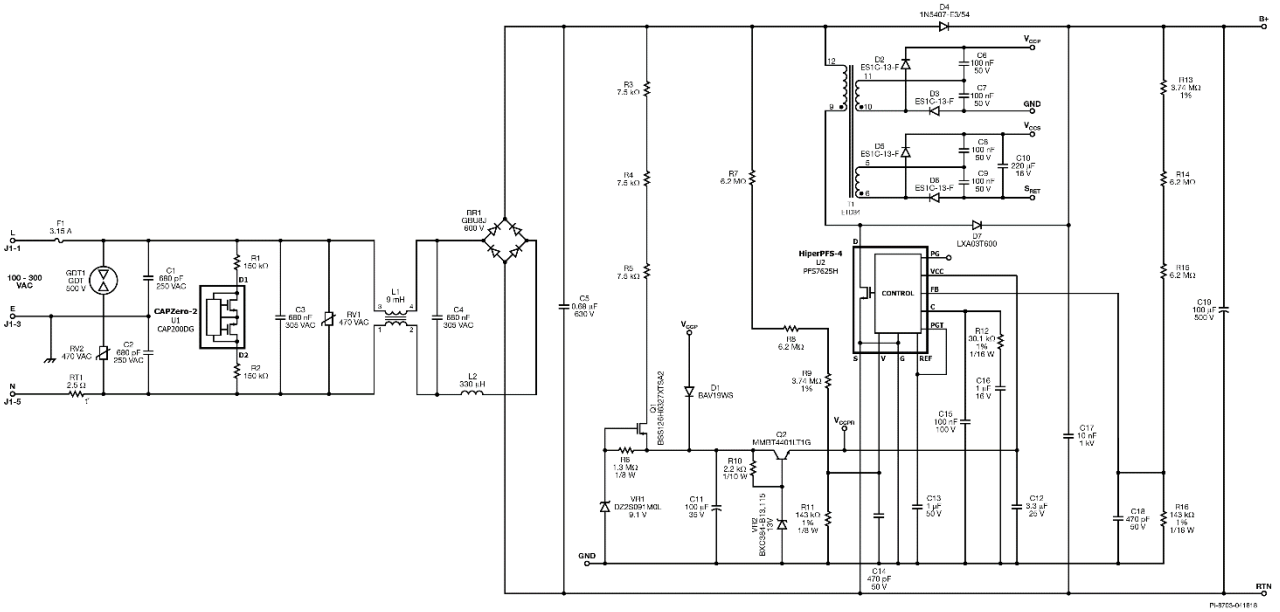

Figure 3 – Schematic - Input Filter, PFC Power Stage, and Bias Supplies.

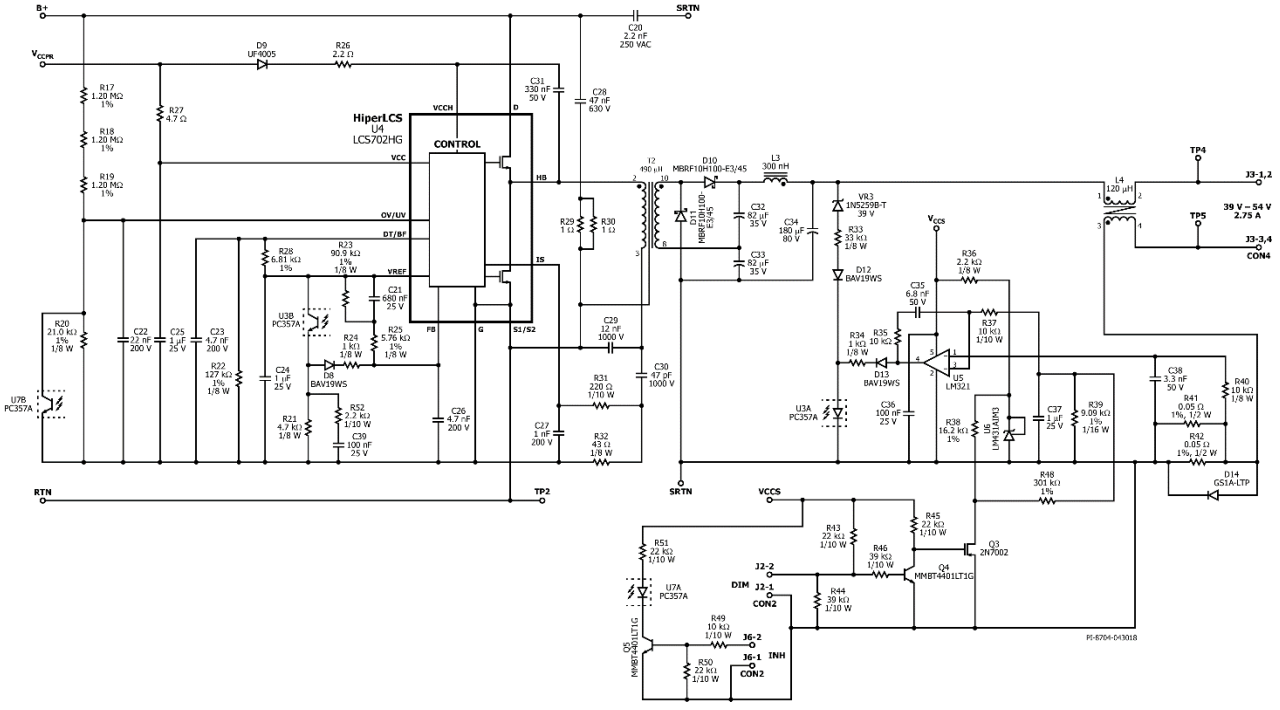

Figure 4 – Schematic - LLC Stage.

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4 Circuit Description

4.1 *Input Filter / Boost Converter / Bias Supply*

The schematic in Figure 3 shows the input EMI filter, PFC stage, and primary bias supply/startup circuit. The power factor corrector utilizes the PFS7625H. The primary and secondary bias supplies are derived from windings on the PFC inductor (T1).

4.2 *EMI Filtering / Inrush Limiting*

Capacitors C1 and C2 are used to control common mode noise, while C3-4 and L2 control differential mode EMI. Fuse F1 protects in case of a primary side fault/failure. Resistors R1-2 and U1 discharge C3-4 when AC power is removed. Inductor L1 controls common mode EMI. The heat sink for U2, U4, D7, and BR1 is connected to primary return to eliminate the heat sink as a source of radiated/capacitively coupled noise. Thermistor RT1 limits inrush current at startup. Capacitor C20 (Figure 4) filters common mode EMI. Inductor L4 (Figure 4) filters common-mode noise at the supply output and prevents an EMI peak at ~15 MHz. Varistors RV1 and RV2, with gas tube GDT1, protect against differential mode line surge.

4.3 *Main PFC Stage*

Components R13-16 (filtered by C18) provide output voltage feedback to U2. PFC output voltage is set at 440 VDC (nom). Components R12 and C15-16 are for frequency compensation. Resistors R7-9 and R11 (filtered by C14) convey input voltage information to U2. Capacitor C13 bypasses the U2 voltage reference pin. This capacitor is sized at 1uF to select "FULL" operating mode for U2. The PGT pin of U2 is tied to the REF pin in order to disable the internal power good function, which is not used in this application.

Capacitor C12 provides local bypassing for the U2 Vcc supply. Diode D4 charges the PFC output capacitor (C19) when AC is first applied, routing the inrush current away from PFC inductor T1 and output diode D7. Capacitor C17 is used to reduce the area of the high frequency loop around components U2 and C19, reducing EMI and U2 peak drain voltage. The incoming AC is rectified by BR1 and filtered by C5. Capacitor C5 is a low-loss polypropylene type to accommodate the high instantaneous current through T1 during U2 on-time.

4.4 *Primary Bias Supply / Start-up*

Components R3-6, Q1, and VR1 provide startup bias for U2. Once U2 starts, components D2, D3, C6-7 and C11 generate a primary-referred bias supply via a winding on PFC choke T1. This is used to power both the PFC and LLC stages of the power supply via D1. The bias supply is set up as a voltage doubler, so that the bias voltage tracks the regulated B+ output from the PFC. Auxiliary winding turns can be calculated from the equation:

$$Nb = Np\ X\ (\frac{Vbias + 2Vd}{VB+})$$

N_b is the number of bias turns, N_p is the number of turns on the main winding of the PFC choke, V_{B+} is the PFC output voltage, and V_d is the voltage drop of the bias rectifiers. N_b should be rounded up to the nearest whole number in the case of a fractional solution.

Once the primary bias supply voltage is established, it is used to turn off MOSFET Q1 via diode VR1, reducing power consumption. Resistors R3-5 protect Q1 from excessive power dissipation if the power supply fails to start.

Components R10, VR2, and Q2 regulate the bias supply voltage for U2 and U4. Components D5-6 and C8-10 generate a bias supply for the secondary control circuitry via a triple insulated winding on T2 and a voltage doubler circuit.

4.5 *LLC Converter*

The schematic in Figure 4 depicts a 39-54 V, 150 W LLC DC-DC converter with constant current output implemented using the LCS702HG.

4.6 *Primary*

Integrated circuit U4 incorporates the control circuitry, drivers and output MOSFETs necessary for an LLC resonant half-bridge (HB) converter. The HB output of U4 drives output transformer T1 via a blocking/resonating capacitor (C29). This capacitor is a polypropylene film type rated for the operating ripple current and to withstand the high voltages present during fault conditions.

Transformer T2 was designed for a leakage inductance of 124 μH. This, along with resonating capacitor C29, sets the primary series resonant frequency at ~120 kHz according to the equation:

$$f_R = \frac{1}{6.28\sqrt{L_L \times C_R}}$$

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Where f_R is the series resonant frequency in Hertz, L_L is the transformer leakage inductance in Henries, and C_R is the value of the resonating capacitor (C29) in Farads.

The transformer turns ratio was set by adjusting the primary turns such that the operating frequency at nominal output voltage (46V) and full load is close to, but slightly less than, the previously described resonant frequency. The operating frequency will move up or down to accommodate LED panels that have voltage drops different than the nominal case.

An operating frequency of 120 kHz for the 46 V nominal output voltage was found to be a good compromise between transformer size, output filter capacitance, and efficiency.

The number of secondary winding turns and wire size were chosen to provide a good compromise between core and copper losses. AWG #42 Litz wire was used for the primary and AWG #40 Litz wire for the secondary. This combination provides high efficiency at the operating frequency (~120 kHz). The number of strands within each gauge of Litz wire was chosen in order to achieve a balance between winding fit and copper losses.

Ferroxcube 3C97 was selected as the T2 core material for its low loss.

Components D9, R26, and C31 comprise the bootstrap circuit to supply the internal high-side driver of U4.

Components R27 and C25 provide filtering and bypassing of the V_{CC} supply for U4. *Note: V_{CC} voltage of >15 V may damage U4.* Capacitor C24 provides filtering and bypass for the U4 Vref pin.

Voltage divider resistors R17-20 set the high-voltage turn-on, turn-off, and overvoltage thresholds of U4. The voltage divider values are chosen to set the LLC turn-on point at 416 VDC and the turn-off point at 330 VDC, with an input overvoltage turn-off point at 548 VDC. Built-in hysteresis sets the input undervoltage turn-off point at 330 VDC. Capacitor C22 filters the signal for the OV/UV pin.

Capacitor C28 is a high-frequency bypass capacitor for the +440 V input, connected with short traces between the D and S1/S2 pins of U4. Series resistors R29-30 damp EMI.

Capacitor C30 forms a current divider with C29, and is used to sample a portion of the T2 primary current. Resistor R32 senses this sampled current, and the resulting signal is filtered by R31 and C27. Capacitor C30 should be rated for the peak voltage present during fault conditions, and should use a stable, low-loss dielectric such as metalized film, SL ceramic, or NPO/COG ceramic. The capacitor used for C30 is a ceramic disc with NPO/COG temperature characteristic. The value chosen for R32 sets the one-cycle (fast)

current limit at 5.4 A, and the seven-cycle (slow) current limit at 3.0 A, according to the equation:

$$I_{CL} = \frac{0.5}{\left(\frac{C30}{C29 + C30}\right) \times R32}$$

I_{CL} is the seven-cycle current limit in amperes, R32 is the current limit resistor in ohms, and C29 and C30 are the values of the resonating and current sampling capacitors in nanofarads, respectively. For the one-cycle current limit, substitute 0.9 V for 0.5 V in the above equation.

Resistor R31 and capacitor C27 filter the primary current signal to the IS pin. Resistor R31 is set to 220 Ω, the minimum recommended value. The value of C27 is set to 1 nF to avoid nuisance tripping due to noise, but not so high as to substantially affect the current limit set values as calculated above. These components should be placed close to the IS pin for maximum effectiveness. The IS pin can tolerate negative currents, so the current sense does not require a complicated rectification scheme.

The Thevenin equivalent combination of R22 and R28 sets the dead time at 320 ns and maximum operating frequency for U4 at 847 kHz. The DT/BF input of U4 is filtered by C23. The combination of R22 and R28 also selects burst mode "1" for U4. This sets the lower and upper burst threshold frequencies at 382 kHz and 437 kHz, respectively.

The FEEDBACK pin has an approximate characteristic of 2.6 kHz per μA into the FEEDBACK pin. As the current into the FEEDBACK pin increases so does the operating frequency of U4, reducing the output voltage. The series combination of R23 and R25 sets the minimum operating frequency for U4 at ~94 kHz. This value was set to be slightly lower than the frequency required for regulation at full load and minimum bulk capacitor voltage. Resistor R23 is bypassed by C21 to provide output soft start during start-up by initially allowing a higher current to flow into the FEEDBACK pin when the feedback loop is open. This causes the switching frequency to start high and then decrease until the output voltage reaches regulation. Resistor R28 is typically set at the same value as the parallel combination of R23 and R25 so that the initial frequency at soft-start is equal to the maximum switching frequency as set by R23 and R25. If the value of R28 is less than this, it will cause a delay before switching occurs when the input voltage is applied.

Optocoupler U3 drives the U4 FEEDBACK pin through R24, which limits the maximum optocoupler current into the FEEDBACK pin. Capacitor C26 filters the FEEDBACK pin. Resistor R21 loads the optocoupler output to force it to run at a relatively high quiescent current, increasing its gain. Resistor R21 also improves large signal step response and burst mode output ripple. Diode D8 isolates R24 from the F_{MAX}/soft start network.

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4.7 *Output Rectification*

The output of transformer T2 is rectified and filtered by D10-11 and C32-33, arranged as a voltage doubler. For C32-33, aluminum polymer capacitors were used for small size, long life, and high ripple current rating. Output rectifiers D10-11 are 100 V Schottky rectifiers chosen for high efficiency.

The output rectifier and filter were arranged as a voltage doubler to enable use of a single secondary winding rather than a center tapped winding. This eliminates the need to twist secondary windings together to balance the currents between the phases. It also eliminates the manufacturing variability (especially variable stray capacitance) introduced by the twisted wires. The voltage doubler allows use of lower voltage devices for both D10-11 and C32-33. The downside of this approach is higher peak current in the transformer secondary, with a small reduction of efficiency.

Additional output filtering is provided by L3 and C34. Capacitor C34 also damps the LLC output impedance peak at ~30 kHz caused by the LLC "virtual" output series R-L and output capacitors C32-33.

4.8 *Output Current and Voltage Control*

Output current is sensed via resistors R41-42. These resistors are clamped by diode D14 to avoid damage to the current control circuitry during an output short circuit. Components R36 and U6 provide a voltage reference for current sense amplifier U5. The reference voltage is divided down by R38-39 and R48, and filtered by C37. Voltage from the current sense resistor is filtered by R40 and C38 and applied to the non-inverting input of U5. Opamp U5 drives optocoupler U3 via D13 and R34. Components R35, R37, R40, R52, C35, and C38 are used for frequency compensation of the current loop. Components VR3 and R33 provide output voltage regulation to protect the power supply in case the output load is removed. These components were selected using a relatively large value for R33 and a relatively low voltage for VR3 to provide a soft voltage limiting characteristic. This helps prevent oscillation at the knee of the V-I characteristic curve and improves the start-up characteristics of the supply into the specified LED load. Diode D12 prevents reverse current through VR3 when the output voltage is less than the VR3 zener voltage. Components J2, Q3-4, R43-46, and C37 are used to provide a remote dimming capability via a PWM input signal. The PWM signal is used to modify the reference voltage for the current sense amplifier to program an output current limit linearly dependent on the PWM signal duty cycle.

With no signal present at J2, Q4 is biased on by resistor network R43-44 and R46. This removes drive from MOSFET Q3 and allows maximum output current (100% output with no dimming signal). A dimming signal with 0% duty cycle (essentially grounding the dimming input) will turn off Q4, turning on Q3 and pulling down the reference voltage that programs the output current via current sense amplifier U5. Higher duty factors charge and discharge capacitor C37 via resistors R38-39 and R48, generating a variable

current limit reference voltage with a small ripple component. This scheme allows adjustment from near zero output current to 100%, or to default to 100% output with no dimming signal present. Voltage divider R43-44 biases Q4 on when there is no dimming signal connected, so that the default is 100% output. This divider also limits the voltage present at the dimming input to accommodate low voltage logic.

Components J6, R49-51, Q5, and U7 comprise a remote inhibit circuit for the LLC stage, which can be used to turn off the output while still allowing the PFC stage to run and provide bias voltage for supervisory functions. The circuit inhibits U4 by shorting the bottom resistor R20 in the LLC UV/OV voltage divider network.

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5 PCB Layout

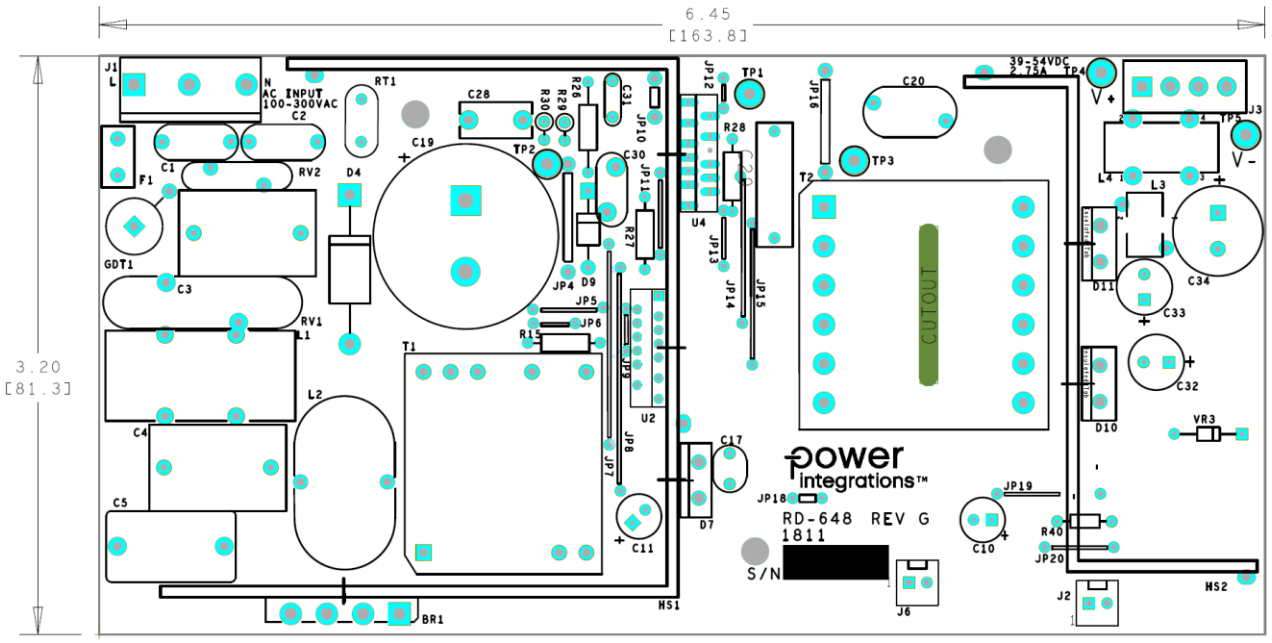

Figure 5 – Printed Circuit Layout, Top Side.

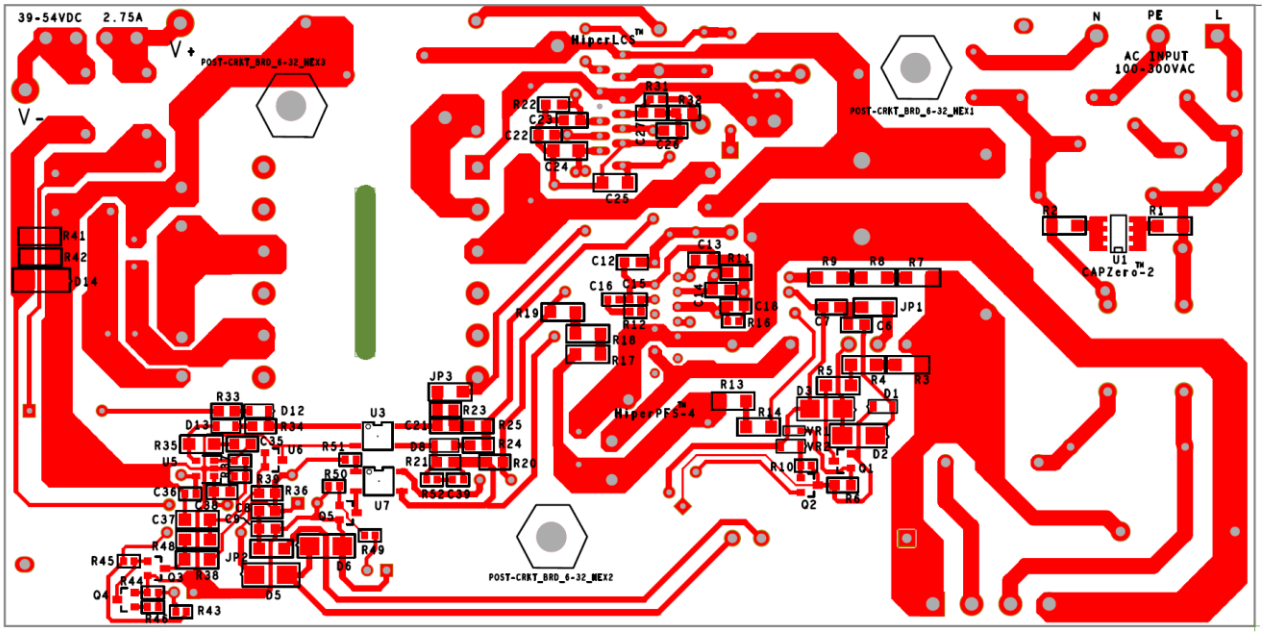

Figure 6 – Printed Circuit Layout, Bottom Side.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	600 V, 8 A, Bridge Rectifier, GBU Case	GBU8J-BP	Micro Commercial
2	2	C1 C2	680 pF, Ceramic, Y1	440LT68-R	Vishay
3	2	C3 C4	680 nF, ±20%,305 VAC, Polypropylene (PP)Film, X2	B32922C3684M000	TDK
4	1	C5	FILM, 0.68 µF, 5%, 630VDC, RAD	ECW-FA2J684J	Panasonic
5	4	C6 C7 C8 C9	100 nF, 50 V, Ceramic, X7R, 0805	CC0805KRX7R9BB104	Yageo
6	1	C10	220 µF, 16 V, Electrolytic, Low ESR, 180 mΩ, (6.3 x 15)	ELXZ160ELL221MF15D	Nippon Chemi-Con
7	1	C11	100 µF, 35 V, Electrolytic, Low ESR, 180 mΩ, (6.3 x 15)	ELXZ350ELL101MF15D	Nippon Chemi-Con
8	1	C12	3.3 µF, 25 V, Ceramic, X7R, 0805	C2012X7R1E335K	TDK
9	1	C13	1 µF,50 V, Ceramic, X7R, 0805	C2012X7R1H105M085AC CGA4J3X7R1H105M125AE	TDK TDK
10	2	C14 C18	470 pF, 50 V, Ceramic, X7R, 0805	CC0805KRX7R9BB471	Yageo
11	1	C15	100 nF 100 V, Ceramic, X7R, 0603	GRM188R72A104KA35D	Murata
12	1	C16	1 µF, 16 V, Ceramic, X5R, 0603	GRM188R61C105KA93D	Murata
13	1	C17	10 nF, 1 kV, Disc Ceramic, X7R	SV01AC103KAR	AVX
14	1	C19	100 µF, ±20%, 500 V, Electrolytic , 3000 Hrs @ 105 °C, Radial, Can - Snap-In	LGN2H101MELA30	Nichicon
15	1	C20	2.2 nF, Ceramic, Y1	440LD22-R	Vishay
16	1	C21	680 nF,25 V, Ceramic, X7R, 0805	GRM219R71E684KA88D	Murata
17	1	C22	22 nF, 200 V, Ceramic, X7R, 0805	08052C223KAT2A	AVX
18	2	C23 C26	4.7 nF, 200 V, Ceramic, X7R, 0805	08052C472KAT2A	AVX
19	3	C24 C25 C37	1 µF, 25 V, Ceramic, X7R, 1206	C3216X7R1E105K	TDK
20	1	C27	1 nF, 200 V, Ceramic, X7R, 0805	08052C102KAT2A	AVX
21	1	C28	47 nF, 630 V, Film	MEXPD24704JJ	Duratech
22	1	C29	12 nF,1000 VDC, Film	BFC238330123	Vishay
23	1	C30	47 pF, 1000 V, Disc Ceramic	561R10TCCQ47	Vishay
24	1	C31	330 nF, 50 V, Ceramic, X7R	FK24X7R1H334K	TDK
25	2	C32 C33	82 µF, 35 V, l Organic Polymer, Gen. Purpose, (8 x 12)	35SEPF82M+TSS	Panasonic
26	1	C34	180 µF, 80 V, Electrolytic, 90 mΩ, (12.5 x 17.5)	EKZN800ELL181MK16S	Nippon Chemi-Con
27	1	C35	6.8 nF, 50 V, Ceramic, X7R, 0805	CC0805KRX7R9BB682	Yageo
28	2	C36 C39	100 nF, 0.1µF, ±10%, 25V, Ceramic Capacitor, X7R, General Purpose, -55°C ~ 125°C, 0603	CL10B104KA8NFNC	Samsung
29	1	C38	3.3 nF, 50 V, Ceramic, X7R, 0805	CC0805KRX7R9BB332	Yageo
30	4	D1 D8 D12 D13	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diodes, Inc.
31	4	D2 D3 D5 D6	150 V, 1 A, Ultrafast Recovery, 25 ns, DO-214AC	ES1C-13-F	Diodes, Inc.
32	1	D4	800 V, 3 A, Recitifier, DO-201AD	1N5407-E3/54	Vishay
33	1	D7	600 V, 3 A, TO-220AC	LXA03T600	Power Integrations
34	1	D9	600 V, 1 A, Ultrafast Recovery, 75 ns, DO-41	UF4005-E3	Vishay
35	2	D10 D11	100 V, 10 A, Schottky, ITO-220FPAC	MBRF10H100-E3/45	Vishay
36	1	D14	50 V, 1 A, DO-214AC	GS1A-LTP	Micro Commercial
37	2	ESIPCLIP M4 METAL1 ESIPCLIP M4 METAL2	Heat Sink Hardware, Edge Clip, 20.76 mm L x 8 mm W x 0.015 mm Thk	NP975864	Aavid Thermalloy
38	1	F1	3.15 A, 300 V, Slow, Long Time Lag, RST	36913150000	Littlefuse
39	1	GDT1	Gas Discharge Tube, 500 V, 10 kA, ±20%, 2 Pole, Through Hole	B88069X4860T502	TDK
40	1	GREASE1	Thermal Grease, Silicone, 5 oz Tube	CT40-5	ITW Chemtronics

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41	1	HEATSHRINK1	HEAT SHRINK 3/8 IN X 4FT Clear	F221B3/8 CL100	Alpha Wire
42	1	HS PAD3	HEAT SINK PAD, TO-220, Sil-Pad K10	K10-58	Bergquist
43	1	HS1	FAB, HEAT SINK, DER648, Primary		Custom
44	1	HS2	FAB, HEAT SINK, DER648, Secondary		Custom
45	1	J1	Header, 5 Position (1 x 5), 0.156 pitch, Vertical, friction lock	0026481055	Molex
46	2	J2 J6	2 Position (1 x 2) header, 0.1 pitch, Vertical	22-23-2021	Molex
47	1	J3	4 Position (1 x 4) header, 0.156 pitch, Vertical	26-48-1045	Molex
48	3	JP1 JP2 JP3	RES, 0 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEY0R00V	Panasonic
49	2	JP4 JP16	Wire Jumper, Insulated, TFE, #18 AWG, 0.6 in	C2052A-12-02	Alpha
50	1	JP5	Wire Jumper, Insulated, #28 AWG, 0.4 in	2842/1 WH005	Alpha Wire
51	4	JP6 JP9 JP13 JP19	Wire Jumper, Insulated, #28 AWG, 0.3 in	2842/1 WH005	Alpha Wire
52	1	JP7	Wire Jumper, Insulated, #28 AWG, 1.0 in	2842/1 WH005	Alpha Wire
53	1	JP8	Wire Jumper, Insulated, #28 AWG, 1.2 in	2842/1 WH005	Alpha Wire
54	1	JP10	Wire Jumper, Insulated, TFE, #18 AWG, 0.3 in	C2052A-12-02	Alpha Wire
55	2	JP11 JP18	Wire Jumper, Insulated, #28 AWG, 0.6 in	2842/1 WH005	Alpha Wire
56	1	JP12	Wire Jumper, Insulated, #28 AWG, 0.2 in	2842/1 WH005	Alpha Wire
57	1	JP14	Wire Jumper, Insulated, #28 AWG, 0.9 in	2842/1 WH005	Alpha Wire
58	1	JP15	Wire Jumper, Insulated, #28 AWG, 0.8 in	2842/1 WH005	Alpha Wire
59	1	JP20	Wire Jumper, Insulated, #28 AWG, 0.7 in	2842/1 WH005	Alpha Wire
60	1	L1	9 mH, 5 A, Common Mode Choke	T22148-902S P.I. Custom	Fontaine
61	1	L2	330 µH, 3.3 A, Vertical Toroidal	2218-V-RC	Bourns
62	1	L3	300 nH, ±15%,Toroidal Choke, OUTPUT, custom, DER-648	32-00363-00	Power Integrations
63	1	L4	120 µH, ±15%,Toroidal Common Mode Choke, custom, DER-648	32-00362-00	Power Integrations
64	3	POST-CRKT_BRD_6-32_HEX?	Post, Circuit Board, Female, Hex, 6-32, snap, 0.50"L, Nylon	561-0500A	Eagle Hardware
65	1	Q1	MOSFET, N-CH, 600 V, 0.021 A (Ta),1.3W (Ta) , TO-236-3, SC-59, SOT-23-3	BSS126H6327XTSA2	Infineon
66	3	Q2 Q4 Q5	NPN, Small Signal BJT, GP SS, 40 V, 0.6 A, SOT-23	MMBT4401LT1G MMBT4401LT3G	Diodes, Inc. On Semi
67	1	Q3	60V, 115MA, SOT23-3	2N7002-7-F	Diodes, Inc.
68	2	R1 R2	RES, 150 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ154V	Panasonic
69	3	R3 R4 R5	RES, 7.5 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ752V	Panasonic
70	1	R6	RES, 1.3 MΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ135V	Panasonic
71	3	R7 R8 R14	RES, 6.2 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ625V	Panasonic
72	2	R9 R13	RES, 3.74 MΩ, 1%, 1/4 W, Thick Film, 1206	CRCW12063M74FKEA	Vishay
73	2	R10 R52	RES, 2.2 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ222V	Panasonic
74	1	R11	RES, 143 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1433V	Panasonic
75	1	R12	RES, 30.1 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF3012V	Panasonic
76	1	R15	RES, 6.2 MΩ, 5%, 1/4 W, Carbon Film	CFR-25JB-6M2	Yageo
77	1	R16	RES, 143 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1433V	Panasonic
78	3	R17 R18 R19	RES, 1.20 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1204V	Panasonic
79	1	R20	RES, 21 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF2102V	Panasonic
80	1	R21	RES, 4.7 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ472V	Panasonic
81	1	R22	RES, 127 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1273V	Panasonic
82	1	R23	RES, 90.9 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF9092V	Panasonic
83	2	R24 R34	RES, 1 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ102V	Panasonic
84	1	R25	RES, 5.76 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF5761V	Panasonic
85	1	R26	RES, 2.2 Ω, 5%, 1/4 W, Carbon Film	CFR-25JB-2R2	Yageo
86	1	R27	RES, 4.7 Ω, 5%, 1/4 W, Carbon Film	CFR-25JB-4R7	Yageo
87	1	R28	RES, 6.81 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-6K81	Yageo
88	2	R29 R30	RES, 1 Ω, 5%, 1/4 W, Carbon Film	CFR-25JB-1R0	Yageo
89	1	R31	RES, 220 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ221V	Panasonic

90	1	R32	RES, 43 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ430V	Panasonic
91	1	R33	RES, 33 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ333V	Panasonic
92	1	R35	RES, 10 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ103V	Panasonic
93	1	R36	RES, 2.2 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ222V	Panasonic
94	2	R37 R49	RES, 10 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ103V	Panasonic
95	1	R38	RES, 16.2 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1622V	Panasonic
96	1	R39	RES, 9.09 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF9091V	Panasonic
97	1	R40	RES, 10 kΩ, 5%, 1/8 W, Carbon Film	CF18JT10K0	Stackpole
98	2	R41 R42	RES, SMD, 0.05 Ω, 1%, ½ W, 1206, ±100ppm/°C, -55°C ~ 155 °C	CSR1206FT50L0	Stackpole
99	4	R43 R45 R50 R51	RES, 22 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ223V	Panasonic
100	2	R44 R46	RES, 39 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ393V	Panasonic
101	1	R48	RES, 301 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF3013V	Panasonic
102	1	RT1	NTC Thermistor, 2.5 Ω, 5 A	SL10 2R505	Ametherm
103	1	RV1	470 VAC, 10 kA, 350 J, 900 pF @ 1 kHz, -40 °C ~ 85 °C (TA), 20 mm, RADIAL	ERZ-V20D471	Panasonic
104	1	RV2	470 VAC, 125 J, 14 mm, RADIAL	V14E300P	Littlefuse
105	6	SCREW1 SCREW2 SCREW3 SCREW4 SCREW5 SCREW6	SCREW MACHINE PHIL 4-40 X 1/4 SS	PMSSS 440 0025 PH	Building Fasteners
106	1	T1	489 μH, +5%, PFC Choke, Custom for DER-648,	30-00475-00	Power Integrations
107	1	T2	490 μH, ±10%, LLC XFMR, Custom for DER-648	30-00476-00	Power Integrations
108	4	TP1 TP2 TP3 TP5	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
109	1	TP4	Test Point, RED, THRU-HOLE MOUNT	5010	Keystone
110	1	U1	CAPZero-2, SO-8C	CAP200DG	Power Integrations
111	1	U2	HiperPFS-4	PFS7625H	Power Integrations
112	2	U3 U7	Optoisolator, Transistor Output, 3750Vrms, 1 Channel, 4-Mini-Flat	PC357N1J000F	Sharp
113	1	U4	HiperLCS, ESIP16/13	LCS702HG	Power Integrations
114	1	U5	OP AMP SINGLE LOW PWR SOT23-5	LM321MF	National Semi
115	1	U6	IC, REG ZENER SHUNT ADJ SOT-23	LM431AIM3/NOPB	National Semi
116	1	VR1	9.1 V, 5%, 150 mW, SSMINI-2	DZ2S091M0L	Panasonic
117	1	VR2	13 V, 2%, 300 mW, SOD-323	BZX384-B13,115	NXP
118	1	VR3	39 V, 5%, 500 mW, DO-35	1N5259B-T	Diodes, Inc.
119	6	WASHER1 WASHER2 WASHER3 WASHER4 WASHER5 WASHER6	WASHER FLAT #4 Zinc, OD 0.219, ID 0.125, Thk 0.032,Yellow Chromate Finish	5205820-2	Tyco
120	1	WASHER7	Washer, Shoulder, #4, 0.125 Shoulder x 0.150 Dia, Polyphenylene Sulfide PPS	7721-1PPSG	Aavid Thermalloy

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7 LED Panel Characterization

A 150 W LED array was used to test the power supply. The LED array consisted of 42 pieces (3 wide, 14 deep), of LED Engin, Inc. LZ1-10CW02-0065 cool white 1 A LEDs. The array hookup is shown in Figure 6. The V-I characteristic of the LED panel is shown in Figure 7, generated using a constant-current bench supply at room temperature. The V-I characteristic shows a population of LEDs near the median value for voltage drop of 3.3 V, resulting in a 46 V drop at 2.75 A operating current.

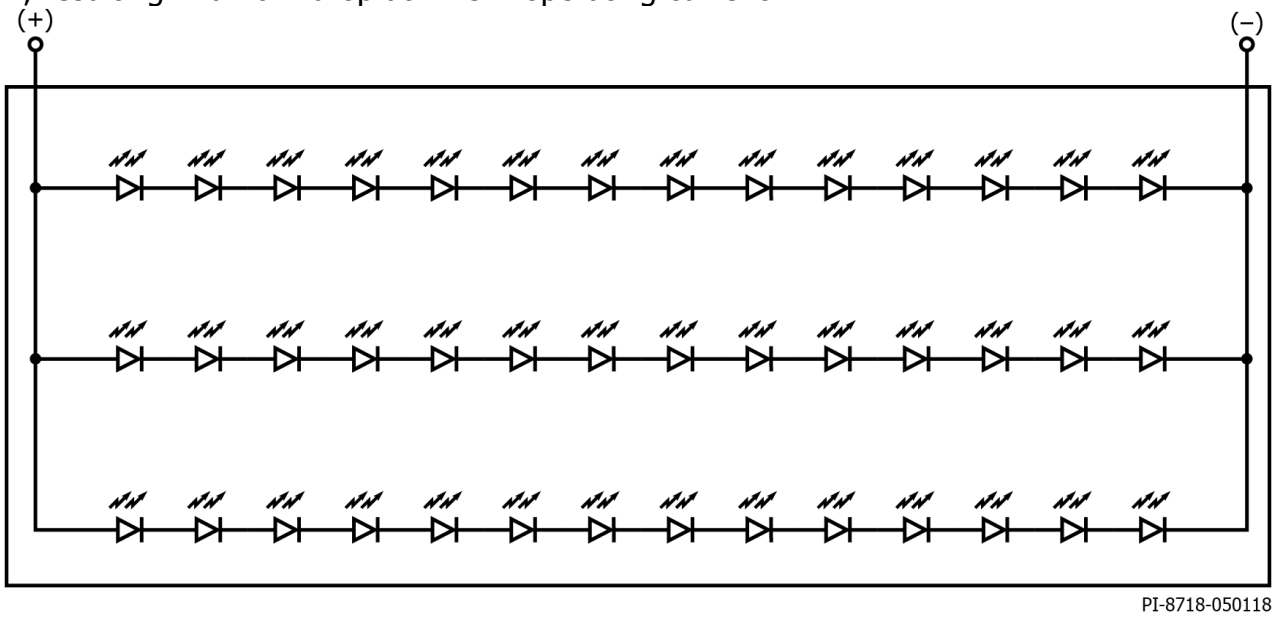

Figure 7– Experimental LED Panel (3 x 14 Array) Schematic.

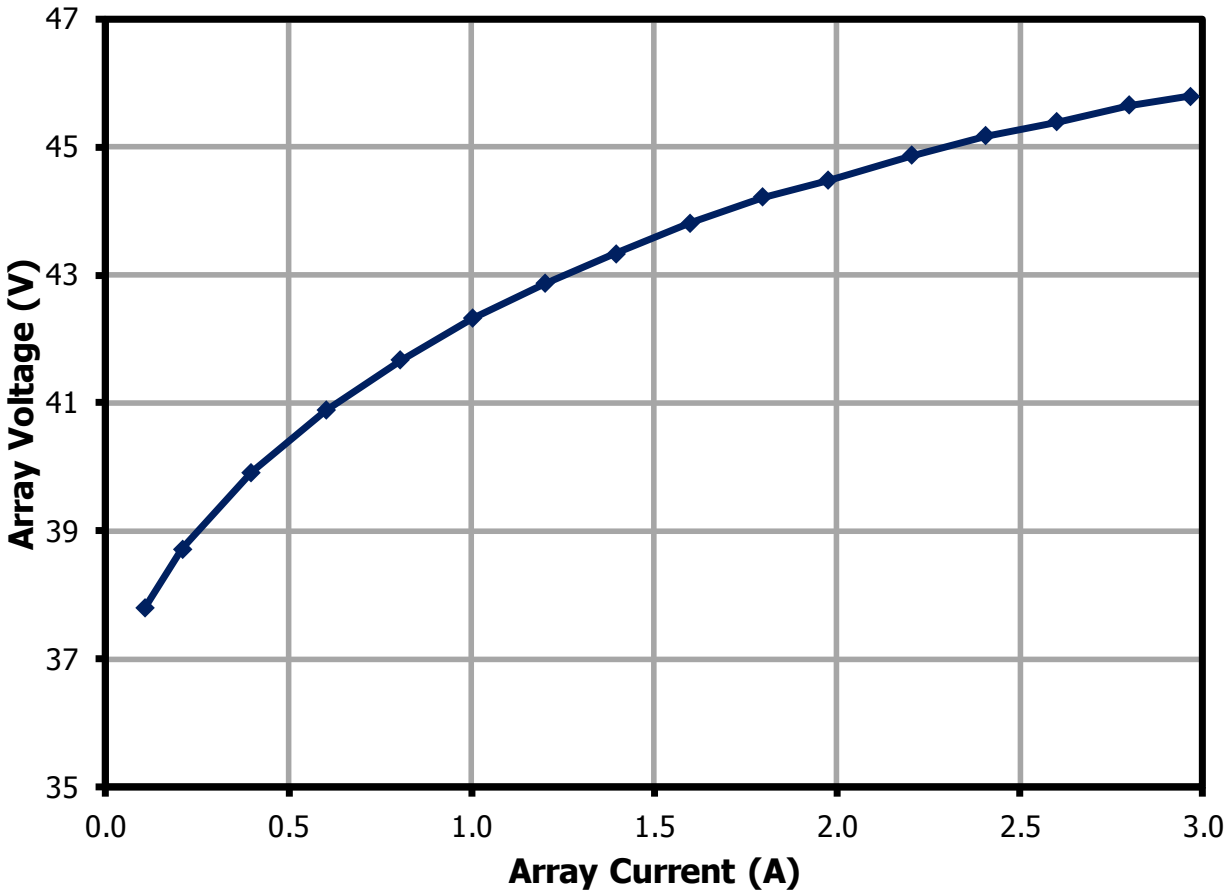

Figure 8 – Streetlight LED Array V-I Characteristic.

The voltage drop limits for high power LEDs can be loosely specified. The specification for the LEDs used in this design example states a voltage drop window of 2.8 V to 3.8 V at rated current and room temperature, not including the effects of temperature drift at ~2 mV / °C. So, at room temperature, a 14-LED string could present a voltage drop anywhere between 39 V to 54 V. This means that both the supply output voltage (39 V to 54 V) and output power (107.25 W to 148.5 W) vary depending on the characteristics of the individual LED panel.

The power supply driving this LED array must be able to provide at least 54 V to light a panel with worst-case maximum voltage, yet also maintain output current control down to 39 V and below for a panel on the low end of the voltage distribution. The power supply also needs to be able to deliver the power to drive a worst-case high-voltage panel without overheating. The median LED voltage drop is 3.3 V, so most panels will operate near the median voltage of 3.3 V X 14, or 46 V. The power supply, though designed to deliver near 150 W to a worst case panel, will in this case be operating at only around 46 V X 2.75 A, or 126.5 W.

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8 Constant Voltage Load

Since this power supply has a constant current output tailored for a relatively fixed constant voltage load, the usual constant current electronic load cannot be used for testing. For bench testing at maximum power, a constant resistance load can be used, set such that the supply output is at maximum output voltage (just before current limit). Other testing, including dimming and gain-phase, will require the actual LED load or a constant voltage load that closely mimics its characteristics.

An actual streetlight luminaire as a load can be unwieldy, and its light output can be distracting. To facilitate EMI and surge testing, a constant voltage load was constructed to emulate the behavior of the LED array in a much smaller package. The circuit is shown in Figure 9. The load consists of paralleled power Darlington transistors Q1-5, each with an emitter resistor (R1-5) to facilitate current sharing. Base resistors R6-10 help prevent oscillation. A string of thirteen 3 mm blue LEDs (D1-13) and one yellow-green LED (D14) are used as a voltage reference to mimic the characteristics of the LED panel. Resistor R11 is adjusted adjust the quiescent current though D1-14 to help match the characteristics of the LED panel. Resistors R12-16 add extra impedance in series with the load to approximate the characteristics of the LED panel. The completed array with heat sink is shown in Figure 9. A small 48 V fan is used to cool the heat sink when the load is operated for extended periods at full power. A cowl made of sheet plastic is used to direct the air flow from the fan. The V-I characteristics of the CV load are shown superimposed on those of the LED array in Figure 10. As can be seen from the graph, the emulator is most accurate at high power. An electronic load with appropriate rating and a constant voltage option (with some series resistance) can also be used for testing, but the load shown here has the advantage that no external AC power is needed.

8.1 *CV Load Schematic*

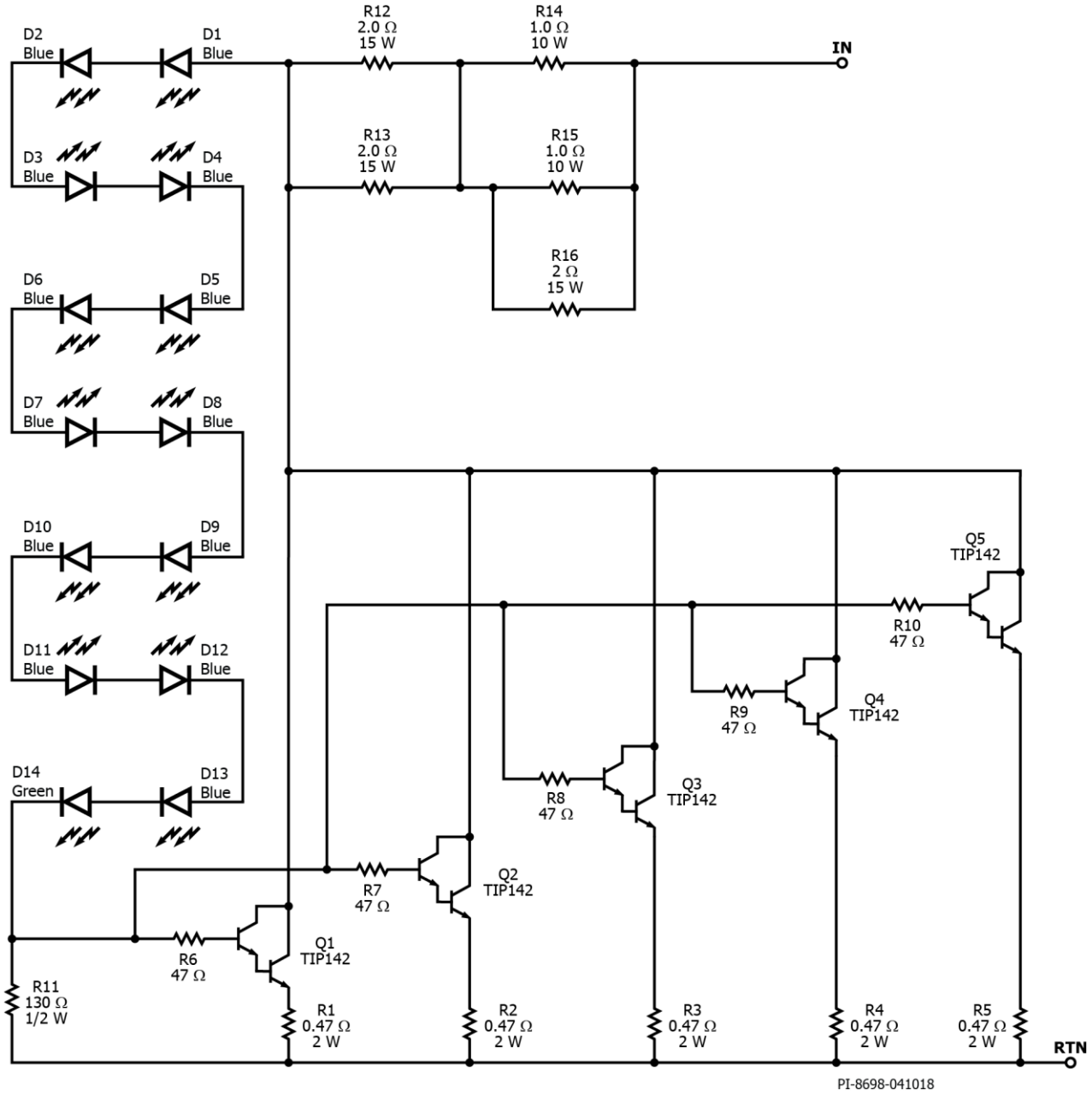

Figure 9 – Constant Voltage Load Schematic.

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8.2 *CV Load BOM*

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	13	D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13	LED, Blue Ultra Bright, 5 mm, 430 nm, 250 mcd	SL905BCE	Sloan
2	1	D14	LED, Green, 3 mm, 565 nm, 40 mcd	SSL-LX3044GD	Lumex Opto
3	5	Q1 Q2 Q3 Q4 Q5	NPN Darlington, Power, 100 V, 10 A, TO-247	TIP142G	On Semi
4	5	R1 R2 R3 R4 R5	RES, 0.47 Ω, 5%, 2 W, Metal Oxide	RSF200JB-0R47	Yageo
5	5	R6 R7 R8 R9 R10	RES, 47 Ω, 5%, 1/4 W, Carbon Film	CFR-25JB-47R	Yageo
6	1	R11	RES, 130 Ω, 5%, 1/2 W, Carbon Film	CFR-50JB-130R	Yageo
7	3	R12 R13 R16	RES, 2 Ω, 5%, 15 W, Wire Wound	280-CR15-2.0-RC	Xicon
8	2	R14 R15	RES, 1.0 Ω, 5%, 10 W, Wire Wound	280-CR10-1.0-RC	Xicon

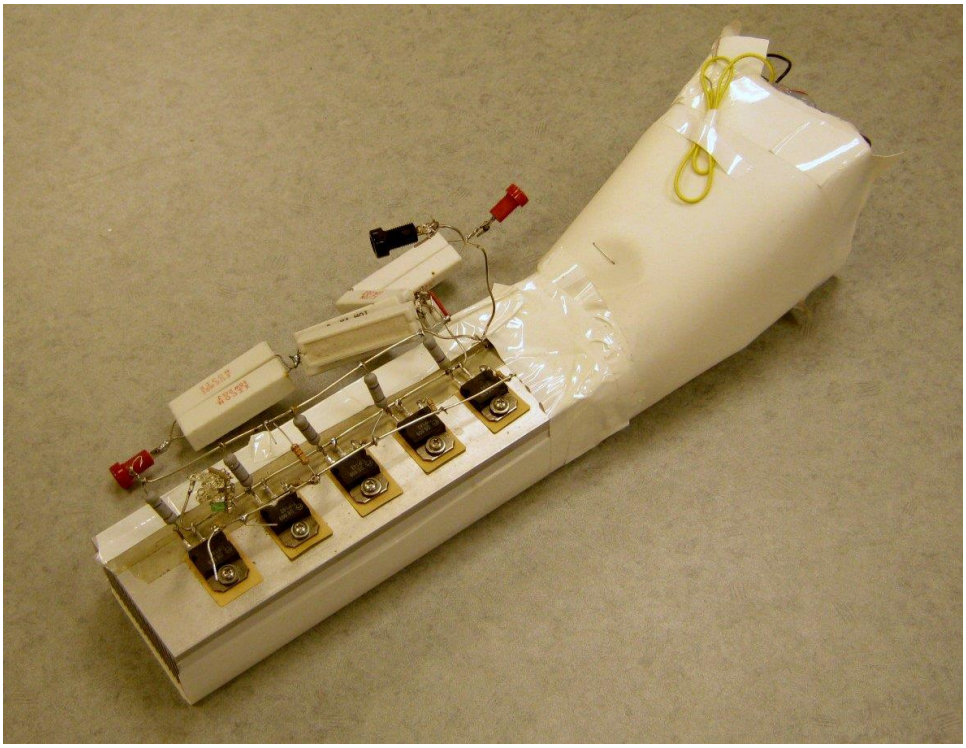

Figure 10 – Constant Voltage Load with Heat Sink and Fan/Shroud.

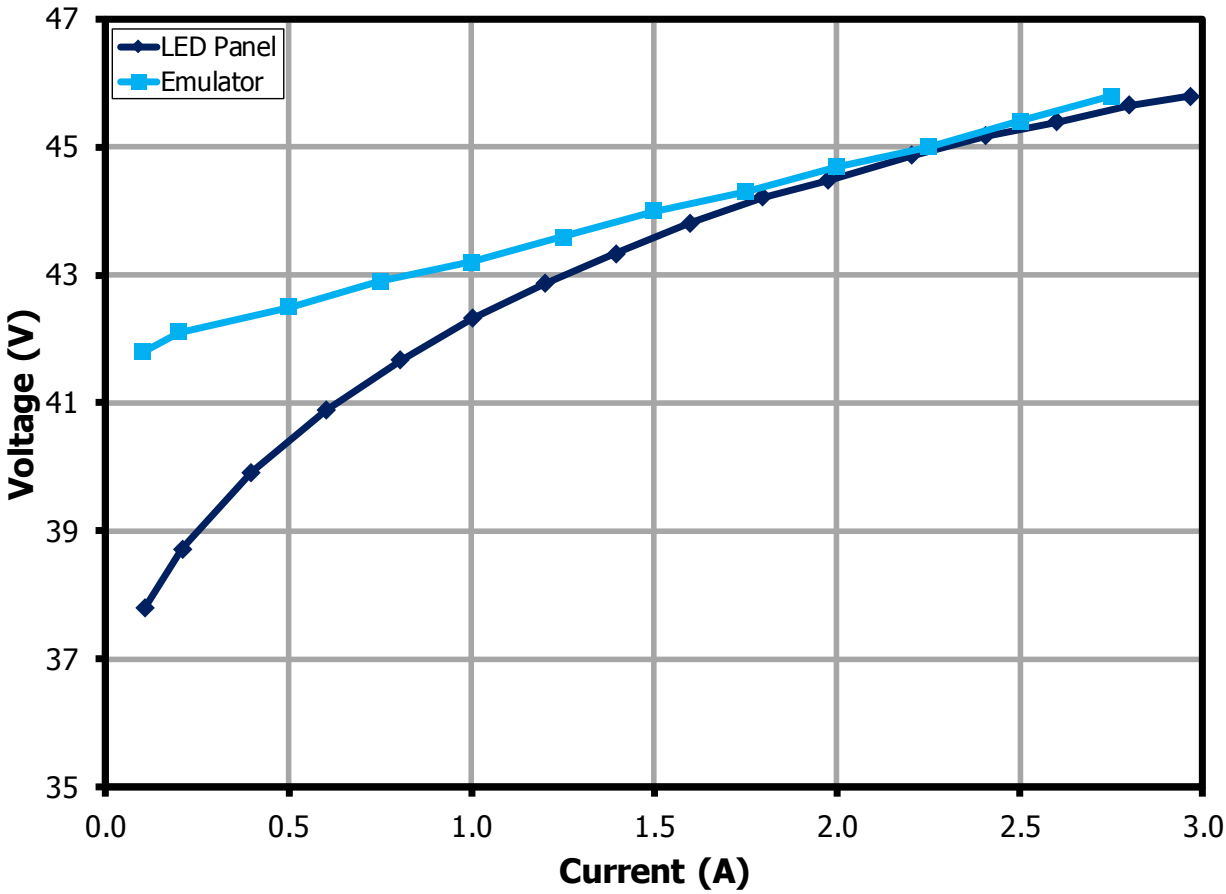

Figure 11 – Comparison of Streetlight LED Array V-I Characteristic with CV Load Emulator**.**

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9 Magnetics

9.1 *PFC Choke (L2) Specification*

9.1.1 *Electrical Diagram*

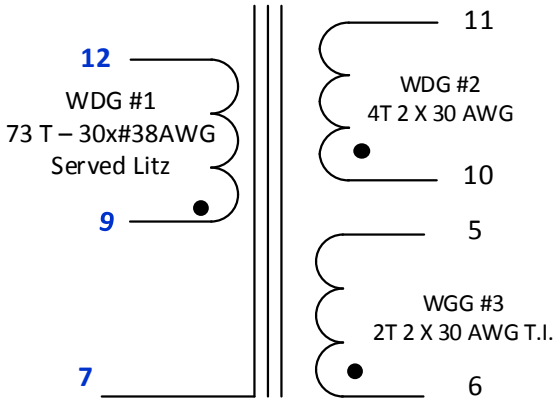

Figure 12 – PFC Choke Electrical Diagram.

9.1.2 *Electrical Specifications*

Inductance	Pins 9-12 measured at 100 kHz, 0.4 V_{RMS}.	489 µH +5%
Resonant Frequency	Pins 9-12. N/A	kHz (Min.)

9.1.3 *Material List*

Item	Description
[1]	Core: TDK Core: PC44PQ26/25.
[2]	Bobbin: PQ26/25-V-12 Pins (6/6).
[3]	Litz Wire: 30 #38 AWG Single Coated Solderable, Served.
[4]	Tape, Polyester Film: 3M 1350-F1 or equivalent, 13.5 mm Wide.
[5]	Tape. Polyester Web, 3M 44 or equivalent, 6 mm Wide.
[6]	Magnet Wire, #30 AWG, Solderable Double Coated.
[7]	Triple Insulated Wire, #30 AWG, Furukawa TEX-E or Equivalent.
[8]	Tape, Copper. 3M 1181 or Equivalent. 6 mm Wide.
[9]	Varnish: Dolph BC-359, or Equivalent.

9.1.4 *Build Diagram*

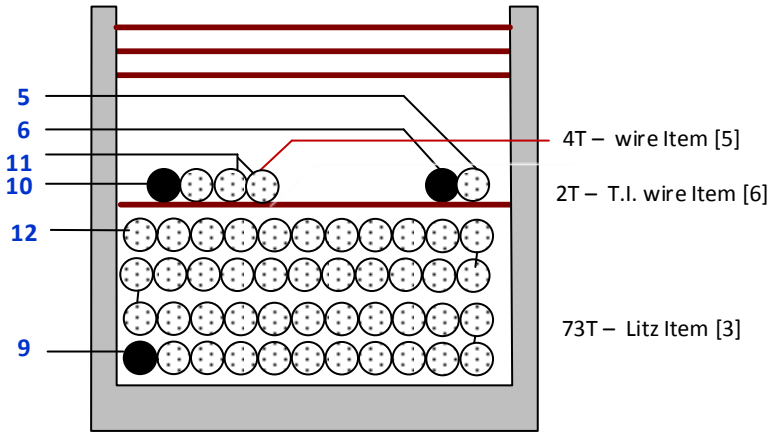

Figure 13 – PFC Inductor Build Diagram.

9.1.5 *Winding Instructions*

Winding Preparation	Place the bobbin on the mandrel with the pin side is on the left side. Winding direction is clockwise direction.
Winding #1	Starting at pin 9, wind 73 turns of Litz wire Item [3], finish at pin 12.
Insulation	Apply one layer of tape Item [4]. Add 15mm length of tape Item [5] over finish lead as shown in pictures for crossover insulation.
Winding #2	Starting at pin 10, wind 4 bifilar turns of wire, Item [6]. Spread turns evenly across bobbin window. Finish at pin 11. Route start and finish leads away from one another.
Winding #3	Starting at pin 6, wind 3 bifilar turns of wire, Item [7], directly on top of previous winding. Spread turns evenly across bobbin window. Finish at pin 5. Route start and finish leads away from one another.
Insulation	Apply 3 layers of tape Item [4].
Final Assembly	Grind cores to specified inductance. Secure core halves with tape [4]. Apply copper flux band around outside of completed choke as shown using copper tape [8]. Center the copper in the winding window, overlap ends and solder (see figure). Attach 2” wire [6] to copper foil near pin 7, terminate at pin 7. Wrap with 2 layers of tape [4]. Remove pins 1, 2, 3, 4, and 8. Dip varnish [9].

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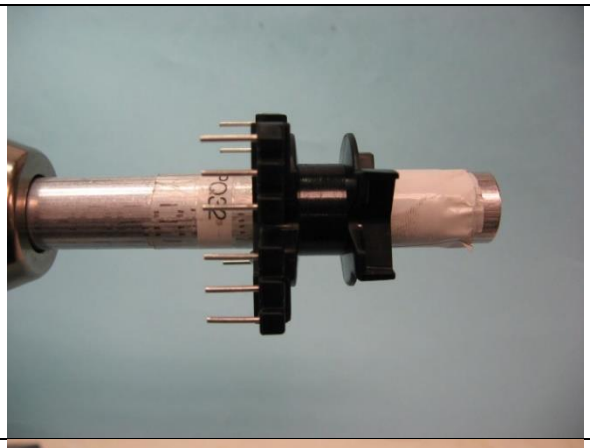
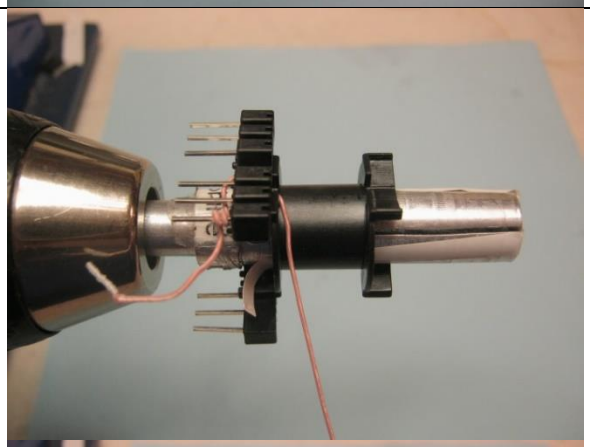
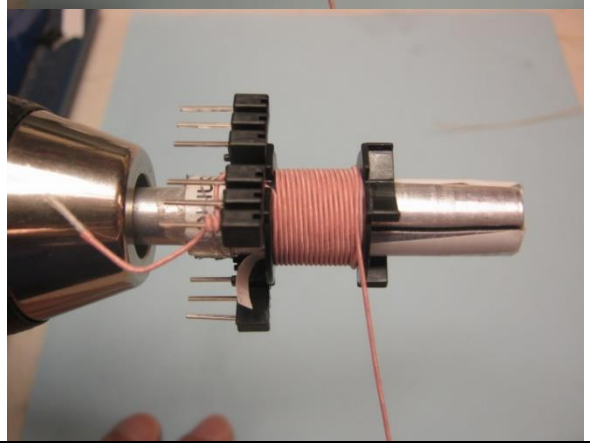
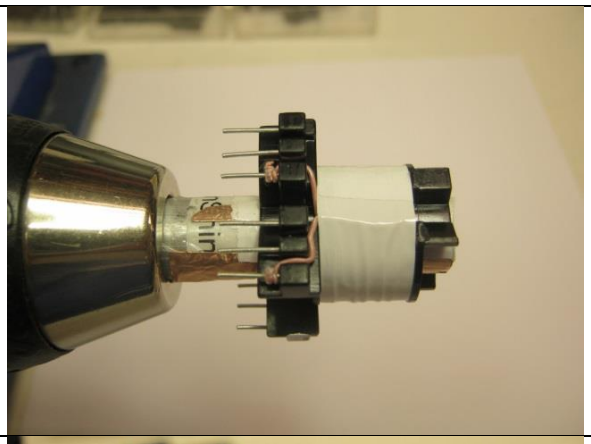
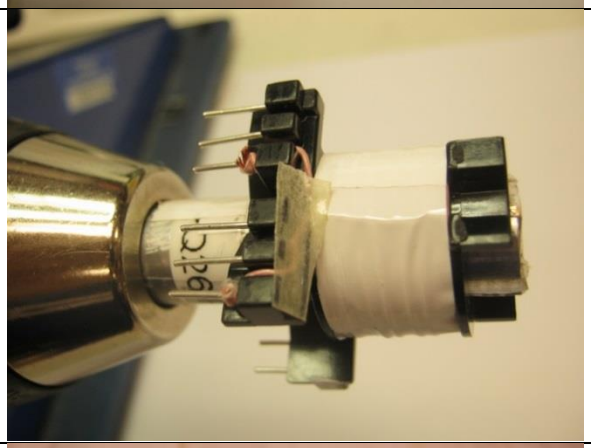
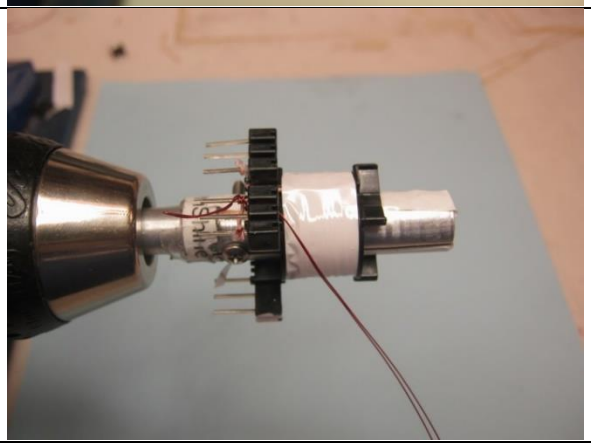
9.1.6 *Winding Illustrations*

Winding Preparation		Place the bobbin on the mandrel with the pin side is on the left side. Winding direction is clockwise direction
Winding 1	 	Starting at pin 9, wind 73 turns with 30 #38 served Litz wire, Item [3].

Insulation		Apply 1 layer of insulating tape, Item [4]. Terminate wire at pin 12
		Add 15 mm length of tape Item [5] over finish lead as shown in pictures for crossover insulation.
Winding 2		Starting at pin 10, wind 4 bifilar turns of wire, Item [6]. Spread turns evenly across bobbin window. Finish at pin 11. Route start and finish leads away from one another.

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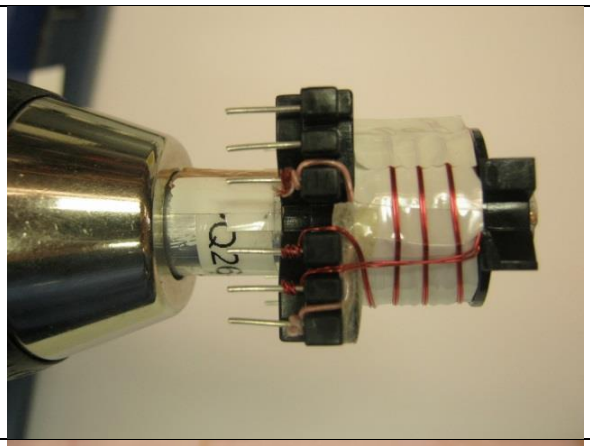
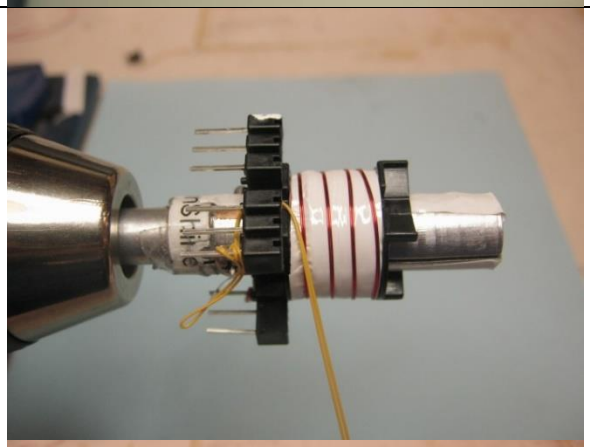
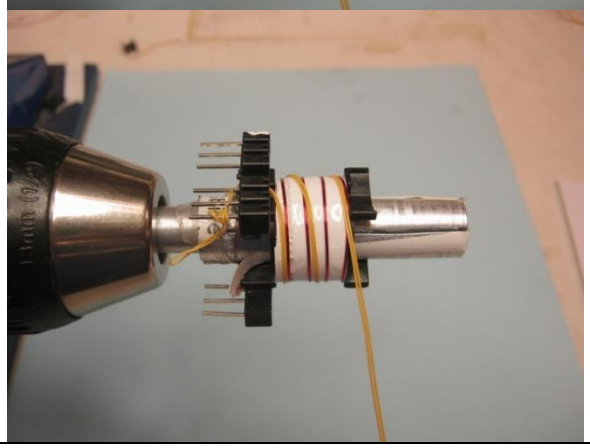
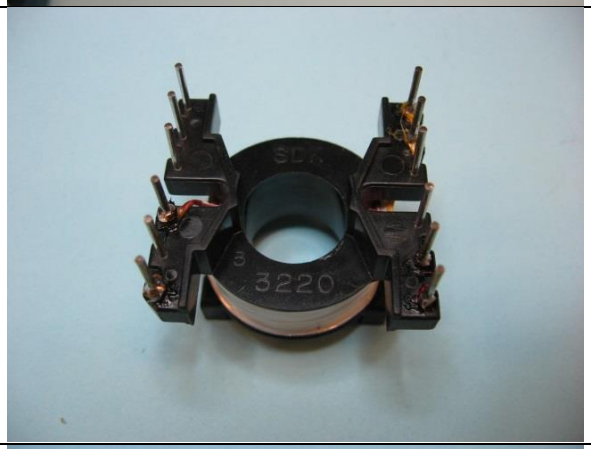
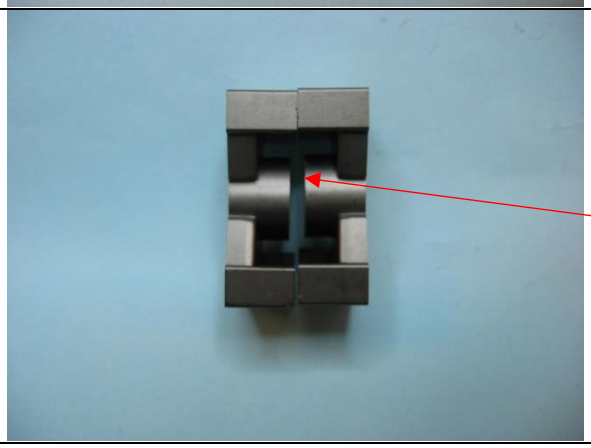
		
Winding 3	 	Starting at pin 6, wind 2 bifilar turns with #30 AWG triple insulated wire, Item [6]. Route start and finish leads away from one another.

Insulation		Apply 3 layers of insulating tape, Item [4]. Terminate wire at pin 5
Solder Terminations		Solder all wire terminations at pins 12, 9, 10, 11, 6, and 5.
Core Grinding		Grind core halves for specified inductance.

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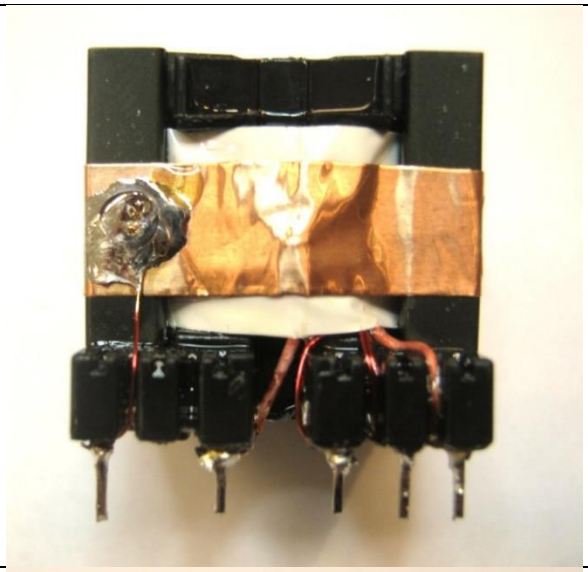
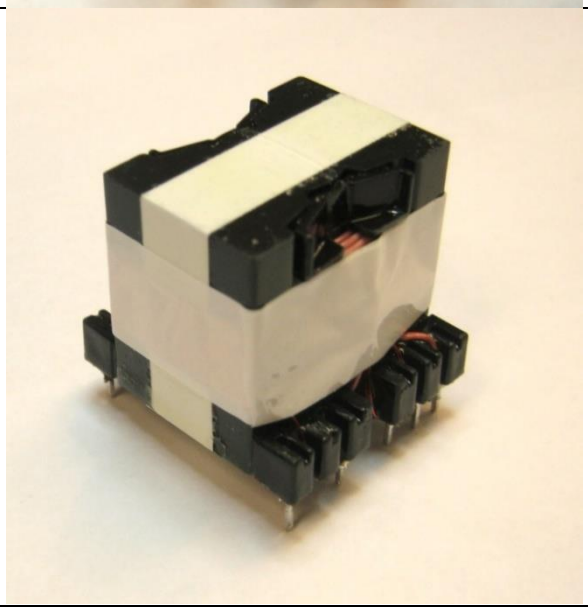
Final Assembly		Secure core halves with tape. Apply copper flux band around outside of completed choke as shown using copper tape [7]. Center the copper in the winding window, overlap ends and solder (see figure). Attach 2" wire [5] to copper foil near pin 7, terminate at pin 7. Wrap with 2 layers of tape [4]. Remove pins 1, 2, 3, 4, and 8. Dip varnish [9].
Finished Part		

9.2 *LLC Transformer (T2) Specification*

9.2.1 *Electrical Diagram*

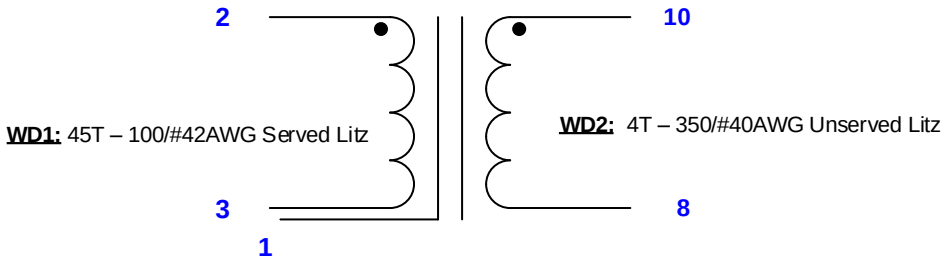


Figure 14 – LLC Transformer Schematic.

9.2.2 *Electrical Specifications*

Electrical Strength	1 second, 60 Hz, from pins 1-3 to 5-8.	3000 VAC
Primary Inductance	Pins 2-3, all other windings open, measured at 100 kHz, 0.4 V_{RMS}.	490 µH ±10%
Resonant Frequency	Pins 2-3, all other windings open.	1500 kHz (Min.)
Primary Leakage Inductance	Pins 2-3, with 8-10 shorted, measured at 100 kHz, 0.4 V_{RMS}.	124 µH ±5%

9.2.3 *Material List*

Item	Description
[1]	Core Pair: ETD34 /17/11 Ferroxcube 3C97 material or equivalent. Grind for A_L = 242 nH/t^2.
[2]	Bobbin: ETD-34-H-12Pins (6/6), PI#: 25-01048-00.
[3]	Bobbin Cover: ETD34.
[4]	Tape: Polyester Film, 3M 1350F-1 or equivalent, 24 mm Wide.
[5]	Litz Wire: 350/#40 AWG Single Coated, Unserved .
[6]	Litz Wire: 100/#42 Single Coated, Served.
[7]	Copper Tape, 3M-1181; or equivalent, 10 mm Wide.
[8]	Tinned Bus Wire, #24 AWG, Alpha 299 or Equivalent.
[9]	Varnish Dolph BC-359 or Equivalent.

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9.2.4 *Build Diagram*

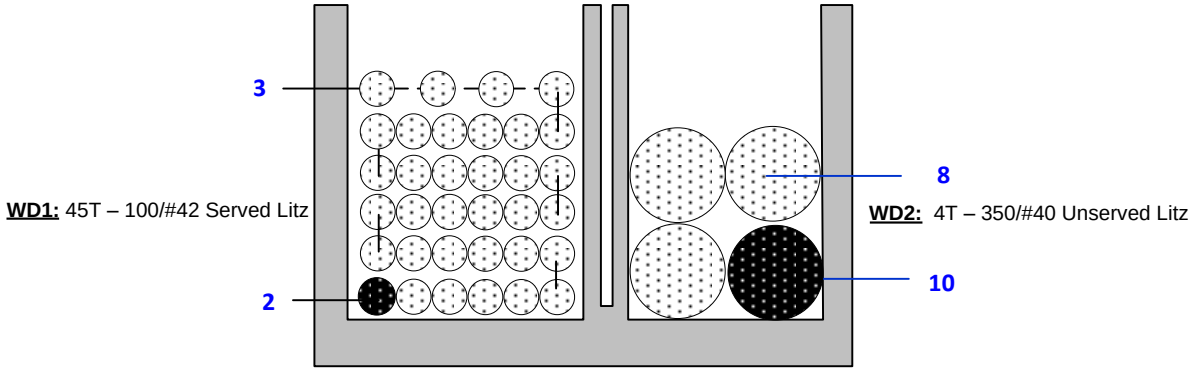
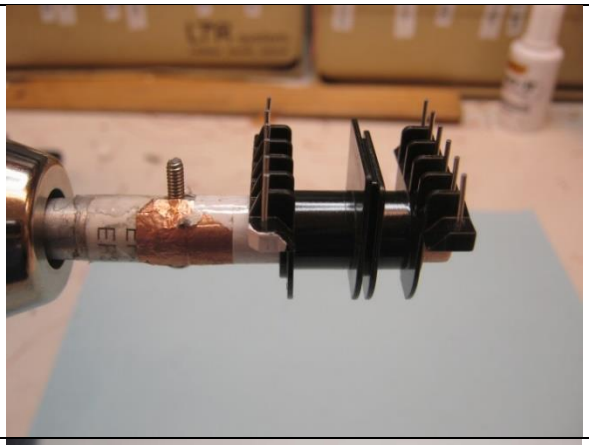
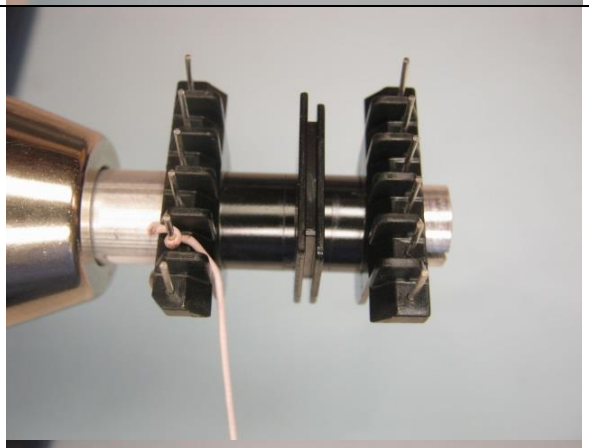
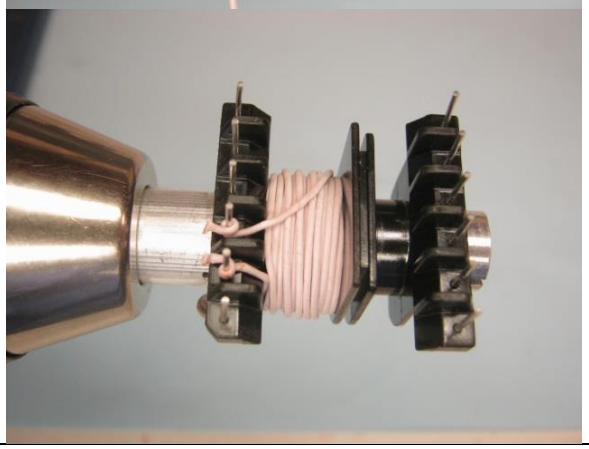


Figure 15 – LLC Transformer Build Diagram.

9.2.5 *Winding Instructions*

WD1 (Primary)	Place the bobbin Item [2] on the mandrel with pins 1-6 on the left side. Note: left-hand bobbin section will be used for primary, right-hand for secondary. Starting on pin 2, wind 45 turns of served Litz wire Item [6] in left side bobbin section and finish on pin 3.
WD2 (Secondary)	Using unserved Litz Item [5], start on pin 10, tightly wind 4 turns in right-hand bobbin section and finish on pin 8.
Bobbin Cover	Slide bobbin cover [3] into grooves in bobbin flanges as shown. Make sure cover is securely seated.
Finish	Grind core halves [1] for specified inductance. Assemble and secure core halves using circumferential turn of copper tape [7]. Overlap copper tape ends and solder. Solder 3/4" termination lead of bus wire Item [8] to copper core band close to pin 1 as shown, and terminate wire at pin 1. Wrap transformer with three turns of tape Item [4]. Fold over the tape wrap as shown to shroud finished transformer, keeping the primary and secondary windings open to air. Remove pins 5 and 6. Dip varnish [9].

9.2.6 *Winding Illustrations*

Winding Preparation		Place the bobbin Item [2] on the mandrel with pins 1-6 on the left side. Note: left-hand bobbin section will be used for primary, right-hand for secondary.
Winding 1 (Primary)	 	Starting on pin 2, wind 45 turns of served Litz wire Item [6] in left side bobbin section and finish on pin 3.

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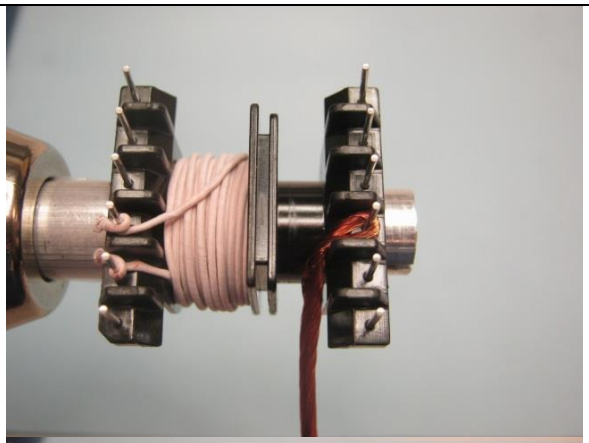
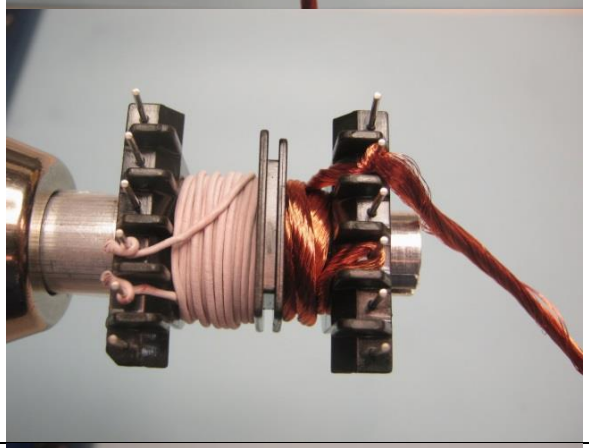
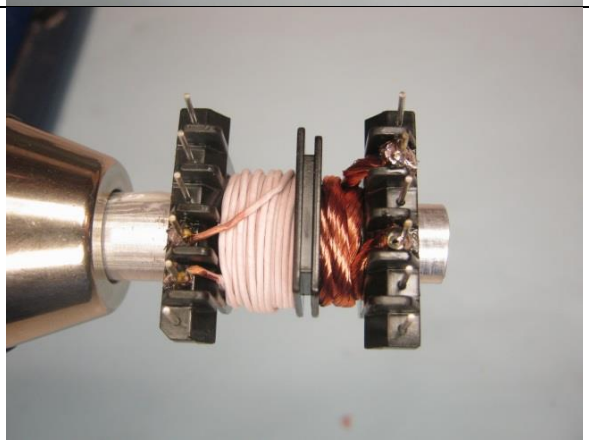
Winding 2 (Secondary)	 	Using unserved Litz Item [5], start on pin 10, tightly wind 4 turns in right-hand bobbin section and finish on pin 8.
Solder Termination		Solder all wire termination at pins 2, 3, 8 and 10.

Bobbin Cover		Slide bobbin cover [3] into grooves in bobbin flanges as shown. Make sure cover is securely seated.
Finish		Grind core halves [1] for specified inductance. Assemble and secure core halves using circumferential turn of copper tape [7]. Overlap copper tape ends and solder. Solder 3/4" termination lead of bus wire Item [8] to copper core band close to pin 1 as shown, and terminate wire at pin 1.
		Wrap transformer with three turns of tape Item [4]. Fold over the tape wrap as shown to shroud finished transformer, keeping the primary and secondary windings open to air. Remove pins 5 and 6. Dip varnish [9].

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9.3 *Output Inductor (L3) Specification*

9.3.1 *Electrical Diagram*

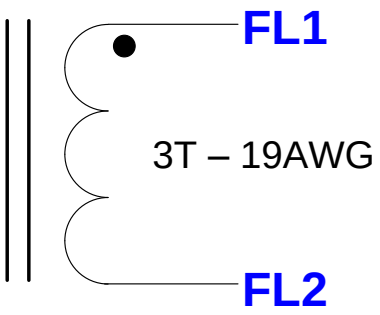

Figure 16 – Inductor Electrical Diagram.

9.3.2 *Electrical Specifications*

Inductance	Pins FL1-FL2, all other windings open, measured at 100 kHz, 0.4 $V_{RMS.}$	300 nH, ±15%

9.3.3 *Material List*

Item	Description
[1]	Powdered Iron Toroidal Core: Micrometals T30-26.
[2]	Magnet wire: #19 AWG Solderable Double Coated.

9.3.4 *Construction Details*

Figure 17 – Finished Part, Front View. Tin Leads to within ~1/8” of Toroid Body.

9.4 ***Output High Frequency Common Mode Choke***

9.4.1 *Electrical Diagram*

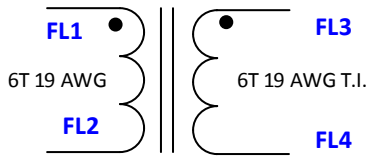

Figure 18 – Inductor Electrical Diagram.

9.4.2 *Electrical Specifications*

Inductance	FL1-2 or FL3-4, measured at 100 kHz, 0.4 V_{RMS}	120 µH, ±15%

9.4.3 *Material List*

Item	Description
[1]	Coated Ferrite Toroid: Fair-Rite 5975001121 or Equivalent.
[2]	Magnet Wire: #19 AWG Solderable Double Coated.
[3]	Triple Insulated Wire: #19 AWG, Furukawa TEX-E or Equivalent.

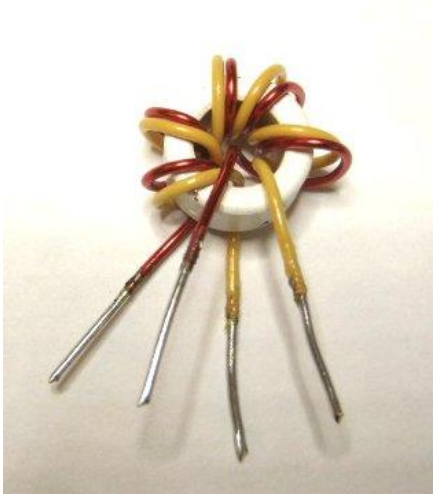

Figure 19 – Finished Inductor.

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10 PFC Design Spreadsheet

In this design, the spreadsheet generated warnings concerning the high value of KP selected, and for the operating current density of the Litz wire size selected for this design.

A high KP value can impact power factor and distortion, so a design generating this warning should be checked for any adverse impact. **This design met the requirements for power factor and harmonic distortion, and the high KP value allowed selection of a PQ26/25 ferrite core for the PFC inductor, with consequent inductor size reduction.**

A warning for current density indicates that the design should be checked in its initial stages for excessive temperature rise in the PFC inductor. The guidelines incorporated the spreadsheet are conservative, so that a warning does not necessarily mean that a given design will fail thermally. **The measured temperature rise for this design was satisfactory.**

Hiper_PFS-4_Boost_081616; Rev.0.5; Copyright Power Integrations 2016	**INPUT**	**INFO**	**OUTPUT**	**UNITS**	**Continuous Mode Boost Converter Design Spreadsheet**
Enter Application Variables					
Input Voltage Range	**Universal**		**Universal**		**Input voltage range**
VACMIN	100		100	VAC	Minimum AC input voltage. Spreadsheet simulation is performed at this voltage. To examine operation at other votlages, enter here, but enter fixed value for LPFC_ACTUAL.
VACMAX	300		300	VAC	Maximum AC input voltage
VBROWNIN		**Info**	91	VAC	Brown-IN voltage has been modified since the V-pin ratio is no longer 100:1
VBROWNOUT		**Info**	78	VAC	Brown-OUT voltage has been modified since the V-pin ratio is no longer 100:1
VO	440	**Info**	440	VDC	Brown IN/OUT voltage has changed due to modifications in the V-pin ratio from 100:1. Recommend Vpin ratio= FB pin ratio for optimized operation. Check the PF, input current distortion, brown in/out and power delivery
PO	160		160	W	Nominal Output power
fL			50	Hz	Line frequency
TA Max			40	°C	Maximum ambient temperature
n	0.95		0.95		Efficiency should be between 0.85 and 0.99. Also, refer to the Loss Budget section and ensure that the estimated efficiency is close to the simulated efficiency
VO_MIN			418	VDC	Minimum Output voltage
VO_RIPPLE_MAX			20	VDC	Maximum Output voltage ripple
tHOLDUP	15		15	ms	Holdup time
VHOLDUP_MIN			310	VDC	Minimum Voltage Output can drop to during holdup
I_INRUSH			40	A	Maximum allowable inrush current
Forced Air Cooling	**No**		**No**		Enter "Yes" for Forced air cooling. Otherwise enter "No". Forced air reduces

					acceptable choke current density and core autopick core size
KP and INDUCTANCE					
KP_TARGET	0.70		0.70		Target ripple to peak inductor current ratio at the peak of VACMIN. Affects inductance value
LPFC_TARGET (0 bias)			497	uH	PFC inductance required to hit KP_TARGET at peak of VACMIN and full load
LPFC_DESIRED (0 bias)			497	uH	LPFC value used for calculations. Leave blank to use LPFC_TARGET. Enter value to hold constant (also enter core selection) while changing VACMIN to examine brownout operation. Calculated inductance with rounded (integral) turns for powder core.
KP_ACTUAL			0.682		Actual KP calculated from LPFC_ACTUAL
LPFC_PEAK			497	uH	Inductance at VACMIN, 90°. For Ferrite, same as LPFC_DESIRED (0 bias)
Basic current parameters					
IAC_RMS			1.68	A	AC input RMS current at VACMIN and Full Power load
IO_DC			0.36	A	Output average current/Average diode current
PFS Parameters					
PFS Part Number	**Auto**		**PFS7625L/H**		If examining brownout operation, over-ride autopick with desired device size
Operating Mode	**Full Power**		**Full Power**		Mode of operation of PFS. For Full Power mode enter "Full Power" otherwise enter "EFFICIENCY" to indicate efficiency mode
IOCP min			5.5	A	Minimum Current limit
IOCP typ			5.9	A	Typical current limit
IOCP max			6.2	A	Maximum current limit
IP			3.51	A	MOSFET peak current
IRMS			1.50	A	PFS MOSFET RMS current
RDSON			0.59	Ohms	Typical RDSon at 100 'C
FS_PK			75	kHz	Estimated frequency of operation at crest of input voltage (at VACMIN)
FS_AVG			56	kHz	Estimated average frequency of operation over line cycle (at VACMIN)
PCOND_LOSS_PFS			1.3	W	Estimated PFS conduction losses
PSW_LOSS_PFS			1.2	W	Estimated PFS switching losses
PFS_TOTAL			2.5	W	Total Estimated PFS losses
TJ Max			100	deg C	Maximum steady-state junction temperature
Rth-JS			2.80	°C/W	Maximum thermal resistance (Junction to heatsink)
HEATSINK Theta-CA			20.75	°C/W	Maximum thermal resistance of heatsink
INDUCTOR DESIGN					
Basic Inductor Parameters					
LPFC (0 Bias)			497	uH	Value of PFC inductor at zero current. This is the value measured with LCR meter. For powder, it will be different than LPFC.
LP_TOL			10.0	%	Tolerance of PFC Inductor Value (ferrite only)
IL_RMS			1.75	A	Inductor RMS current (calculated at VACMIN and Full Power Load)
Material and Dimensions					
Core Type	**Ferrite**		**Ferrite**		Enter "Sendust", "Pow Iron" or "Ferrite"
Core Material	**Auto**		**PC44/PC95**		Select from 60u, 75u, 90u or 125 u for Sendust cores. Fixed at PC44/PC95 for Ferrite cores. Fixed at -52 material for Pow Iron cores.

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Core Geometry	**Auto**		**PQ**		Toroid only for Sendust and Powdered Iron; EE or PQ for Ferrite cores.
Core	**Auto**		**PQ26/25**		Core part number
Ae			118.00	mm^2	Core cross sectional area
Le			55.50	mm	Core mean path length
AL			6530.00	nH/t^2	Core AL value
Ve			6.53	cm^3	Core volume
HT (EE/PQ) / ID (toroid)			3.34	mm	Core height/Height of window; ID if toroid
MLT			56.2	mm	Mean length per turn
BW			13.80	mm	Bobbin width
LG			1.34	mm	Gap length (Ferrite cores only)
Flux and MMF calculations					
BP_TARGET (ferrite only)			3900	Gauss	Target flux density at worst case: IOCP and maximum tolerance inductance (ferrite only) - drives turns and gap
B_OCP (or BP)			3879	Gauss	Target flux density at worst case: IOCP and maximum tolerance inductance (ferrite only) - drives turns and gap
B_MAX			2084	Gauss	peak flux density at AC peak, VACMIN and Full Power Load, nominal inductance
µ_TARGET (powder only)			N/A	%	target µ at peak current divided by µ at zero current, at VACMIN, full load (powder only) - drives auto core selection
µ_MAX (powder only)			N/A	%	mu_max greater than 75% indicates a very large core. Please verify
µ_OCP (powder only)			N/A	%	µ at IOCPtyp divided by µ at zero current
I_TEST			5.9	A	Current at which B_TEST and H_TEST are calculated, for checking flux at a current other than IOCP or IP; if blank IOCP_typ is used.
B_TEST			3691	Gauss	Flux density at I_TEST and maximum tolerance inductance
µ_TEST (powder only)			N/A	%	µ at IOCP divided by µ at zero current, at IOCPtyp
Wire					
TURNS			74		Inductor turns. To adjust turns, change BP_TARGET (ferrite) or µ_TARGET (powder)
ILRMS			1.75	A	Inductor RMS current
Wire type	**Litz**		**Litz**		Select between "Litz" or "Magnet" for double coated magnet wire
AWG	38		38	AWG	Inductor wire gauge
Filar	30		30		Inductor wire number of parallel strands. Leave blank to auto-calc for Litz
OD (per strand)			0.102	mm	Outer diameter of single strand of wire
OD bundle (Litz only)			0.78	mm	Will be different than OD if Litz
DCR			0.39	ohm	Choke DC Resistance
P AC Resistance Ratio			1.25		Ratio of total Cu loss including HF ACR loss vs. assuming only DCR (uses Dowell equations)
J		**Warning**	7.18	A/mm^2	Current density is high, if copper loss is high use thicker wire, more strands, or larger core
FIT			97%	%	Percentage fill of winding window for EE/PQ core. Full window approx. 90%
Layers			3.76		Estimated layers in winding
Loss calculations					
BAC-p-p			1459	Gauss	Core AC peak-peak flux excursion at VACMIN, peak of sine wave
LPFC_CORE_LOSS			0.32	W	Estimated Inductor core Loss
LPFC_COPPER_LOSS			1.50	W	Estimated Inductor copper losses
LPFC_TOTAL_LOSS			1.82	W	Total estimated Inductor Losses

External PFC Diode					
DPFC_PFC Diode Part Number	**Auto**		LXA03T600		PFC Diode Part Number
Type			Qspeed		PFC Diode Type
Manufacturer			PI		Diode Manufacturer
VRRM			600.00	V	Diode rated reverse voltage
IF			3.00	A	Diode rated forward current
Qrr			50.00	nC	High Temperature
VF			2.10	V	Diode rated forward voltage drop
PCOND_DIODE			0.76	W	Estimated Diode conduction losses
PSW_DIODE			0.14	W	Estimated Diode switching losses
P_DIODE			0.90	W	Total estimated Diode losses
TJ Max			100	deg C	Maximum steady-state operating temperature
Rth-JS		**Warning**	1.90	degC/W	Warning, Rth too low
HEATSINK Theta-CA			64.12	degC/W	Maximum thermal resistance of heatsink
IFSM			23.00	A	Non-repetitive peak surge current rating. Consider larger size diode if inrush or thermal limited.
Output Capacitor					
COUT	**Auto**		68	uF	Minimum value of Output capacitance
VO_RIPPLE_EXPECTED			17.9	V	Expected ripple voltage on Output with selected Output capacitor
T_HOLDUP_EXPECTED			20.7	ms	Expected holdup time with selected Output capacitor
ESR_LF			2.93	ohms	Low Frequency Capacitor ESR
ESR_HF		**Warning**	1.17	ohms	!!! Warning high frequency ESR must be between 0.01 and 1 ohms
IC_RMS_LF			0.25	A	Low Frequency Capacitor RMS current
IC_RMS_HF			0.68	A	High Frequency Capacitor RMS current
CO_LF_LOSS			0.18	W	Estimated Low Frequency ESR loss in Output capacitor
CO_HF_LOSS			0.54	W	Estimated High frequency ESR loss in Output capacitor
Total CO LOSS			0.72	W	Total estimated losses in Output Capacitor
Input Bridge (BR1) and Fuse (F1)					
F1_I^2t Rating			6.12	A^2*s	Minimum I^2t rating for fuse
Fuse Current rating			2.61	A	Minimum Current rating of fuse
VF			0.90	V	Input bridge Diode forward Diode drop
IAVG			1.62	A	Input average current at 70 VAC.
PIV_INPUT BRIDGE			424	V	Peak inverse voltage of input bridge
PCOND_LOSS_BRIDGE			2.73	W	Estimated Bridge Diode conduction loss
CIN			0.5	uF	Input capacitor. Use metallized polypropylene or film foil type with high ripple current rating
RT1			10.61	ohms	Input Thermistor value
D_Precharge			1N5407		Recommended precharge Diode
PFS4 small signal components					
C_REF			1.0	uF	REF pin capacitor value
RV1			4.0	MOhms	Line sense resistor 1
RV2			6.0	MOhms	Line sense resistor 2
RV3			6.0	MOhms	Typical value of the lower resistor connected to the V-PIN. Use 1% resistor only!
RV4			141.2	kOhms	Description pending, could be modified based on feedback chain R1-R4
C_V			0.566	nF	V pin decoupling capacitor (RV4 and C_V should have a time constant of 80us) Pick the closest available capacitance.
C_VCC			1.0	uF	Supply decoupling capacitor
C_C			100	nF	Feedback C pin decoupling capacitor
Power good Vo lower			333	V	Vo lower threshold voltage at which power

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threshold VPG(L)					good signal will trigger
PGT set resistor			291.4	kohm	Power good threshold setting resistor
Feedback Components					
R1			4.0	Mohms	Feedback network, first high voltage divider resistor
R2			6.0	Mohms	Feedback network, second high voltage divider resistor
R3			6.0	Mohms	Feedback network, third high voltage divider resistor
R4			141.2	kohms	Feedback network, lower divider resistor
C1			0.566	nF	Feedback network, loop speedup capacitor. (R4 and C1 should have a time constant of 80us) Pick the closest available capacitance.
R5			21.5	kohms	Feedback network: zero setting resistor
C2			1000	nF	Feedback component- noise suppression capacitor
Loss Budget (Estimated at VACMIN)					
PFS Losses			2.55	W	Total estimated losses in PFS
Boost diode Losses			0.90	W	Total estimated losses in Output Diode
Input Bridge losses			2.73	W	Total estimated losses in input bridge module
Inductor losses			1.82	W	Total estimated losses in PFC choke
Output Capacitor Loss			0.72	W	Total estimated losses in Output capacitor
EMI choke copper loss			0.50	W	Total estimated losses in EMI choke copper
Total losses			8.72	W	Overall loss estimate
Efficiency			0.95		Estimated efficiency at VACMIN, full load.
CAPZero component selection recommendation					
CAPZero Device			CAP200DG		(Optional) Recommended CAPZero device to discharge X-Capacitor with time constant of 1 second
Total Series Resistance (Rcapzero1+Rcapzero2)			0.78	k-ohms	Maximum Total Series resistor value to discharge X-Capacitors
EMI filter components recommendation					
CIN_RECOMMENDED			680	nF	Metallized polyester film capacitor after bridge, ratio with Po
CX2			470	nF	X capacitor after differencial mode choke and before bridge, ratio with Po
LDM_calc			220	uH	estimated minimum differencial inductance to avoid <10kHz resonance in input current
CX1			470	nF	X capacitor before common mode choke, ratio with Po
LCM			10	mH	typical common mode choke value
LCM_leakage			30	uH	estimated leakage inductance of CM choke, typical from 30~60uH
CY1 (and CY2)			220	pF	typical Y capacitance for common mode noise suppression
LDM_Actual			190	uH	cal_LDM minus LCM_leakage, utilizing CM leakage inductance as DM choke.
DCR_LCM	0.10		0.10	Ohms	total DCR of CM choke for estimating copper loss
DCR_LDM	0.10		0.10	Ohms	total DCR of DM choke(or CM #2) for estimating copper loss
Note: CX2 can be placed between CM choke and DM choke depending on EMI design requirement.					

11 LLC Transformer Design Spreadsheet

To optimize the transformer design for a wide output voltage range, three spreadsheets are generated. The first generated is for the nominal panel voltage of 46 V. The transformer parameters are locked into this spreadsheet, then two more spreadsheets are generated from the nominal spreadsheet for the extreme operating points of 39 V and 54 V. The nominal spreadsheet parameters are adjusted until operation is satisfactory for the extreme operating points as well as nominal. This usually means that the transformer turns are adjusted so that the transformer flux swing at the high voltage operating extreme is acceptable. The supply operates at the desired nominal frequency for the 46 V median output voltage. Operating frequency drops from nominal for 54 V output, and increases for 39 V operation. To accommodate the high output voltage/low operating frequency case, the transformer turns are adjusted for an acceptable flux swing at the lower operating frequency. K ratio for the nominal spreadsheet (spreadsheet line 46) is set to ~3 to reduce frequency sensitivity vs. output load to help control frequency excursion at low output voltage, low current and avoid burst mode.

This approach optimizes efficiency for the most commonly encountered operating conditions. A supply designed using this approach also has a much smaller frequency excursion over the output voltage extremes than for a design optimized with a single spreadsheet for the 54 V maximum voltage/power condition. Overall efficiency was also higher for the design optimized for the median voltage.

11.1 *Component Adjustments Needed for Voltage Doubler Design*

Some of the transformer and circuit parameters need to be changed from the spreadsheet values for use with a voltage doubler output configuration. **Transformer secondary turns (spreadsheet line 52) should be halved for a voltage doubler design, with twice as much wire area to compensate for increased current in the winding.**

To aid startup at maximum output power, the value for current sense resistor as shown on line 195 was adjusted for a higher overcurrent limit than the initial value shown in the spreadsheet. The current limit resistor for the 54 V spreadsheet should be used as the starting point, as this is the highest operating power point. The final value for primary current sense resistor is determined on the bench in initial testing. A 3 A repetitive current limit allowed startup under worst-case conditions and helped prevent auto-restart during differential mode surge testing. This yields a value of primary current sense resistor of 43 Ω. The soft start capacitor value (Line 184) was changed from the default spreadsheet value of 330 nF to 680 nF (determined by bench testing) to aid startup into a constant voltage load.

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11.2 ***Warning Messages***

In all three spreadsheets, a warning message is generated for OV shutdown (VOV_shut, line 6). This is a consequence of raising the Vbulk_nom (line 3) to 440 VDC to allow for sufficient headroom for operating the PFC stage at 277 VAC input to accommodate US commercial/industrial lighting applications.

The spreadsheet for both the high (54V) and low (39V) output voltage extremes will display a warning message for Vres_expected (line 59). This is a consequence of the frequency shifts required for regulation at the two output voltage extremes, and is expected. This message can be ignored.

The spreadsheet for minimum output voltage (39V) displays an error message for device selection (line 26). This is because at minimum output voltage, the output power is considerably less than at nominal or maximum output voltage. This message should be ignored.

11.3 *Nominal Output Voltage (46 V) Spreadsheet*

HiperLCS_042413; Rev.1.3; Copyright Power Integrations 2013	INPUTS	INFO	OUTPUTS	UNITS	HiperLCS_042413_Rev1-3.xls; HiperLCS Half-Bridge, Continuous mode LLC Resonant Converter Design Spreadsheet
Enter Input Parameters					
Vbulk_nom	440		440	V	Nominal LLC input voltage
Vbrownout	330		330	V	Brownout threshold voltage. HiperLCS will shut down if voltage drops below this value. Allowable value is between 65% and 76% of Vbulk_nom. Set to 65% for max holdup time
Vbrownin			416	V	Startup threshold on bulk capacitor
VOV_shut		Warning	548	V	!!! Warning. OV shutdown voltage is too high. Reduce Vbulk_nom OR Vbrownout
VOV_restart			528	V	Restart voltage after OV protection.
CBULK	68.00		68	uF	Minimum value of bulk cap to meet holdup time requirement; Adjust holdup time and Vbrownout to change bulk cap value
tHOLDUP			21.9	ms	Bulk capacitor hold up time
Enter LLC (secondary) outputs					**The spreadsheet assumes AC stacking of the secondaries**
VO1	46.00		46.00	V	Main Output Voltage. Spreadsheet assumes that this is the regulated output
IO1	2.75		2.75	A	Main output maximum current
VD1	0.70		0.70	V	Forward voltage of diode in Main output
PO1			127	W	Output Power from first LLC output
VO2			0.00	V	Second Output Voltage
IO2			0.00	A	Second output current
VD2			0.70	V	Forward voltage of diode used in second output
PO2			0.00	W	Output Power from second LLC output
P_LLC			127	W	Specified LLC output power
LCS Device Selection					
Device	**LCS702**		**LCS702**		**LCS Device**
RDS-ON (MAX)			1.39	ohms	RDS-ON (max) of selected device
Coss			250	pF	Equivalent Coss of selected device
Cpri			40	pF	Stray Capacitance at transformer primary
Pcond_loss			1.5	W	Conduction loss at nominal line and full load
Tmax-hs			90	deg C	Maximum heatsink temperature
Theta J-HS			9.1	deg C/W	Thermal resistance junction to heatsink (with grease and no insulator)
Expected Junction temperature			103	deg C	Expectd Junction temperature
Ta max			50	deg C	Expected max ambient temperature
Theta HS-A			27	deg C/W	Required thermal resistance heatsink to ambient
LLC Resonant Parameter and Transformer Calculations (generates red curve)					
Vres_target	450.00		450	V	Desired Input voltage at which power train operates at resonance. If greater than Vbulk_nom, LLC operates below resonance at VBULK.
Po			128	W	LLC output power including diode loss
Vo			46.70	V	Main Output voltage (includes diode drop) for calculating Nsec and turns ratio
f_target	120.00		120	kHz	Desired switching frequency at Vbulk_nom. 66 kHz to 300 kHz, recommended 180-250 kHz
Lpar			366	uH	Parallel inductance. (Lpar = Lopen - Lres for integrated transformer; Lpar = Lmag for non-integrated low-leakage transformer)
Lpri	490.00		490	uH	Primary open circuit inductance for integrated transformer; for low-leakage transformer it is sum of primary inductance and series inductor. If left blank, auto-calculation shows value necessary for slight loss of ZVS at ~80% of Vnom

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	124.00		124.0	uH	Series inductance or primary leakage inductance of integrated transformer; if left blank auto-calculation is for K=4
Kratio			3.0		Ratio of Lpar to Lres. Maintain value of K such that 2.1 < K < 11. Preferred Lres is such that K<7.
Cres	12.00		12.0	nF	Series resonant capacitor. Red background cells produce red graph. If Lpar, Lres, Cres, and n_RATIO_red_graph are left blank, they will be auto-calculated
Lsec	16.300		16.300	uH	Secondary side inductance of one phase of main output; measure and enter value, or adjust value until f_predicted matches what is measured ;
15			41	%	Leakage distribution factor (primary to secondary). >50% signifies most of the leakage is in primary side. Gap physically under secondary yields >50%, requiring fewer primary turns.
n_eq			4.74		Turns ratio of LLC equivalent circuit ideal transformer
Npri	45.0		45.0		Primary number of turns; if input is blank, default value is auto-calculation so that f_predicted = f_target and m=50%
Nsec	8.0		8.0		Secondary number of turns (each phase of Main output). Default value is estimate to maintain BAC<=200 mT, using selected core (below)
f_predicted			127	kHz	Expected frequency at nominal input voltage and full load; Heavily influenced by n_eq and primary turns
f_res			130	kHz	Series resonant frequency (defined by series inductance Lres and C)
f_brownout			100	kHz	Expected switching frequency at Vbrownout, full load. Set HiperLCS minimum frequency to this value.
f_par			66	kHz	Parallel resonant frequency (defined by Lpar + Lres and C)
f_inversion			79	kHz	LLC full load gain inversion frequency. Operation below this frequency results in operation in gain inversion region.
Vinversion			198	V	LLC full load gain inversion point input voltage
Vres_expected			443	V	Expected value of input voltage at which LLC operates at resonance.
RMS Currents and Voltages					
IRMS_LLC_Primary			1.03	A	Primary winding RMS current at full load, Vbulk_nom and f_predicted
Winding 1 (Lower secondary Voltage) RMS current			2.2	A	Winding 1 (Lower secondary Voltage) RMS current
Lower Secondary Voltage Capacitor RMS current			1.4	A	Lower Secondary Voltage Capacitor RMS current
Winding 2 (Higher secondary Voltage) RMS current			0.0	A	Winding 2 (Higher secondary Voltage) RMS current
Higher Secondary Voltage Capacitor RMS current			0.0	A	Higher Secondary Voltage Capacitor RMS current
Cres_Vrms			108	V	Resonant capacitor AC RMS Voltage at full load and nominal input voltage
Virtual Transformer Trial - (generates blue curve)					
New primary turns			45.0		Trial transformer primary turns; default value is from resonant section
New secondary turns			8.0		Trial transformer secondary turns; default value is from resonant section
New Lpri			490	uH	Trial transformer open circuit inductance; default value is from resonant section
New Cres			12.0	nF	Trial value of series capacitor (if left blank calculated value chosen so f_res same as in main resonant section above

New estimated Lres			124.0	uH	Trial transformer estimated Lres
New estimated Lpar			366	uH	Estimated value of Lpar for trial transformer
New estimated Lsec			16.300	uH	Estimated value of secondary leakage inductance
New Kratio			3.0		Ratio of Lpar to Lres for trial transformer
New equivalent circuit transformer turns ratio			4.74		Estimated effective transformer turns ratio
V powertrain inversion new			198	V	Input voltage at LLC full load gain inversion point
f_res_trial			130	kHz	New Series resonant frequency
f_predicted_trial			127	kHz	New nominal operating frequency
IRMS_LLC_Primary			1.03	A	Primary winding RMS current at full load and nominal input voltage (Vbulk) and f_predicted_trial
Winding 1 (Lower secondary Voltage) RMS current			2.2	A	RMS current through Output 1 winding, assuming half sinusoidal waveshape
Lower Secondary Voltage Capacitor RMS current			1.5	A	Lower Secondary Voltage Capacitor RMS current
Winding 2 (Higher secondary Voltage) RMS current			2.2	A	RMS current through Output 2 winding; Output 1 winding is AC stacked on top of Output 2 winding
Higher Secondary Voltage Capacitor RMS current			0.0	A	Higher Secondary Voltage Capacitor RMS current
Vres_expected_trial			443	V	Expected value of input voltage at which LLC operates at resonance.
Transformer Core Calculations (Calculates From Resonant Parameter Section)					
Transformer Core	**EER28L**		**EER28L**		**Transformer Core**
Ae	0.97		0.97	cm^2	Enter transformer core cross-sectional area
Ve	7.64		7.64	cm^3	Enter the volume of core
Aw	123.00		123.0	mm^2	Area of window
Bw	20.90		20.9	mm	Total Width of Bobbin
Loss density			200.0	mW/cm^3	Enter the loss per unit volume at the switching frequency and BAC (Units same as kW/m^3)
MLT			4.0	cm	Mean length per turn
Nchambers			2		Number of Bobbin chambers
Wsep			3.0	mm	Winding separator distance (will result in loss of winding area)
Ploss			1.5	W	Estimated core loss
Bpkfmin			151	mT	First Quadrant peak flux density at minimum frequency.
BAC			236	mT	AC peak to peak flux density (calculated at f_predicted, Vbulk at full load)
Primary Winding					
Npri			45.0		Number of primary turns; determined in LLC resonant section
Primary gauge	42		42	AWG	Individual wire strand gauge used for primary winding
Equivalent Primary Metric Wire gauge			0.060	mm	Equivalent diameter of wire in metric units
Primary litz strands	100		100		Number of strands in Litz wire; for non-litz primary winding, set to 1
Primary Winding Allocation Factor			50	%	Primary window allocation factor - percentage of winding space allocated to primary
AW_P			53	mm^2	Winding window area for primary
Fill Factor			40%	%	% Fill factor for primary winding (typical max fill is 60%)
Resistivity_25 C_Primary			59.29	m-ohm/m	Resistivity in milli-ohms per meter
Primary DCR 25 C			105.45	m-ohm	Estimated resistance at 25 C
Primary DCR 100 C			141.30	m-ohm	Estimated resistance at 100 C (approximately 33% higher than at 25 C)
Primary RMS current			1.03	A	Measured RMS current through the primary winding
ACR_Trf_Primary			228.32	m-ohm	Measured AC resistance (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature

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Primary copper loss			0.24	W	Total primary winding copper loss at 85 C
Primary Layers			3.91		Number of layers in primary Winding
Secondary Winding 1 (Lower secondary voltage OR Single output)					**Note - Power loss calculations are for each winding half of secondary**
Output Voltage			46.00	V	Output Voltage (assumes AC stacked windings)
Sec 1 Turns			8.00		Secondary winding turns (each phase)
Sec 1 RMS current (total, AC+DC)			2.2	A	RMS current through Output 1 winding, assuming half sinusoidal waveshape
Winding current (DC component)			1.38	A	DC component of winding current
Winding current (AC RMS component)			1.71	A	AC component of winding current
Sec 1 Wire gauge	40		40	AWG	Individual wire strand gauge used for secondary winding
Equivalent secondary 1 Metric Wire gauge			0.080	mm	Equivalent diameter of wire in metric units
Sec 1 litz strands	350		350		Number of strands used in Litz wire; for non-litz non-integrated transformer set to 1
Resistivity_25 C_sec1			10.65	m-ohm/m	Resistivity in milli-ohms per meter
DCR_25C_Sec1			3.37	m-ohm	Estimated resistance per phase at 25 C (for reference)
DCR_100C_Sec1			4.51	m-ohm	Estimated resistance per phase at 100 C (approximately 33% higher than at 25 C)
DCR_Ploss_Sec1			0.07	W	Estimated Power loss due to DC resistance (both secondary phases)
ACR_Sec1			4.79	m-ohm	Measured AC resistance per phase (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature. Default value of ACR is twice the DCR value at 100 C
ACR_Ploss_Sec1			0.03	W	Estimated AC copper loss (both secondary phases)
Total winding 1 Copper Losses			0.10	W	Total (AC + DC) winding copper loss for both secondary phases
Capacitor RMS current			1.4	A	Output capacitor RMS current
Co1			2.4	uF	Secondary 1 output capacitor
Capacitor ripple voltage			3.0	%	Peak to Peak ripple voltage on secondary 1 output capacitor
Output rectifier RMS Current			2.2	A	Schottky losses are a stronger function of load DC current. Sync Rectifier losses are a function of RMS current
Secondary 1 Layers			1.73		Number of layers in secondary 1 Winding
Secondary Winding 2 (Higher secondary voltage)					**Note - Power loss calculations are for each winding half of secondary**
Output Voltage			0.00	V	Output Voltage (assumes AC stacked windings)
Sec 2 Turns			0.00		Secondary winding turns (each phase) AC stacked on top of secondary winding 1
Sec 2 RMS current (total, AC+DC)			2.2	A	RMS current through Output 2 winding; Output 1 winding is AC stacked on top of Output 2 winding
Winding current (DC component)			0.0	A	DC component of winding current
Winding current (AC RMS component)			0.0	A	AC component of winding current
Sec 2 Wire gauge			40	AWG	Individual wire strand gauge used for secondary winding
Equivalent secondary 2 Metric Wire gauge			0.080	mm	Equivalent diameter of wire in metric units
Sec 2 litz strands			0		Number of strands used in Litz wire; for non-litz non-integrated transformer set to 1
Resistivity_25 C_sec2			37290.65	m-ohm/m	Resistivity in milli-ohms per meter
Transformer Secondary MLT			3.95	cm	Mean length per turn

DCR_25C_Sec2			0.00	m-ohm	Estimated resistance per phase at 25 C (for reference)
DCR_100C_Sec2			0.00	m-ohm	Estimated resistance per phase at 100 C (approximately 33% higher than at 25 C)
DCR_Ploss_Sec1			0.00	W	Estimated Power loss due to DC resistance (both secondary halves)
ACR_Sec2			0.00	m-ohm	Measured AC resistance per phase (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature. Default value of ACR is twice the DCR value at 100 C
ACR_Ploss_Sec2			0.00	W	Estimated AC copper loss (both secondary halves)
Total winding 2 Copper Losses			0.00	W	Total (AC + DC) winding copper loss for both secondary halves
Capacitor RMS current			0.0	A	Output capacitor RMS current
Co2			N/A	uF	Secondary 2 output capacitor
Capacitor ripple voltage			N/A	%	Peak to Peak ripple voltage on secondary 1 output capacitor
Output rectifier RMS Current			0.0	A	Schottky losses are a stronger function of load DC current. Sync Rectifier losses are a function of RMS current
Secondary 2 Layers			1.00		Number of layers in secondary 2 Winding
Transformer Loss Calculations					**Does not include fringing flux loss from gap**
Primary copper loss (from Primary section)			0.24	W	Total primary winding copper loss at 85 C
Secondary copper Loss			0.10	W	Total copper loss in secondary winding
Transformer total copper loss			0.34	W	Total copper loss in transformer (primary + secondary)
AW_S			52.67	mm^2	Area of window for secondary winding
Secondary Fill Factor			89%	%	% Fill factor for secondary windings; typical max fill is 60% for served and 75% for unserved Litz
Signal Pins Resistor Values					
f_min			100	kHz	Minimum frequency when optocoupler is cut-off. Only change this variable based on actual bench measurements
Dead Time			320	ns	Dead time
Burst Mode	**1**		**1**		Select Burst Mode: 1, 2, and 3 have hysteresis and have different frequency thresholds
f_max			847	kHz	Max internal clock frequency, dependent on dead-time setting. Is also start-up frequency
f_burst_start			382.4	kHz	Lower threshold frequency of burst mode, provides hysteresis. This is switching frequency at restart after a bursting off-period
f_burst_stop			437.0	kHz	Upper threshold frequency of burst mode; This is switching frequency at which a bursting off-period stops
DT/BF pin upper divider resistor			6.79	k-ohms	Resistor from DT/BF pin to VREF pin
DT/BF pin lower divider resistor			129.1	k-ohms	Resistor from DT/BF pin to G pin
Rstart			5.79	k-ohms	Start-up resistor - resistor in series with soft-start capacitor; equivalent resistance from FB to VREF pins at startup. Use default value unless additional start-up delay is desired.
Start up delay			0.0	ms	Start-up delay; delay before switching begins. Reduce R_START to increase delay
Rfmin			78.3	k-ohms	Resistor from VREF pin to FB pin, to set min operating frequency; This resistor plus Rstart determine f_MIN. Includes 7% HiperLCS frequency tolerance to ensure f_min is below f_brownout
C_softstart			0.33	uF	Softstart capacitor. Recommended values are between 0.1 uF and 0.47 uF

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Ropto			1.2	k-ohms	Resistor in series with opto emitter
OV/UV pin lower resistor	20.00		20.0	k-ohm	Lower resistor in OV/UV pin divider
OV/UV pin upper resistor			3.45	M-ohm	Total upper resistance in OV/UV pin divider
LLC Capacitive Divider Current Sense Circuit					
Slow current limit	3.00		3.00	A	8-cycle current limit - check positive half-cycles during brownout and startup
Fast current limit			5.40	A	1-cycle current limit - check positive half-cycles during startup
LLC sense capacitor			47	pF	HV sense capacitor, forms current divider with main resonant capacitor
RLLC sense resistor			42.7	ohms	LLC current sense resistor, senses current in sense capacitor
IS pin current limit resistor			220	ohms	Limits current from sense resistor into IS pin when voltage on sense R is < -0.5V
IS pin noise filter capacitor			1.0	nF	IS pin bypass capacitor; forms a pole with IS pin current limit capacitor
IS pin noise filter pole frequency			724	kHz	This pole attenuates IS pin signal
Loss Budget					
LCS device Conduction loss			1.5	W	Conduction loss at nominal line and full load
Output diode Loss			1.9	W	Estimated diode losses
Transformer estimated total copper loss			0.34	W	Total copper loss in transformer (primary + secondary)
Transformer estimated total core loss			1.5	W	Estimated core loss
Total transformer losses			1.9	W	Total transformer losses
Total estimated losses			5.3	W	Total losses in LLC stage
Estimated Efficiency			96%	%	Estimated efficiency
PIN			132	W	LLC input power
Secondary Turns and Voltage Centering Calculator					**This is to help you choose the secondary turns - Outputs not connected to any other part of spreadsheet**
V1			46.00	V	Target regulated output voltage Vo1. Change to see effect on slave output
V1d1			0.70	V	Diode drop voltage for Vo1
N1			9.00		Total number of turns for Vo1
V1_Actaul			46.00	V	Expected output
V2			0.00	V	Target output voltage Vo2
V2d2			0.70	V	Diode drop voltage for Vo2
N2			1.00		Total number of turns for Vo2
V2_Actual			4.49	V	Expected output voltage
Separate Series Inductor (For Non-Integrated Transformer Only)					**Not applicable if using integrated magnetics - not connected to any other part of spreadsheet**
Lsep			124.00	uH	Desired inductance of separate inductor
Ae_Ind			0.53	cm^2	Inductor core cross-sectional area
Inductor turns			24		Number of primary turns
BP_fnom			152	mT	AC flux for core loss calculations (at f_predicted and full load)
Expected peak primary current			3.0	A	Expected peak primary current
BP_fmin			295	mT	Peak flux density, calculated at minimum frequency fmin
Inductor Litz gauge			41	AWG	Individual wire strand gauge used for primary winding
Equivalent Inductor Metric Wire gauge			0.070	mm	Equivalent diameter of wire in metric units
Inductor litz strands			125		Number of strands used in Litz wire
Inductor parallel wires			1		Number of parallel individual wires to make up Litz wire
Resistivity_25 C_Sep_Ind			37.6	m-ohm/m	Resistivity in milli-ohms per meter
Inductor MLT			7.00	cm	Mean length per turn

Inductor DCR 25 C			63.2	m-ohm	Estimated resistance at 25 C (for reference)
Inductor DCR 100 C			84.7	m-ohm	Estimated resistance at 100 C (approximately 33% higher than at 25 C)
ACR_Sep_Inductor			135.5	m-ohm	Measured AC resistance (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature
Inductor copper loss			0.14	W	Total primary winding copper loss at 85 C
Feedback section					
VMAIN	**Auto**		46.00		Output voltage rail that optocoupler LED is connected to
ITL431_BIAS			1	mA	Minimum operating current in TL431 cathode
VF			1	V	Typical Optocoupler LED forward voltage at IOPTO_BJTMAX (max current)
VCE_SAT			0.3	V	Optocoupler transistor saturation voltage
CTR_MIN			0.8		Optocoupler minimum CTR at VCE_SAT and at IOPTO_BJT_MAX
VTL431_SAT			2.5	V	TL431 minimum cathode voltage when saturated
RLED_SHUNT			1	k-ohms	Resistor across optocoupler LED to ensure minimum TL431 bias current is met
ROPTO_LOAD			4.70	k-ohms	Resistor from optocoupler emitter to ground, sets load current
IFMAX			347.08	uA	FB pin current when switching at FMAX (e.g. startup)
IOPTO_BJT_MAX			0.97	mA	Optocoupler transistor maximum current - when bursting at FMAX (e.g. startup)
RLED_SERIES_MAX			17.29	k-ohms	Maximum value of gain setting resistor, in series with optocoupler LED, to ensure optocoupler can deliver IOPTO_BJT_MAX. Includes -10% tolerance factor.

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11.4 *Maximum Output Voltage / Output Power (54 V) Spreadsheet*

HiperLCS_042413; Rev.1.3; Copyright Power Integrations 2013	**INPUTS**	**INFO**	**OUTPUTS**	**UNITS**	**HiperLCS_042413_Rev1-3.xls; HiperLCS Half-Bridge, Continuous mode LLC Resonant Converter Design Spreadsheet**
Enter Input Parameters					
Vbulk_nom	440		440	V	Nominal LLC input voltage
Vbrownout	330		330	V	Brownout threshold voltage. HiperLCS will shut down if voltage drops below this value. Allowable value is between 65% and 76% of Vbulk_nom. Set to 65% for max holdup time
Vbrownin			416	V	Startup threshold on bulk capacitor
VOV_shut		Warning	548	V	!!! Warning. OV shutdown voltage is too high. Reduce Vbulk_nom OR Vbrownout
VOV_restart			528	V	Restart voltage after OV protection.
CBULK	68.00		68	uF	Minimum value of bulk cap to meet holdup time requirement; Adjust holdup time and Vbrownout to change bulk cap value
tHOLDUP			18.7	ms	Bulk capacitor hold up time
Enter LLC (secondary) outputs					**The spreadsheet assumes AC stacking of the secondaries**
VO1	54.00		54.00	V	Main Output Voltage. Spreadsheet assumes that this is the regulated output
IO1	2.75		2.75	A	Main output maximum current
VD1	0.70		0.70	V	Forward voltage of diode in Main output
PO1			149	W	Output Power from first LLC output
VO2			0.00	V	Second Output Voltage
IO2			0.00	A	Second output current
VD2			0.70	V	Forward voltage of diode used in second output
PO2			0.00	W	Output Power from second LLC output
P_LLC			149	W	Specified LLC output power
LCS Device Selection					
Device	**LCS702**		**LCS702**		**LCS Device**
RDS-ON (MAX)			1.39	ohms	RDS-ON (max) of selected device
Coss			250	pF	Equivalent Coss of selected device
Cpri			40	pF	Stray Capacitance at transformer primary
Pcond_loss			1.9	W	Conduction loss at nominal line and full load
Tmax-hs			90	deg C	Maximum heatsink temperature
Theta J-HS			9.1	deg C/W	Thermal resistance junction to heatsink (with grease and no insulator)
Expected Junction temperature			107	deg C	Expectd Junction temperature
Ta max			50	deg C	Expected max ambient temperature
Theta HS-A			21	deg C/W	Required thermal resistance heatsink to ambient
LLC Resonant Parameter and Transformer Calculations (generates red curve)					
Vres_target	450.00		450	V	Desired Input voltage at which power train operates at resonance. If greater than Vbulk_nom, LLC operates below resonance at VBULK.
Po			150	W	LLC output power including diode loss
Vo			54.70	V	Main Output voltage (includes diode drop) for calculating Nsec and turns ratio
f_target	120.00		120	kHz	Desired switching frequency at Vbulk_nom. 66 kHz to 300 kHz, recommended 180-250 kHz
Lpar			366	uH	Parallel inductance. (Lpar = Lopen - Lres for integrated transformer; Lpar = Lmag for non-integrated low-leakage transformer)
Lpri	490.00		490	uH	Primary open circuit inductance for integrated transformer; for low-leakage transformer it is sum of primary inductance and series inductor. If left blank, auto-calculation shows value necessary for slight loss of ZVS at ~80% of Vnom

	124.00		124.0	uH	Series inductance or primary leakage inductance of integrated transformer; if left blank auto-calculation is for K=4
Kratio			3.0		Ratio of Lpar to Lres. Maintain value of K such that 2.1 < K < 11. Preferred Lres is such that K<7.
Cres	12.00		12.0	nF	Series resonant capacitor. Red background cells produce red graph. If Lpar, Lres, Cres, and n_RATIO_red_graph are left blank, they will be auto-calculated
Lsec	16.300		16.300	uH	Secondary side inductance of one phase of main output; measure and enter value, or adjust value until f_predicted matches what is measured ;
15			41	%	Leakage distribution factor (primary to secondary). >50% signifies most of the leakage is in primary side. Gap physically under secondary yields >50%, requiring fewer primary turns.
n_eq			4.74		Turns ratio of LLC equivalent circuit ideal transformer
Npri	45.0		45.0		Primary number of turns; if input is blank, default value is auto-calculation so that f_predicted = f_target and m=50%
Nsec	8.0		8.0		Secondary number of turns (each phase of Main output). Default value is estimate to maintain BAC<=200 mT, using selected core (below)
f_predicted			109	kHz	Expected frequency at nominal input voltage and full load; Heavily influenced by n_eq and primary turns
f_res			130	kHz	Series resonant frequency (defined by series inductance Lres and C)
f_brownout			92	kHz	Expected switching frequency at Vbrownout, full load. Set HiperLCS minimum frequency to this value.
f_par			66	kHz	Parallel resonant frequency (defined by Lpar + Lres and C)
f_inversion			78	kHz	LLC full load gain inversion frequency. Operation below this frequency results in operation in gain inversion region.
Vinversion			217	V	LLC full load gain inversion point input voltage
Vres_expected		Warning	518	V	!!! Warning Expected value of VRES is more than 3% away from target value. Adjust Npri, Lsec, or Lpri to fix this problem
RMS Currents and Voltages					
IRMS_LLC_Primary			1.17	A	Primary winding RMS current at full load, Vbulk_nom and f_predicted
Winding 1 (Lower secondary Voltage) RMS current			2.2	A	Winding 1 (Lower secondary Voltage) RMS current
Lower Secondary Voltage Capacitor RMS current			1.5	A	Lower Secondary Voltage Capacitor RMS current
Winding 2 (Higher secondary Voltage) RMS current			0.0	A	Winding 2 (Higher secondary Voltage) RMS current
Higher Secondary Voltage Capacitor RMS current			0.0	A	Higher Secondary Voltage Capacitor RMS current
Cres_Vrms			141	V	Resonant capacitor AC RMS Voltage at full load and nominal input voltage
Virtual Transformer Trial - (generates blue curve)					
New primary turns			45.0		Trial transformer primary turns; default value is from resonant section
New secondary turns			8.0		Trial transformer secondary turns; default value is from resonant section
New Lpri			490	uH	Trial transformer open circuit inductance; default value is from resonant section
New Cres			12.0	nF	Trial value of series capacitor (if left blank calculated value chosen so f_res same as in main resonant

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					section above
New estimated Lres			124.0	uH	Trial transformer estimated Lres
New estimated Lpar			366	uH	Estimated value of Lpar for trial transformer
New estimated Lsec			16.300	uH	Estimated value of secondary leakage inductance
New Kratio			3.0		Ratio of Lpar to Lres for trial transformer
New equivalent circuit transformer turns ratio			4.74		Estimated effective transformer turns ratio
V powertrain inversion new			217	V	Input voltage at LLC full load gain inversion point
f_res_trial			130	kHz	New Series resonant frequency
f_predicted_trial			109	kHz	New nominal operating frequency
IRMS_LLC_Primary			1.17	A	Primary winding RMS current at full load and nominal input voltage (Vbulk) and f_predicted_trial
Winding 1 (Lower secondary Voltage) RMS current			2.2	A	RMS current through Output 1 winding, assuming half sinusoidal waveshape
Lower Secondary Voltage Capacitor RMS current			1.4	A	Lower Secondary Voltage Capacitor RMS current
Winding 2 (Higher secondary Voltage) RMS current			2.2	A	RMS current through Output 2 winding; Output 1 winding is AC stacked on top of Output 2 winding
Higher Secondary Voltage Capacitor RMS current			0.0	A	Higher Secondary Voltage Capacitor RMS current
Vres_expected_trial		Warning	518	V	!!! Warning. Vres_expected_trial is more than 3% away from target value. Adjust New Primary turns or New Lpri to fix this problem
Transformer Core Calculations (Calculates From Resonant Parameter Section)					
Transformer Core	**EER28L**		**EER28L**		**Transformer Core**
Ae	0.97		0.97	cm^2	Enter transformer core cross-sectional area
Ve	7.64		7.64	cm^3	Enter the volume of core
Aw	123.00		123.0	mm^2	Area of window
Bw	20.90		20.9	mm	Total Width of Bobbin
Loss density			200.0	mW/cm^3	Enter the loss per unit volume at the switching frequency and BAC (Units same as kW/m^3)
MLT			4.0	cm	Mean length per turn
Nchambers			2		Number of Bobbin chambers
Wsep			3.0	mm	Winding separator distance (will result in loss of winding area)
Ploss			1.5	W	Estimated core loss
Bpkfmin			192	mT	First Quadrant peak flux density at minimum frequency.
BAC			322	mT	AC peak to peak flux density (calculated at f_predicted, Vbulk at full load)
Primary Winding					
Npri			45.0		Number of primary turns; determined in LLC resonant section
Primary gauge	42		42	AWG	Individual wire strand gauge used for primary winding
Equivalent Primary Metric Wire gauge			0.060	mm	Equivalent diameter of wire in metric units
Primary litz strands	100		100		Number of strands in Litz wire; for non-litz primary winding, set to 1
Primary Winding Allocation Factor			50	%	Primary window allocation factor - percentage of winding space allocated to primary
AW_P			53	mm^2	Winding window area for primary
Fill Factor			40%	%	% Fill factor for primary winding (typical max fill is 60%)
Resistivity_25 C_Primary			59.29	m-ohm/m	Resistivity in milli-ohms per meter
Primary DCR 25 C			105.45	m-ohm	Estimated resistance at 25 C
Primary DCR 100 C			141.30	m-ohm	Estimated resistance at 100 C (approximately 33% higher than at 25 C)
Primary RMS current			1.17	A	Measured RMS current through the primary winding
ACR_Trf_Primary			205.55	m-ohm	Measured AC resistance (at 100 kHz, room

					temperature), multiply by 1.33 to approximate 100 C winding temperature
Primary copper loss			0.28	W	Total primary winding copper loss at 85 C
Primary Layers			3.91		Number of layers in primary Winding
Secondary Winding 1 (Lower secondary voltage OR Single output)					**Note - Power loss calculations are for each winding half of secondary**
Output Voltage			54.00	V	Output Voltage (assumes AC stacked windings)
Sec 1 Turns			8.00		Secondary winding turns (each phase)
Sec 1 RMS current (total, AC+DC)			2.2	A	RMS current through Output 1 winding, assuming half sinusoidal waveshape
Winding current (DC component)			1.38	A	DC component of winding current
Winding current (AC RMS component)			1.74	A	AC component of winding current
Sec 1 Wire gauge	40		40	AWG	Individual wire strand gauge used for secondary winding
Equivalent secondary 1 Metric Wire gauge			0.080	mm	Equivalent diameter of wire in metric units
Sec 1 litz strands	350		350		Number of strands used in Litz wire; for non-litz non-integrated transformer set to 1
Resistivity_25 C_sec1			10.65	m-ohm/m	Resistivity in milli-ohms per meter
DCR_25C_Sec1			3.37	m-ohm	Estimated resistance per phase at 25 C (for reference)
DCR_100C_Sec1			4.51	m-ohm	Estimated resistance per phase at 100 C (approximately 33% higher than at 25 C)
DCR_Ploss_Sec1			0.07	W	Estimated Power loss due to DC resistance (both secondary phases)
ACR_Sec1			4.72	m-ohm	Measured AC resistance per phase (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature. Default value of ACR is twice the DCR value at 100 C
ACR_Ploss_Sec1			0.03	W	Estimated AC copper loss (both secondary phases)
Total winding 1 Copper Losses			0.10	W	Total (AC + DC) winding copper loss for both secondary phases
Capacitor RMS current			1.5	A	Output capacitor RMS current
Co1			2.4	uF	Secondary 1 output capacitor
Capacitor ripple voltage			3.0	%	Peak to Peak ripple voltage on secondary 1 output capacitor
Output rectifier RMS Current			2.2	A	Schottky losses are a stronger function of load DC current. Sync Rectifier losses are a function of RMS current
Secondary 1 Layers			1.73		Number of layers in secondary 1 Winding
Secondary Winding 2 (Higher secondary voltage)					**Note - Power loss calculations are for each winding half of secondary**
Output Voltage			0.00	V	Output Voltage (assumes AC stacked windings)
Sec 2 Turns			0.00		Secondary winding turns (each phase) AC stacked on top of secondary winding 1
Sec 2 RMS current (total, AC+DC)			2.2	A	RMS current through Output 2 winding; Output 1 winding is AC stacked on top of Output 2 winding
Winding current (DC component)			0.0	A	DC component of winding current
Winding current (AC RMS component)			0.0	A	AC component of winding current
Sec 2 Wire gauge			40	AWG	Individual wire strand gauge used for secondary winding
Equivalent secondary 2 Metric Wire gauge			0.080	mm	Equivalent diameter of wire in metric units
Sec 2 litz strands			0		Number of strands used in Litz wire; for non-litz non-integrated transformer set to 1
Resistivity_25 C_sec2			37290.65	m-ohm/m	Resistivity in milli-ohms per meter
Transformer Secondary MLT			3.95	cm	Mean length per turn

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DCR_25C_Sec2			0.00	m-ohm	Estimated resistance per phase at 25 C (for reference)
DCR_100C_Sec2			0.00	m-ohm	Estimated resistance per phase at 100 C (approximately 33% higher than at 25 C)
DCR_Ploss_Sec1			0.00	W	Estimated Power loss due to DC resistance (both secondary halves)
ACR_Sec2			0.00	m-ohm	Measured AC resistance per phase (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature. Default value of ACR is twice the DCR value at 100 C
ACR_Ploss_Sec2			0.00	W	Estimated AC copper loss (both secondary halves)
Total winding 2 Copper Losses			0.00	W	Total (AC + DC) winding copper loss for both secondary halves
Capacitor RMS current			0.0	A	Output capacitor RMS current
Co2			N/A	uF	Secondary 2 output capacitor
Capacitor ripple voltage			N/A	%	Peak to Peak ripple voltage on secondary 1 output capacitor
Output rectifier RMS Current			0.0	A	Schottky losses are a stronger function of load DC current. Sync Rectifier losses are a function of RMS current
Secondary 2 Layers			1.00		Number of layers in secondary 2 Winding
Transformer Loss Calculations					**Does not include fringing flux loss from gap**
Primary copper loss (from Primary section)			0.28	W	Total primary winding copper loss at 85 C
Secondary copper Loss			0.10	W	Total copper loss in secondary winding
Transformer total copper loss			0.38	W	Total copper loss in transformer (primary + secondary)
AW_S			52.67	mm^2	Area of window for secondary winding
Secondary Fill Factor			89%	%	% Fill factor for secondary windings; typical max fill is 60% for served and 75% for unserved Litz
Signal Pins Resistor Values					
f_min			92	kHz	Minimum frequency when optocoupler is cut-off. Only change this variable based on actual bench measurements
Dead Time			320	ns	Dead time
Burst Mode	**1**		**1**		Select Burst Mode: 1, 2, and 3 have hysteresis and have different frequency thresholds
f_max			847	kHz	Max internal clock frequency, dependent on dead-time setting. Is also start-up frequency
f_burst_start			382.4	kHz	Lower threshold frequency of burst mode, provides hysteresis. This is switching frequency at restart after a bursting off-period
f_burst_stop			437.0	kHz	Upper threshold frequency of burst mode; This is switching frequency at which a bursting off-period stops
DT/BF pin upper divider resistor			6.79	k-ohms	Resistor from DT/BF pin to VREF pin
DT/BF pin lower divider resistor			129.1	k-ohms	Resistor from DT/BF pin to G pin
Rstart			5.79	k-ohms	Start-up resistor - resistor in series with soft-start capacitor; equivalent resistance from FB to VREF pins at startup. Use default value unless additional start-up delay is desired.
Start up delay			0.0	ms	Start-up delay; delay before switching begins. Reduce R_START to increase delay
Rfmin			86.0	k-ohms	Resistor from VREF pin to FB pin, to set min operating frequency; This resistor plus Rstart determine f_MIN. Includes 7% HiperLCS frequency tolerance to ensure f_min is below f_brownout
C_softstart			0.33	uF	Softstart capacitor. Recommended values are between 0.1 uF and 0.47 uF
Ropto			1.2	k-ohms	Resistor in series with opto emitter

OV/UV pin lower resistor	20.00		20.0	k-ohm	Lower resistor in OV/UV pin divider
OV/UV pin upper resistor			3.45	M-ohm	Total upper resistance in OV/UV pin divider
LLC Capacitive Divider Current Sense Circuit					
Slow current limit	3.00		3.00	A	8-cycle current limit - check positive half-cycles during brownout and startup
Fast current limit			5.40	A	1-cycle current limit - check positive half-cycles during startup
LLC sense capacitor			47	pF	HV sense capacitor, forms current divider with main resonant capacitor
RLLC sense resistor			42.7	ohms	LLC current sense resistor, senses current in sense capacitor
IS pin current limit resistor			220	ohms	Limits current from sense resistor into IS pin when voltage on sense R is < -0.5V
IS pin noise filter capacitor			1.0	nF	IS pin bypass capacitor; forms a pole with IS pin current limit capacitor
IS pin noise filter pole frequency			724	kHz	This pole attenuates IS pin signal
Loss Budget					
LCS device Conduction loss			1.9	W	Conduction loss at nominal line and full load
Output diode Loss			1.9	W	Estimated diode losses
Transformer estimated total copper loss			0.38	W	Total copper loss in transformer (primary + secondary)
Transformer estimated total core loss			1.5	W	Estimated core loss
Total transformer losses			1.9	W	Total transformer losses
Total estimated losses			5.7	W	Total losses in LLC stage
Estimated Efficiency			96%	%	Estimated efficiency
PIN			154	W	LLC input power
Secondary Turns and Voltage Centering Calculator					**This is to help you choose the secondary turns - Outputs not connected to any other part of spreadsheet**
V1			54.00	V	Target regulated output voltage Vo1. Change to see effect on slave output
V1d1			0.70	V	Diode drop voltage for Vo1
N1			9.00		Total number of turns for Vo1
V1_Actaul			54.00	V	Expected output
V2			0.00	V	Target output voltage Vo2
V2d2			0.70	V	Diode drop voltage for Vo2
N2			1.00		Total number of turns for Vo2
V2_Actual			5.38	V	Expected output voltage
Separate Series Inductor (For Non-Integrated Transformer Only)					**Not applicable if using integrated magnetics - not connected to any other part of spreadsheet**
Lsep			124.00	uH	Desired inductance of separate inductor
Ae_Ind			0.53	cm^2	Inductor core cross-sectional area
Inductor turns			24		Number of primary turns
BP_fnom			172	mT	AC flux for core loss calculations (at f_predicted and full load)
Expected peak primary current			3.0	A	Expected peak primary current
BP_fmin			295	mT	Peak flux density, calculated at minimum frequency fmin
Inductor Litz gauge			41	AWG	Individual wire strand gauge used for primary winding
Equivalent Inductor Metric Wire gauge			0.070	mm	Equivalent diameter of wire in metric units
Inductor litz strands			125		Number of strands used in Litz wire
Inductor parallel wires			1		Number of parallel individual wires to make up Litz wire
Resistivity_25 C_Sep_Ind			37.6	m-ohm/m	Resistivity in milli-ohms per meter
Inductor MLT			7.00	cm	Mean length per turn
Inductor DCR 25 C			63.2	m-ohm	Estimated resistance at 25 C (for reference)

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Inductor DCR 100 C			84.7	m-ohm	Estimated resistance at 100 C (approximately 33% higher than at 25 C)
ACR_Sep_Inductor			135.5	m-ohm	Measured AC resistance (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature
Inductor copper loss			0.18	W	Total primary winding copper loss at 85 C
Feedback section					
VMAIN	**Auto**		54.00		Output voltage rail that optocoupler LED is connected to
ITL431_BIAS			1	mA	Minimum operating current in TL431 cathode
VF			1	V	Typical Optocoupler LED forward voltage at IOPTO_BJTMAX (max current)
VCE_SAT			0.3	V	Optocoupler transistor saturation voltage
CTR_MIN			0.8		Optocoupler minimum CTR at VCE_SAT and at IOPTO_BJT_MAX
VTL431_SAT			2.5	V	TL431 minimum cathode voltage when saturated
RLED_SHUNT			1	k-ohms	Resistor across optocoupler LED to ensure minimum TL431 bias current is met
ROPTO_LOAD			4.70	k-ohms	Resistor from optocoupler emitter to ground, sets load current
IFMAX			347.08	uA	FB pin current when switching at FMAX (e.g. startup)
IOPTO_BJT_MAX			0.97	mA	Optocoupler transistor maximum current - when bursting at FMAX (e.g. startup)
RLED_SERIES_MAX			20.53	k-ohms	Maximum value of gain setting resistor, in series with optocoupler LED, to ensure optocoupler can deliver IOPTO_BJT_MAX. Includes -10% tolerance factor.

11.5 *Minimum Output Voltage / Power (39 V) Spreadsheet*

HiperLCS_042413; Rev.1.3; Copyright Power Integrations 2013	INPUTS	INFO	OUTPUTS	UNITS	HiperLCS_042413_Rev1-3.xls; HiperLCS Half-Bridge, Continuous mode LLC Resonant Converter Design Spreadsheet
Enter Input Parameters					
Vbulk_nom	440		440	V	Nominal LLC input voltage
Vbrownout	330		330	V	Brownout threshold voltage. HiperLCS will shut down if voltage drops below this value. Allowable value is between 65% and 76% of Vbulk_nom. Set to 65% for max holdup time
Vbrownin			416	V	Startup threshold on bulk capacitor
VOV_shut		Warning	548	V	!!! Warning. OV shutdown voltage is too high. Reduce Vbulk_nom OR Vbrownout
VOV_restart			528	V	Restart voltage after OV protection.
CBULK	68.00		68	uF	Minimum value of bulk cap to meet holdup time requirement; Adjust holdup time and Vbrownout to change bulk cap value
tHOLDUP			25.7	ms	Bulk capacitor hold up time
Enter LLC (secondary) outputs					**The spreadsheet assumes AC stacking of the secondaries**
VO1	39.00		39.00	V	Main Output Voltage. Spreadsheet assumes that this is the regulated output
IO1	2.75		2.75	A	Main output maximum current
VD1	0.70		0.70	V	Forward voltage of diode in Main output
PO1			107	W	Output Power from first LLC output
VO2			0.00	V	Second Output Voltage
IO2			0.00	A	Second output current
VD2			0.70	V	Forward voltage of diode used in second output
PO2			0.00	W	Output Power from second LLC output
P_LLC			107	W	Specified LLC output power
LCS Device Selection					
Device	**LCS702**	**Warning**	**LCS702**		**!!! Warning. Device may be too large. Select smaller device**
RDS-ON (MAX)			1.39	ohms	RDS-ON (max) of selected device
Coss			250	pF	Equivalent Coss of selected device
Cpri			40	pF	Stray Capacitance at transformer primary
Pcond_loss			1.1	W	Conduction loss at nominal line and full load
Tmax-hs			90	deg C	Maximum heatsink temperature
Theta J-HS			9.1	deg C/W	Thermal resistance junction to heatsink (with grease and no insulator)
Expected Junction temperature			100	deg C	Expectd Junction temperature
Ta max			50	deg C	Expected max ambient temperature
Theta HS-A			37	deg C/W	Required thermal resistance heatsink to ambient
LLC Resonant Parameter and Transformer Calculations (generates red curve)					
Vres_target	450.00		450	V	Desired Input voltage at which power train operates at resonance. If greater than Vbulk_nom, LLC operates below resonance at VBULK.
Po			109	W	LLC output power including diode loss
Vo			39.70	V	Main Output voltage (includes diode drop) for calculating Nsec and turns ratio
f_target	120.00		120	kHz	Desired switching frequency at Vbulk_nom. 66 kHz to 300 kHz, recommended 180-250 kHz
Lpar			366	uH	Parallel inductance. (Lpar = Lopen - Lres for integrated transformer; Lpar = Lmag for non-integrated low-leakage transformer)
Lpri	490.00		490	uH	Primary open circuit inductance for integrated transformer; for low-leakage transformer it is sum of primary inductance and series inductor. If left blank, auto-calculation shows value necessary for

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					slight loss of ZVS at ~80% of Vnom
	124.00		124.0	uH	Series inductance or primary leakage inductance of integrated transformer; if left blank auto-calculation is for K=4
Kratio			3.0		Ratio of Lpar to Lres. Maintain value of K such that 2.1 < K < 11. Preferred Lres is such that K<7.
Cres	12.00		12.0	nF	Series resonant capacitor. Red background cells produce red graph. If Lpar, Lres, Cres, and n_RATIO_red_graph are left blank, they will be auto-calculated
Lsec	16.300		16.300	uH	Secondary side inductance of one phase of main output; measure and enter value, or adjust value until f_predicted matches what is measured ;
15			41	%	Leakage distribution factor (primary to secondary). >50% signifies most of the leakage is in primary side. Gap physically under secondary yields >50%, requiring fewer primary turns.
n_eq			4.74		Turns ratio of LLC equivalent circuit ideal transformer
Npri	45.0		45.0		Primary number of turns; if input is blank, default value is auto-calculation so that f_predicted = f_target and m=50%
Nsec	8.0		8.0		Secondary number of turns (each phase of Main output). Default value is estimate to maintain BAC<=200 mT, using selected core (below)
f_predicted			152	kHz	Expected frequency at nominal input voltage and full load; Heavily influenced by n_eq and primary turns
f_res			130	kHz	Series resonant frequency (defined by series inductance Lres and C)
f_brownout			112	kHz	Expected switching frequency at Vbrownout, full load. Set HiperLCS minimum frequency to this value.
f_par			66	kHz	Parallel resonant frequency (defined by Lpar + Lres and C)
f_inversion			81	kHz	LLC full load gain inversion frequency. Operation below this frequency results in operation in gain inversion region.
Vinversion			184	V	LLC full load gain inversion point input voltage
Vres_expected		Warning	376	V	!!! Warning Expected value of VRES is more than 3% away from target value. Adjust Npri, Lsec, or Lpri to fix this problem
RMS Currents and Voltages					
IRMS_LLC_Primary			0.89	A	Primary winding RMS current at full load, Vbulk_nom and f_predicted
Winding 1 (Lower secondary Voltage) RMS current			2.2	A	Winding 1 (Lower secondary Voltage) RMS current
Lower Secondary Voltage Capacitor RMS current			1.4	A	Lower Secondary Voltage Capacitor RMS current
Winding 2 (Higher secondary Voltage) RMS current			0.0	A	Winding 2 (Higher secondary Voltage) RMS current
Higher Secondary Voltage Capacitor RMS current			0.0	A	Higher Secondary Voltage Capacitor RMS current
Cres_Vrms			77	V	Resonant capacitor AC RMS Voltage at full load and nominal input voltage
Virtual Transformer Trial - (generates blue curve)					
New primary turns			45.0		Trial transformer primary turns; default value is from resonant section
New secondary turns			8.0		Trial transformer secondary turns; default value is from resonant section
New Lpri			490	uH	Trial transformer open circuit inductance; default

					value is from resonant section
New Cres			12.0	nF	Trial value of series capacitor (if left blank calculated value chosen so f_res same as in main resonant section above
New estimated Lres			124.0	uH	Trial transformer estimated Lres
New estimated Lpar			366	uH	Estimated value of Lpar for trial transformer
New estimated Lsec			16.300	uH	Estimated value of secondary leakage inductance
New Kratio			3.0		Ratio of Lpar to Lres for trial transformer
New equivalent circuit transformer turns ratio			4.74		Estimated effective transformer turns ratio
V powertrain inversion new			184	V	Input voltage at LLC full load gain inversion point
f_res_trial			130	kHz	New Series resonant frequency
f_predicted_trial			152	kHz	New nominal operating frequency
IRMS_LLC_Primary			0.89	A	Primary winding RMS current at full load and nominal input voltage (Vbulk) and f_predicted_trial
Winding 1 (Lower secondary Voltage) RMS current			2.4	A	RMS current through Output 1 winding, assuming half sinusoidal waveshape
Lower Secondary Voltage Capacitor RMS current			1.9	A	Lower Secondary Voltage Capacitor RMS current
Winding 2 (Higher secondary Voltage) RMS current			2.4	A	RMS current through Output 2 winding; Output 1 winding is AC stacked on top of Output 2 winding
Higher Secondary Voltage Capacitor RMS current			0.0	A	Higher Secondary Voltage Capacitor RMS current
Vres_expected_trial		Warning	376	V	!!! Warning. Vres_expected_trial is more than 3% away from target value. Adjust New Primary turns or New Lpri to fix this problem
Transformer Core Calculations (Calculates From Resonant Parameter Section)					
Transformer Core	**EER28L**		**EER28L**		**Transformer Core**
Ae	0.97		0.97	cm^2	Enter transformer core cross-sectional area
Ve	7.64		7.64	cm^3	Enter the volume of core
Aw	123.00		123.0	mm^2	Area of window
Bw	20.90		20.9	mm	Total Width of Bobbin
Loss density			200.0	mW/cm^3	Enter the loss per unit volume at the switching frequency and BAC (Units same as kW/m^3)
MLT			4.0	cm	Mean length per turn
Nchambers			2		Number of Bobbin chambers
Wsep			3.0	mm	Winding separator distance (will result in loss of winding area)
Ploss			1.5	W	Estimated core loss
Bpkfmin			114	mT	First Quadrant peak flux density at minimum frequency.
BAC			168	mT	AC peak to peak flux density (calculated at f_predicted, Vbulk at full load)
Primary Winding					
Npri			45.0		Number of primary turns; determined in LLC resonant section
Primary gauge	42		42	AWG	Individual wire strand gauge used for primary winding
Equivalent Primary Metric Wire gauge			0.060	mm	Equivalent diameter of wire in metric units
Primary litz strands	100		100		Number of strands in Litz wire; for non-litz primary winding, set to 1
Primary Winding Allocation Factor			50	%	Primary window allocation factor - percentage of winding space allocated to primary
AW_P			53	mm^2	Winding window area for primary
Fill Factor			40%	%	% Fill factor for primary winding (typical max fill is 60%)
Resistivity_25 C_Primary			59.29	m-ohm/m	Resistivity in milli-ohms per meter
Primary DCR 25 C			105.45	m-ohm	Estimated resistance at 25 C

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Primary DCR 100 C			141.30	m-ohm	Estimated resistance at 100 C (approximately 33% higher than at 25 C)
Primary RMS current			0.89	A	Measured RMS current through the primary winding
ACR_Trf_Primary			265.66	m-ohm	Measured AC resistance (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature
Primary copper loss			0.21	W	Total primary winding copper loss at 85 C
Primary Layers			3.91		Number of layers in primary Winding
Secondary Winding 1 (Lower secondary voltage OR Single output)					**Note - Power loss calculations are for each winding half of secondary**
Output Voltage			39.00	V	Output Voltage (assumes AC stacked windings)
Sec 1 Turns			8.00		Secondary winding turns (each phase)
Sec 1 RMS current (total, AC+DC)			2.2	A	RMS current through Output 1 winding, assuming half sinusoidal waveshape
Winding current (DC component)			1.38	A	DC component of winding current
Winding current (AC RMS component)			1.69	A	AC component of winding current
Sec 1 Wire gauge	40		40	AWG	Individual wire strand gauge used for secondary winding
Equivalent secondary 1 Metric Wire gauge			0.080	mm	Equivalent diameter of wire in metric units
Sec 1 litz strands	350		350		Number of strands used in Litz wire; for non-litz non-integrated transformer set to 1
Resistivity_25 C_sec1			10.65	m-ohm/m	Resistivity in milli-ohms per meter
DCR_25C_Sec1			3.37	m-ohm	Estimated resistance per phase at 25 C (for reference)
DCR_100C_Sec1			4.51	m-ohm	Estimated resistance per phase at 100 C (approximately 33% higher than at 25 C)
DCR_Ploss_Sec1			0.07	W	Estimated Power loss due to DC resistance (both secondary phases)
ACR_Sec1			4.91	m-ohm	Measured AC resistance per phase (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature. Default value of ACR is twice the DCR value at 100 C
ACR_Ploss_Sec1			0.03	W	Estimated AC copper loss (both secondary phases)
Total winding 1 Copper Losses			0.10	W	Total (AC + DC) winding copper loss for both secondary phases
Capacitor RMS current			1.4	A	Output capacitor RMS current
Co1			2.4	uF	Secondary 1 output capacitor
Capacitor ripple voltage			3.0	%	Peak to Peak ripple voltage on secondary 1 output capacitor
Output rectifier RMS Current			2.2	A	Schottky losses are a stronger function of load DC current. Sync Rectifier losses are a function of RMS current
Secondary 1 Layers			1.73		Number of layers in secondary 1 Winding
Secondary Winding 2 (Higher secondary voltage)					**Note - Power loss calculations are for each winding half of secondary**
Output Voltage			0.00	V	Output Voltage (assumes AC stacked windings)
Sec 2 Turns			0.00		Secondary winding turns (each phase) AC stacked on top of secondary winding 1
Sec 2 RMS current (total, AC+DC)			2.2	A	RMS current through Output 2 winding; Output 1 winding is AC stacked on top of Output 2 winding
Winding current (DC component)			0.0	A	DC component of winding current
Winding current (AC RMS component)			0.0	A	AC component of winding current
Sec 2 Wire gauge			40	AWG	Individual wire strand gauge used for secondary winding
Equivalent secondary 2 Metric Wire gauge			0.080	mm	Equivalent diameter of wire in metric units
Sec 2 litz strands			0		Number of strands used in Litz wire; for non-litz

					non-integrated transformer set to 1
Resistivity_25 C_sec2			37290.65	m-ohm/m	Resistivity in milli-ohms per meter
Transformer Secondary MLT			3.95	cm	Mean length per turn
DCR_25C_Sec2			0.00	m-ohm	Estimated resistance per phase at 25 C (for reference)
DCR_100C_Sec2			0.00	m-ohm	Estimated resistance per phase at 100 C (approximately 33% higher than at 25 C)
DCR_Ploss_Sec1			0.00	W	Estimated Power loss due to DC resistance (both secondary halves)
ACR_Sec2			0.00	m-ohm	Measured AC resistance per phase (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature. Default value of ACR is twice the DCR value at 100 C
ACR_Ploss_Sec2			0.00	W	Estimated AC copper loss (both secondary halves)
Total winding 2 Copper Losses			0.00	W	Total (AC + DC) winding copper loss for both secondary halves
Capacitor RMS current			0.0	A	Output capacitor RMS current
Co2			N/A	uF	Secondary 2 output capacitor
Capacitor ripple voltage			N/A	%	Peak to Peak ripple voltage on secondary 1 output capacitor
Output rectifier RMS Current			0.0	A	Schottky losses are a stronger function of load DC current. Sync Rectifier losses are a function of RMS current
Secondary 2 Layers			1.00		Number of layers in secondary 2 Winding
Transformer Loss Calculations					**Does not include fringing flux loss from gap**
Primary copper loss (from Primary section)			0.21	W	Total primary winding copper loss at 85 C
Secondary copper Loss			0.10	W	Total copper loss in secondary winding
Transformer total copper loss			0.31	W	Total copper loss in transformer (primary + secondary)
AW_S			52.67	mm^2	Area of window for secondary winding
Secondary Fill Factor			89%	%	% Fill factor for secondary windings; typical max fill is 60% for served and 75% for unserved Litz
Signal Pins Resistor Values					
f_min			112	kHz	Minimum frequency when optocoupler is cut-off. Only change this variable based on actual bench measurements
Dead Time			420	ns	Dead time
Burst Mode	**1**		**1**		Select Burst Mode: 1, 2, and 3 have hysteresis and have different frequency thresholds
f_max			645	kHz	Max internal clock frequency, dependent on dead-time setting. Is also start-up frequency
f_burst_start			285.0	kHz	Lower threshold frequency of burst mode, provides hysteresis. This is switching frequency at restart after a bursting off-period
f_burst_stop			325.7	kHz	Upper threshold frequency of burst mode; This is switching frequency at which a bursting off-period stops
DT/BF pin upper divider resistor			9.56	k-ohms	Resistor from DT/BF pin to VREF pin
DT/BF pin lower divider resistor			181.7	k-ohms	Resistor from DT/BF pin to G pin
Rstart			8.21	k-ohms	Start-up resistor - resistor in series with soft-start capacitor; equivalent resistance from FB to VREF pins at startup. Use default value unless additional start-up delay is desired.
Start up delay			0.0	ms	Start-up delay; delay before switching begins. Reduce R_START to increase delay
Rfmin			66.0	k-ohms	Resistor from VREF pin to FB pin, to set min operating frequency; This resistor plus Rstart determine f_MIN. Includes 7% HiperLCS frequency

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					tolerance to ensure f_min is below f_brownout
C_softstart			0.33	uF	Softstart capacitor. Recommended values are between 0.1 uF and 0.47 uF
Ropto			1.6	k-ohms	Resistor in series with opto emitter
OV/UV pin lower resistor	20.00		20.0	k-ohm	Lower resistor in OV/UV pin divider
OV/UV pin upper resistor			3.45	M-ohm	Total upper resistance in OV/UV pin divider
LLC Capacitive Divider Current Sense Circuit					
Slow current limit	3.00		3.00	A	8-cycle current limit - check positive half-cycles during brownout and startup
Fast current limit			5.40	A	1-cycle current limit - check positive half-cycles during startup
LLC sense capacitor			47	pF	HV sense capacitor, forms current divider with main resonant capacitor
RLLC sense resistor			42.7	ohms	LLC current sense resistor, senses current in sense capacitor
IS pin current limit resistor			220	ohms	Limits current from sense resistor into IS pin when voltage on sense R is < -0.5V
IS pin noise filter capacitor			1.0	nF	IS pin bypass capacitor; forms a pole with IS pin current limit capacitor
IS pin noise filter pole frequency			724	kHz	This pole attenuates IS pin signal
Loss Budget					
LCS device Conduction loss			1.1	W	Conduction loss at nominal line and full load
Output diode Loss			1.9	W	Estimated diode losses
Transformer estimated total copper loss			0.31	W	Total copper loss in transformer (primary + secondary)
Transformer estimated total core loss			1.5	W	Estimated core loss
Total transformer losses			1.8	W	Total transformer losses
Total estimated losses			4.9	W	Total losses in LLC stage
Estimated Efficiency			96%	%	Estimated efficiency
PIN			112	W	LLC input power
Secondary Turns and Voltage Centering Calculator					**This is to help you choose the secondary turns - Outputs not connected to any other part of spreadsheet**
V1			39.00	V	Target regulated output voltage Vo1. Change to see effect on slave output
V1d1			0.70	V	Diode drop voltage for Vo1
N1			9.00		Total number of turns for Vo1
V1_Actaul			39.00	V	Expected output
V2			0.00	V	Target output voltage Vo2
V2d2			0.70	V	Diode drop voltage for Vo2
N2			1.00		Total number of turns for Vo2
V2_Actual			3.71	V	Expected output voltage
Separate Series Inductor (For Non-Integrated Transformer Only)					**Not applicable if using integrated magnetics - not connected to any other part of spreadsheet**
Lsep			124.00	uH	Desired inductance of separate inductor
Ae_Ind			0.53	cm^2	Inductor core cross-sectional area
Inductor turns			24		Number of primary turns
BP_fnom			131	mT	AC flux for core loss calculations (at f_predicted and full load)
Expected peak primary current			3.0	A	Expected peak primary current
BP_fmin			295	mT	Peak flux density, calculated at minimum frequency fmin
Inductor Litz gauge			41	AWG	Individual wire strand gauge used for primary winding
Equivalent Inductor Metric Wire gauge			0.070	mm	Equivalent diameter of wire in metric units
Inductor litz strands			125		Number of strands used in Litz wire
Inductor parallel wires			1		Number of parallel individual wires to make up Litz

					wire
Resistivity_25 C_Sep_Ind			37.6	m-ohm/m	Resistivity in milli-ohms per meter
Inductor MLT			7.00	cm	Mean length per turn
Inductor DCR 25 C			63.2	m-ohm	Estimated resistance at 25 C (for reference)
Inductor DCR 100 C			84.7	m-ohm	Estimated resistance at 100 C (approximately 33% higher than at 25 C)
ACR_Sep_Inductor			135.5	m-ohm	Measured AC resistance (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature
Inductor copper loss			0.11	W	Total primary winding copper loss at 85 C
Feedback section					
VMAIN	**Auto**		39.00		Output voltage rail that optocoupler LED is connected to
ITL431_BIAS			1	mA	Minimum operating current in TL431 cathode
VF			1	V	Typical Optocoupler LED forward voltage at IOPTO_BJTMAX (max current)
VCE_SAT			0.3	V	Optocoupler transistor saturation voltage
CTR_MIN			0.8		Optocoupler minimum CTR at VCE_SAT and at IOPTO_BJT_MAX
VTL431_SAT			2.5	V	TL431 minimum cathode voltage when saturated
RLED_SHUNT			1	k-ohms	Resistor across optocoupler LED to ensure minimum TL431 bias current is met
ROPTO_LOAD			4.70	k-ohms	Resistor from optocoupler emitter to ground, sets load current
IFMAX			264.44	uA	FB pin current when switching at FMAX (e.g. startup)
IOPTO_BJT_MAX			0.89	mA	Optocoupler transistor maximum current - when bursting at FMAX (e.g. startup)
RLED_SERIES_MAX			15.17	k-ohms	Maximum value of gain setting resistor, in series with optocoupler LED, to ensure optocoupler can deliver IOPTO_BJT_MAX. Includes -10% tolerance factor.

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12 Heat Sinks

12.1 *Primary Heat Sink*

12.1.1 *Primary Heat Sink Sheet Metal*

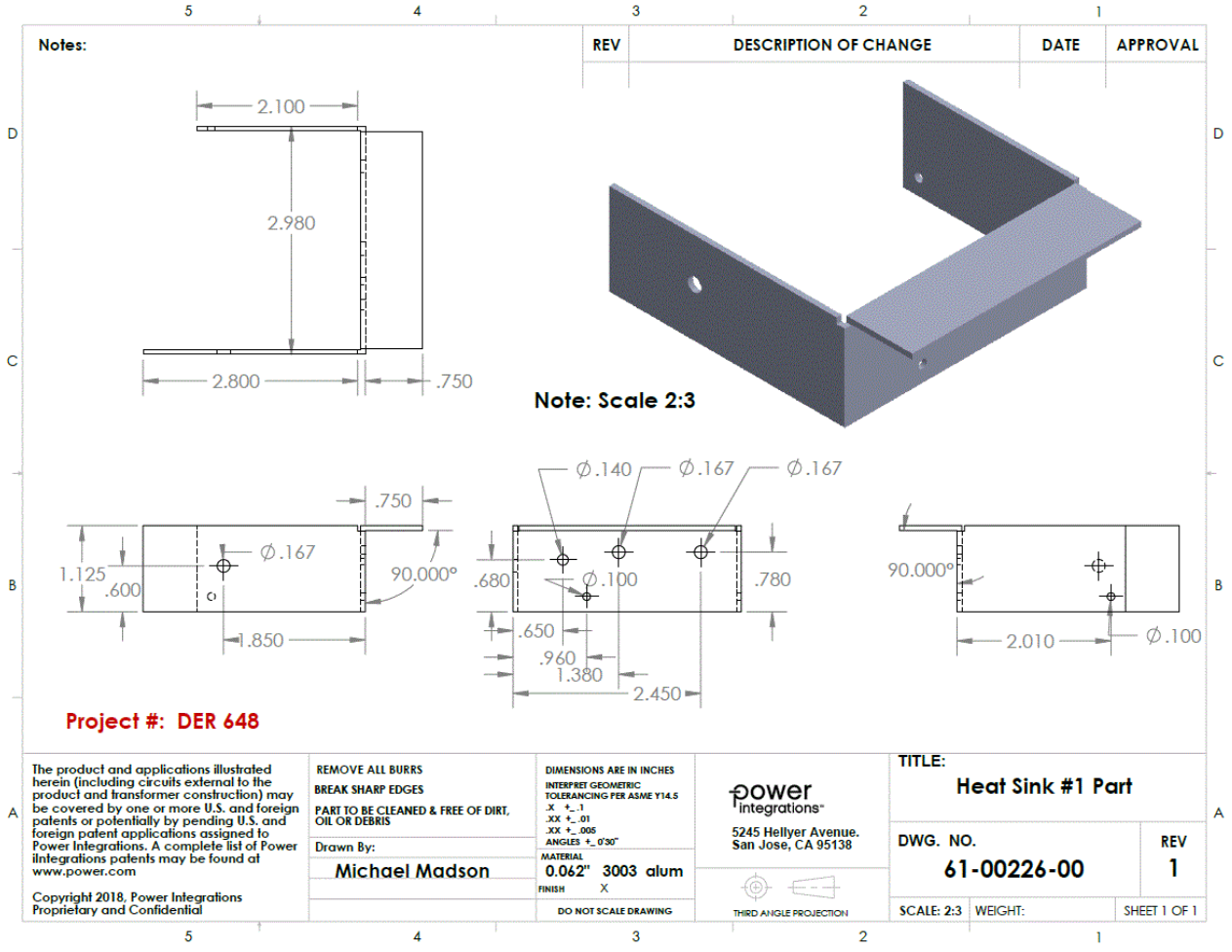

Figure 20 – Primary Heat Sink Sheet Metal Drawing.

12.1.2 *Primary Heat Sink with Fasteners*

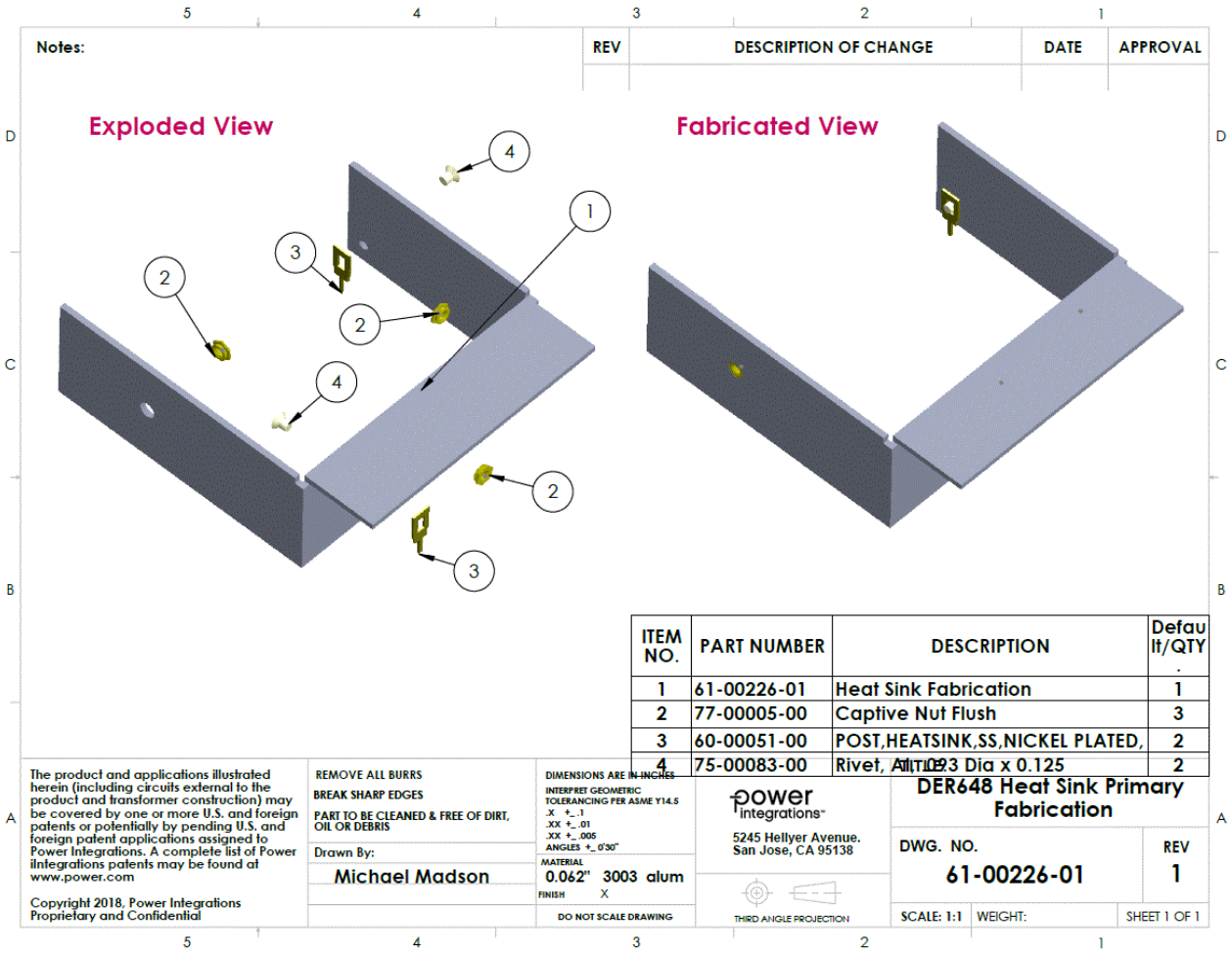

Figure 21 – Finished Primary Heat Sink Drawing with Installed Fasteners.

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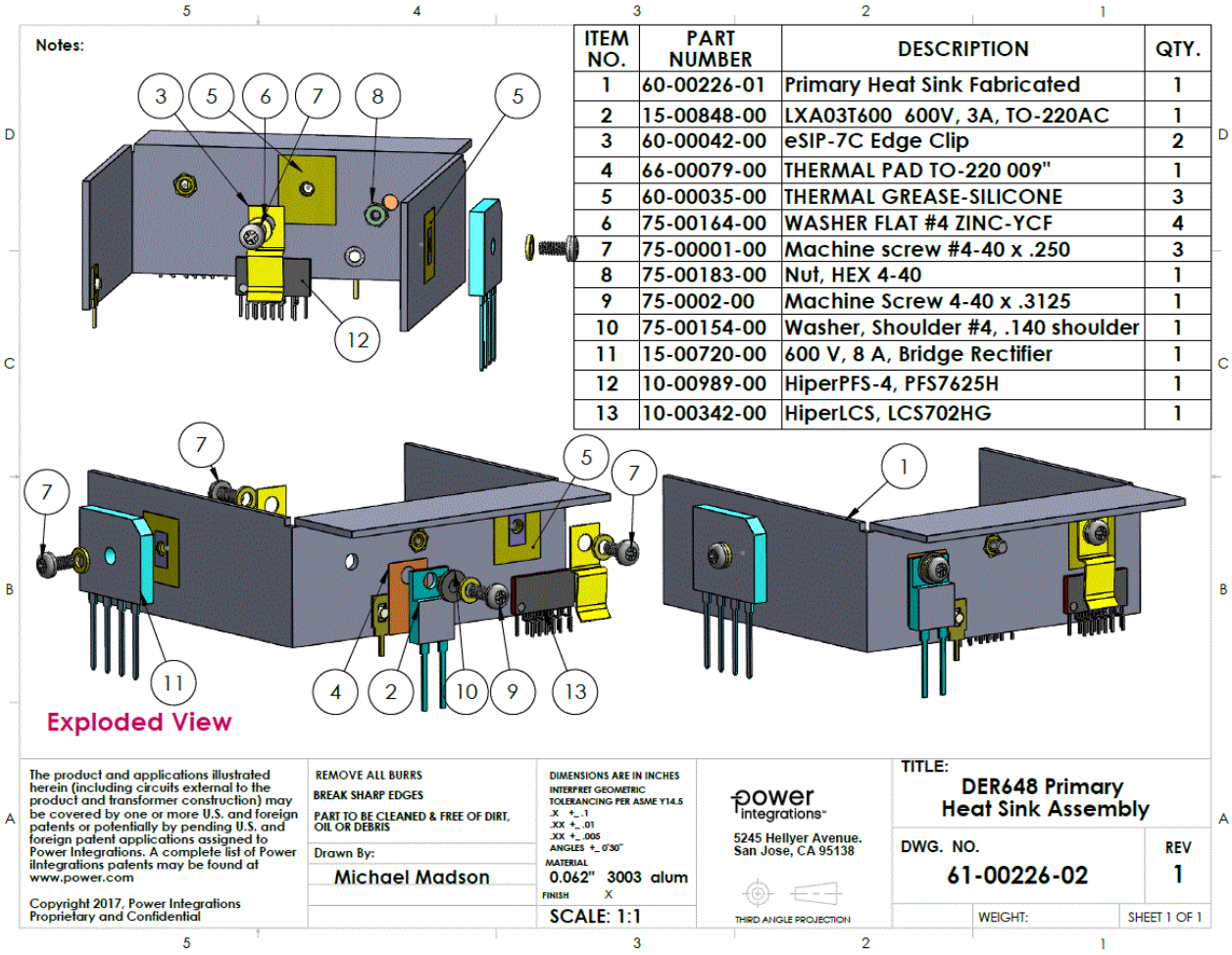
12.1.3 *Primary Heat Sink Assembly*



ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	60-00226-01	Primary Heat Sink Fabricated	1
2	15-00848-00	LXA03T600 600V, 3A, TO-220AC	1
3	60-00042-00	eSIP-7C Edge Clip	2
4	66-00079-00	THERMAL PAD TO-220 009"	1
5	60-00035-00	THERMAL GREASE-SILICONE	3
6	75-00164-00	WASHER FLAT #4 ZINC-YCF	4
7	75-00001-00	Machine screw #4-40 x .250	3
8	75-00183-00	Nut, HEX 4-40	1
9	75-0002-00	Machine Screw 4-40 x .3125	1
10	75-00154-00	Washer, Shoulder #4, .140 shoulder	1
11	15-00720-00	600 V, 8 A, Bridge Rectifier	1
12	10-00989-00	HiperPFS-4, PFS7625H	1
13	10-00342-00	HiperLCS, LCS702HG	1

Figure 22 – Primary Heat Sink Assembly.

12.2 ***Secondary Heat Sink***

12.2.1 *Secondary Heat Sink Sheet Metal*

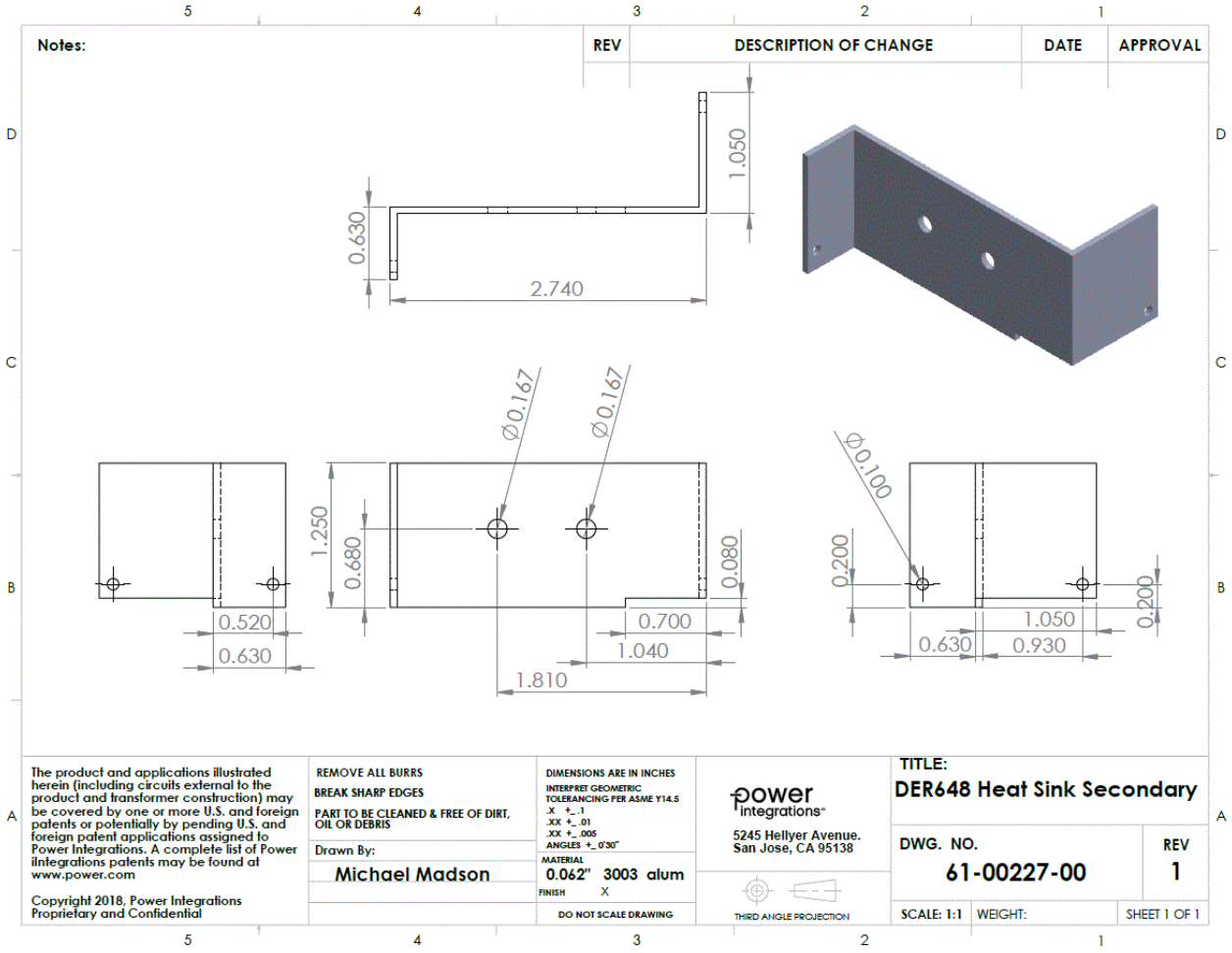


Figure 23 – Secondary Heat Sink Sheet Metal Drawing.

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12.2.2 *Secondary Heat Sink with Fasteners*

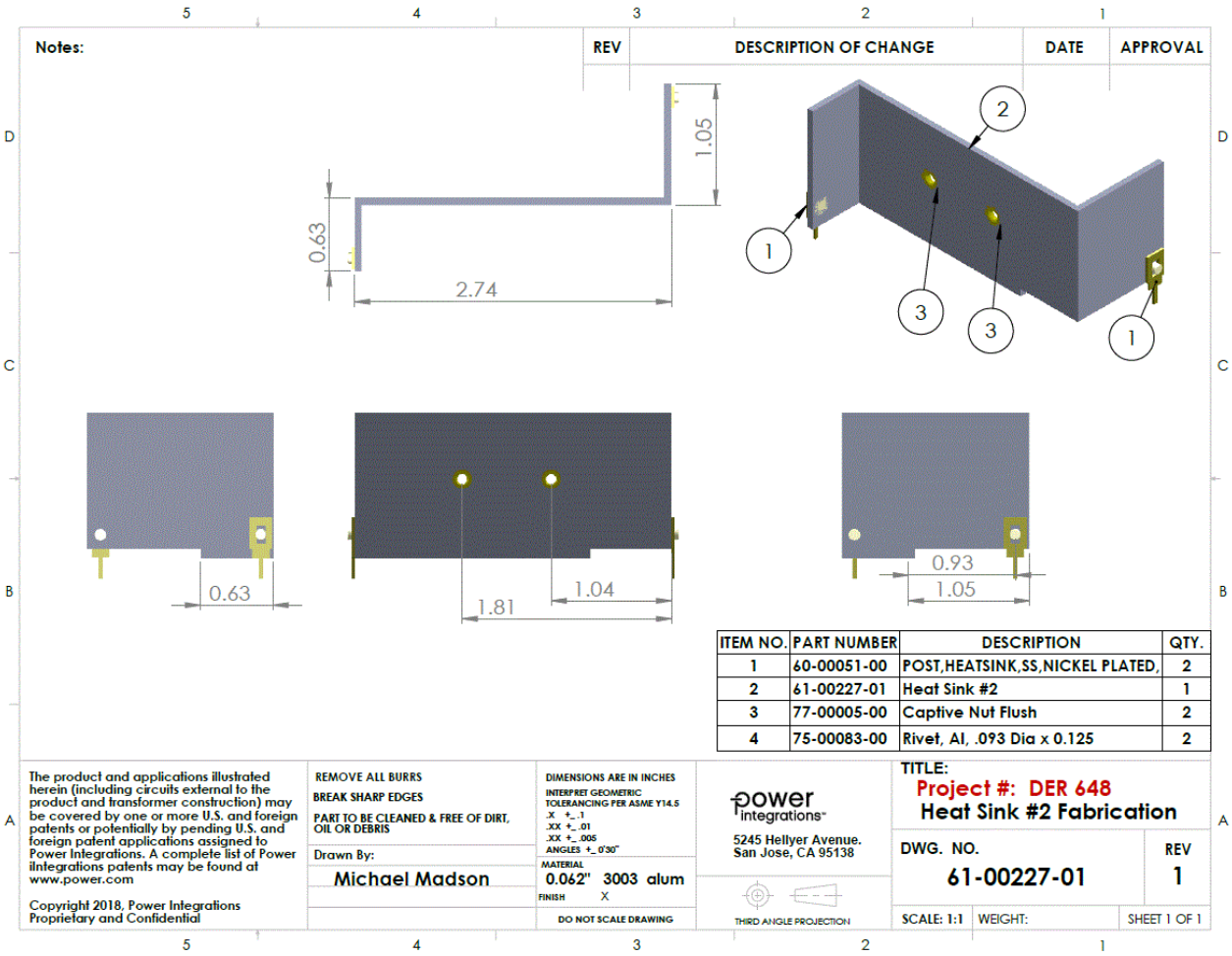

Figure 24 – Finished Secondary Heat Sink with Installed Fasteners.

12.2.3 *Secondary Heat Sink Assembly*

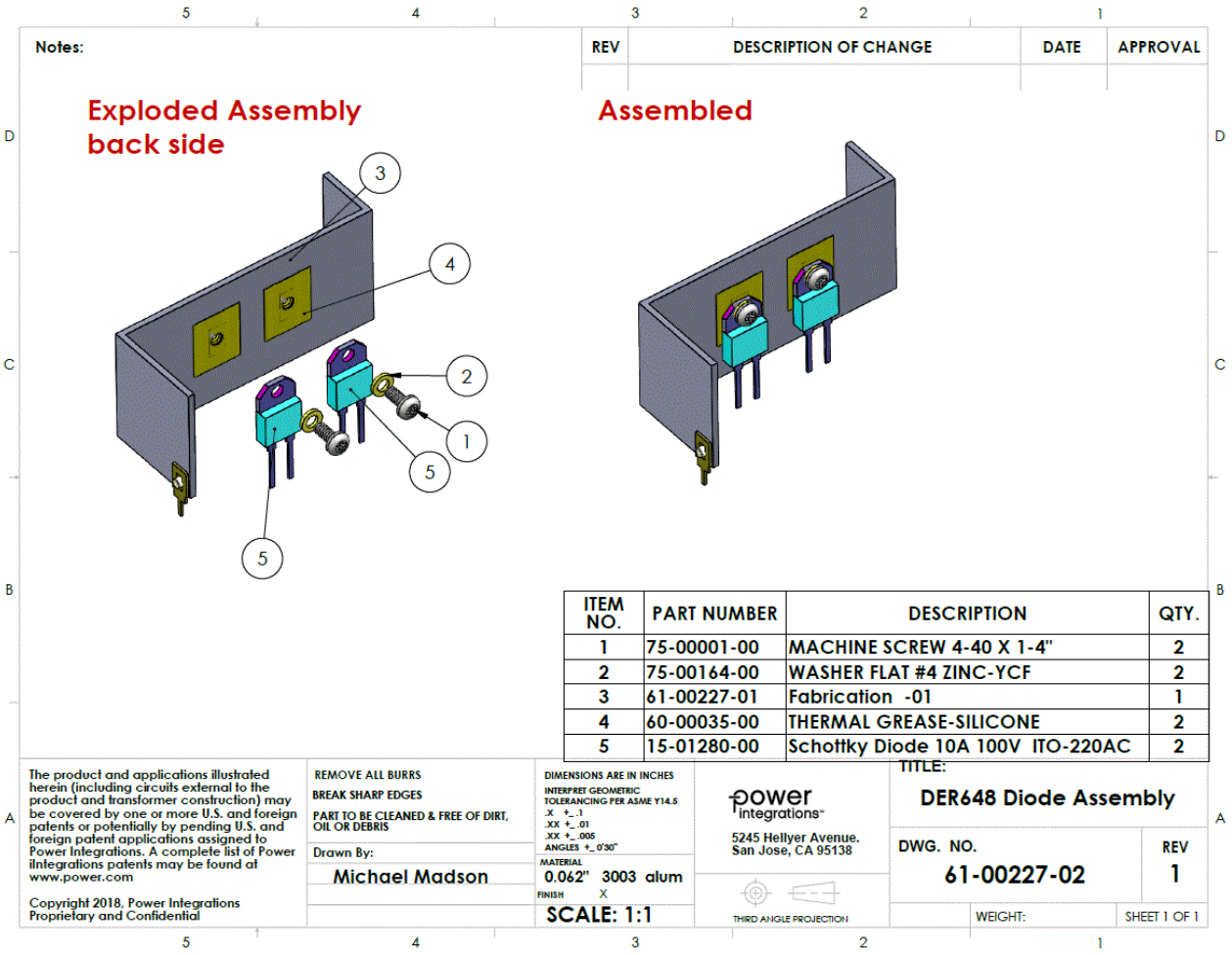

Figure 25 – DER-648 Secondary Heat Sink Assembly.

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13 Performance Data

All measurements were taken at room temperature and 60 Hz (input frequency) unless otherwise specified. Output voltage measurements were taken at the output connectors.

13.1 *LLC Stage Efficiency*

To make this measurement, the LLC stage was powered by connecting an external 440 VDC source across bulk capacitor C19 , with external supplies to source the primary and secondary bias voltages. The output of the supply was used to feed an electronic load set for constant voltage with a series 2.3 Ω resistor to simulate the dynamic impedance of an equivalent LED load. Data was taken at 54 V, 46 V, and 39 V, these being the maximum, median, and minimum voltages for the led panel. The dimming input of the supply was used with a wide range PWM source to program the current delivered to the load in order to vary the output power.

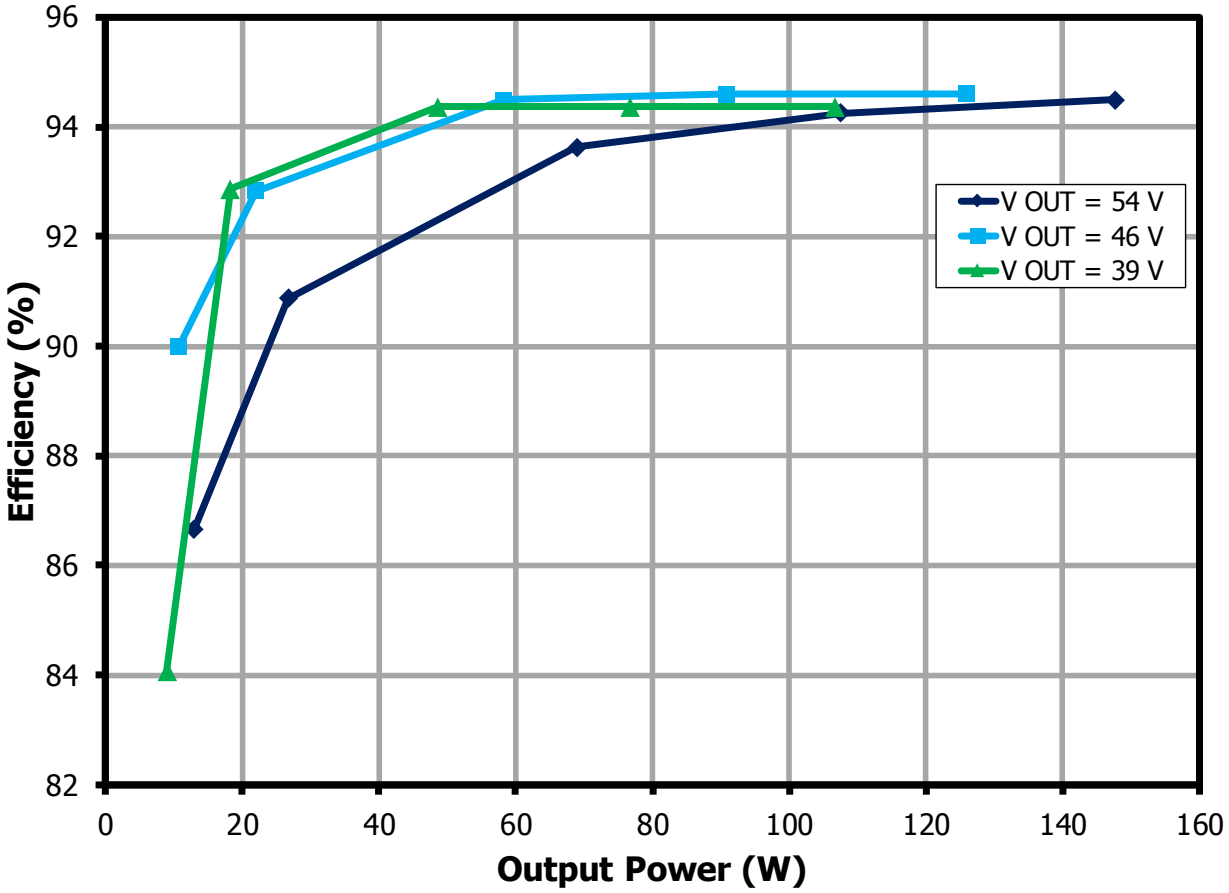

Figure 26 – LLC Stage Efficiency vs. Load, 440 VDC Input.

13.2 *PFC Stage Efficiency*

For this measurement, the LLC converter was disabled by removing resistor R17 in the input voltage sensing string. The PFC was powered using a sine wave source, and the B+ was loaded with an electronic load in CC mode.

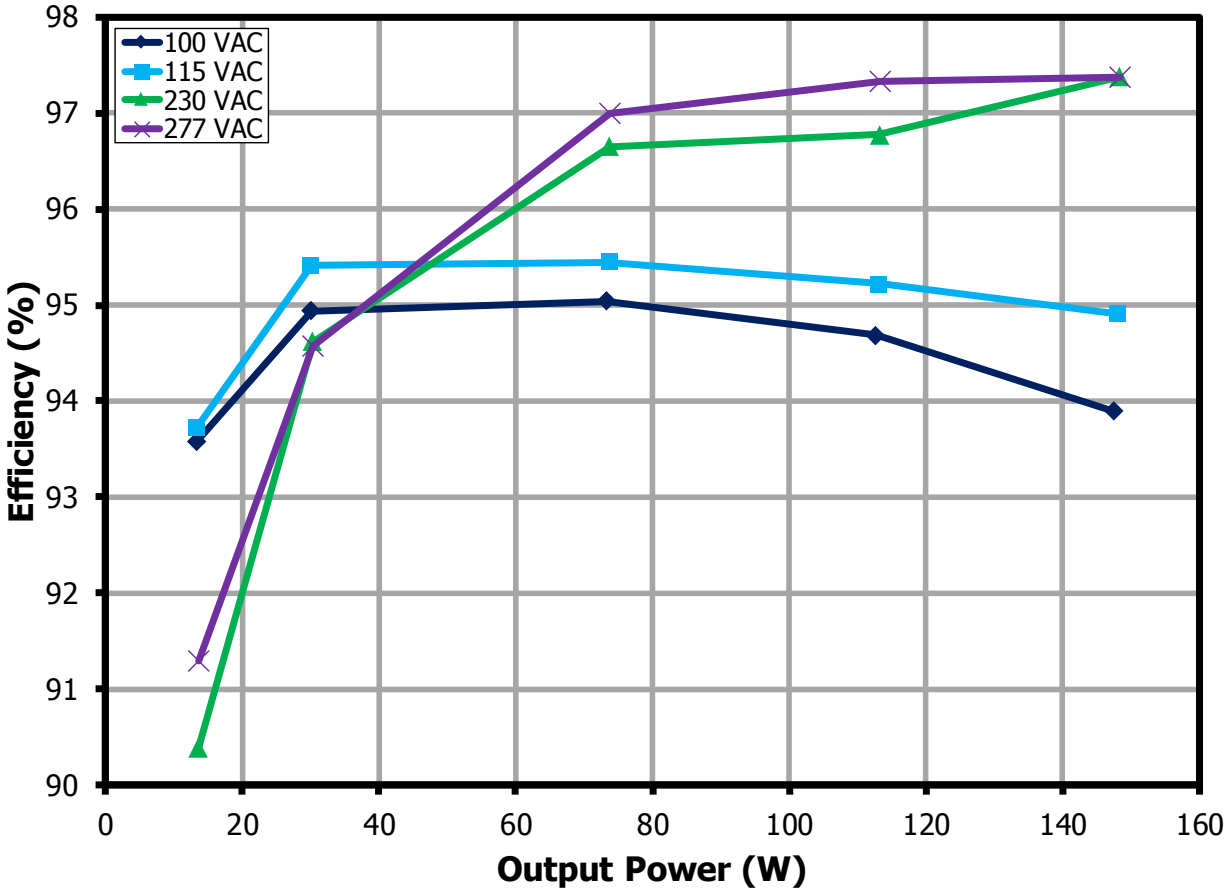

Figure 27 – PFC Stage Efficiency vs. Load.

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13.3 *Total Efficiency*

Figures below show the total supply efficiency (PFC and LLC stages). AC input was supplied using a sine wave source. The output was loaded with an electronic load set for constant voltage mode with a 2.3 Ω series resistance to mimic the characteristics of the LED array depicted in section 7. Output voltage was adjusted for 54 V. Output current was adjusted using the UUT dimming input and a pulse generator with wide duty cycle range.

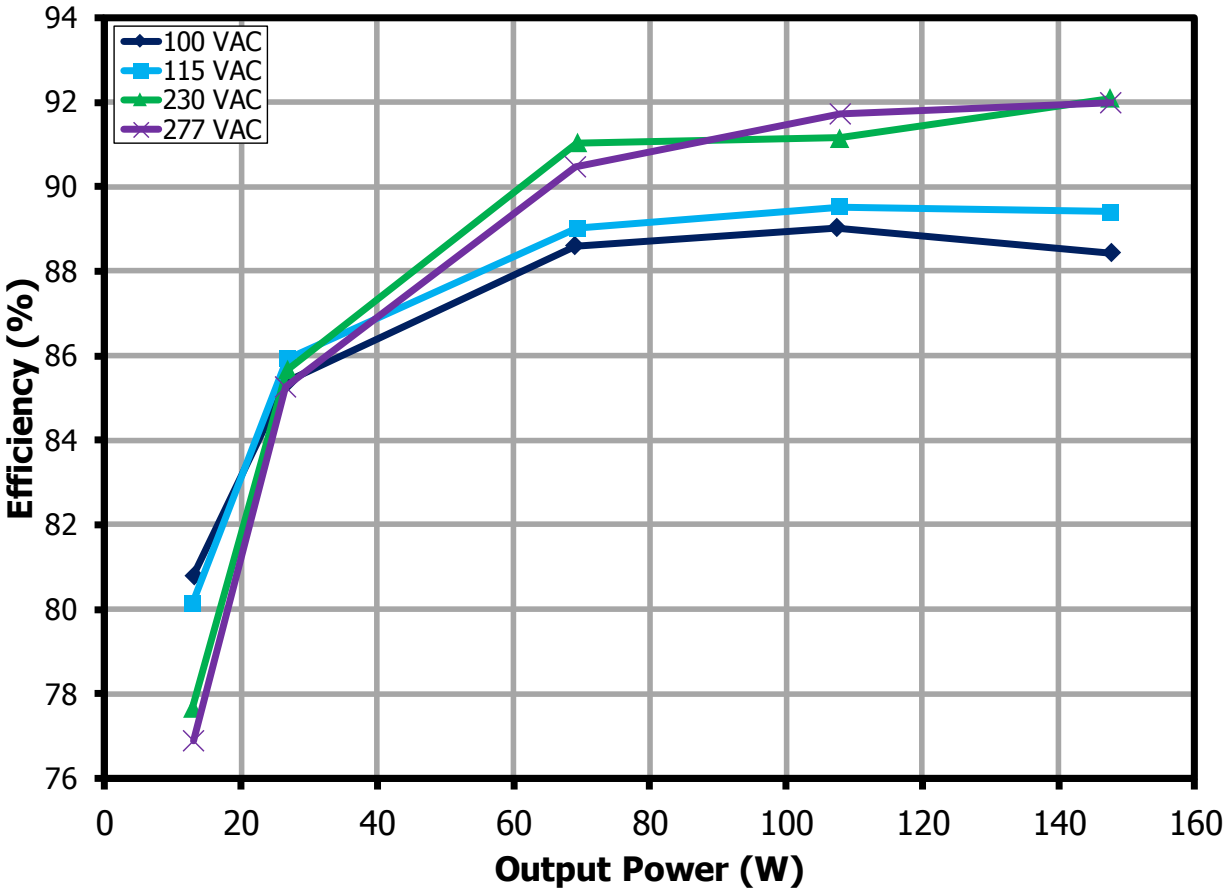

Figure 28 – Total Efficiency vs. Load, 54 V Output.

13.4 *No-Load Input Power*

No-load input power was tested with a sine wave source and a Yokogawa WT210 power analyzer set for a 20-minute integration time. The LLC stage was disabled using the inhibit input, and the UUT output cable was left unplugged.

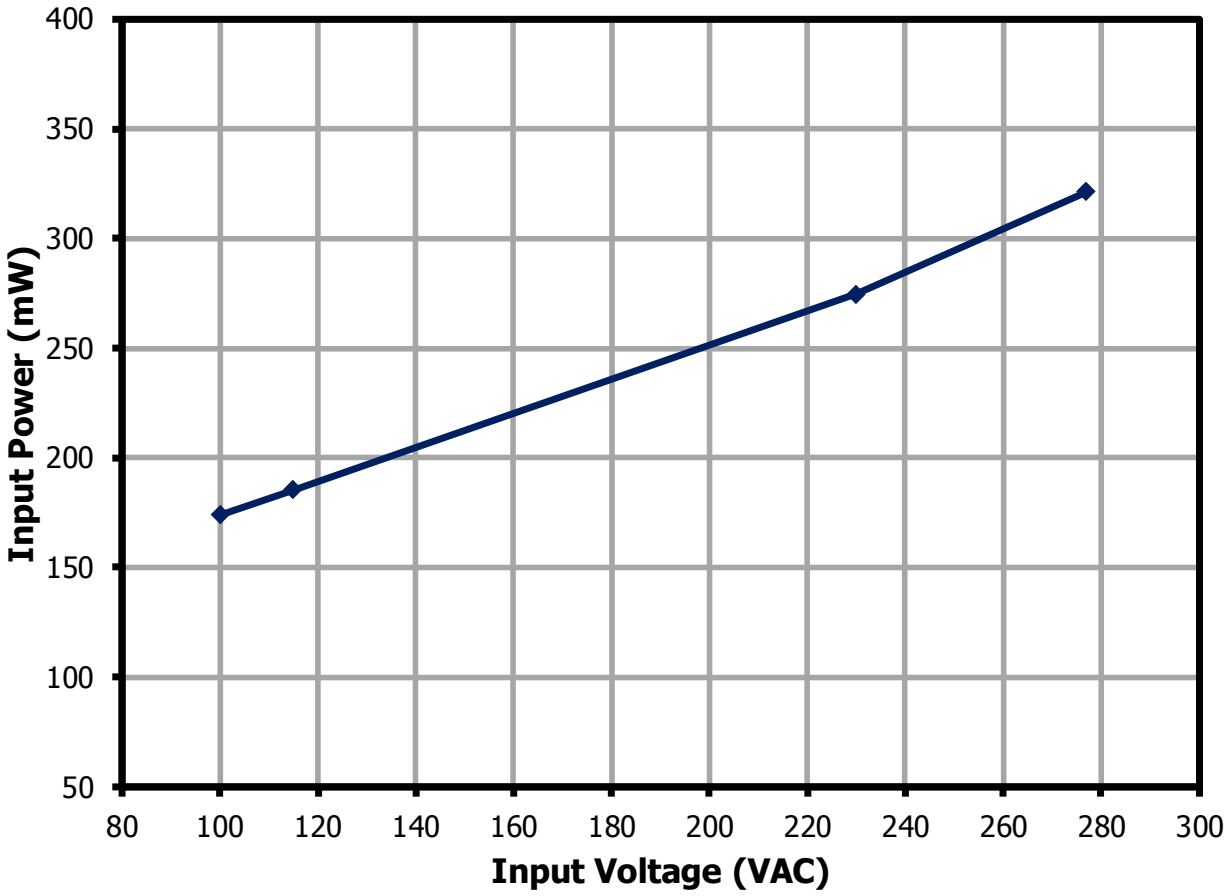

Figure 29 – No-Load Input Power vs. Input Voltage.

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13.5 *Power Factor*

Power factor measurements were made using a sine wave AC source and a constant voltage electronic load with 2.3 Ω series resistor. Output Voltage was set to 54 V using an electronic CV load with 2.3 Ω series resistance. Output power was varied using the supply dimming input and a wide range PWM source.

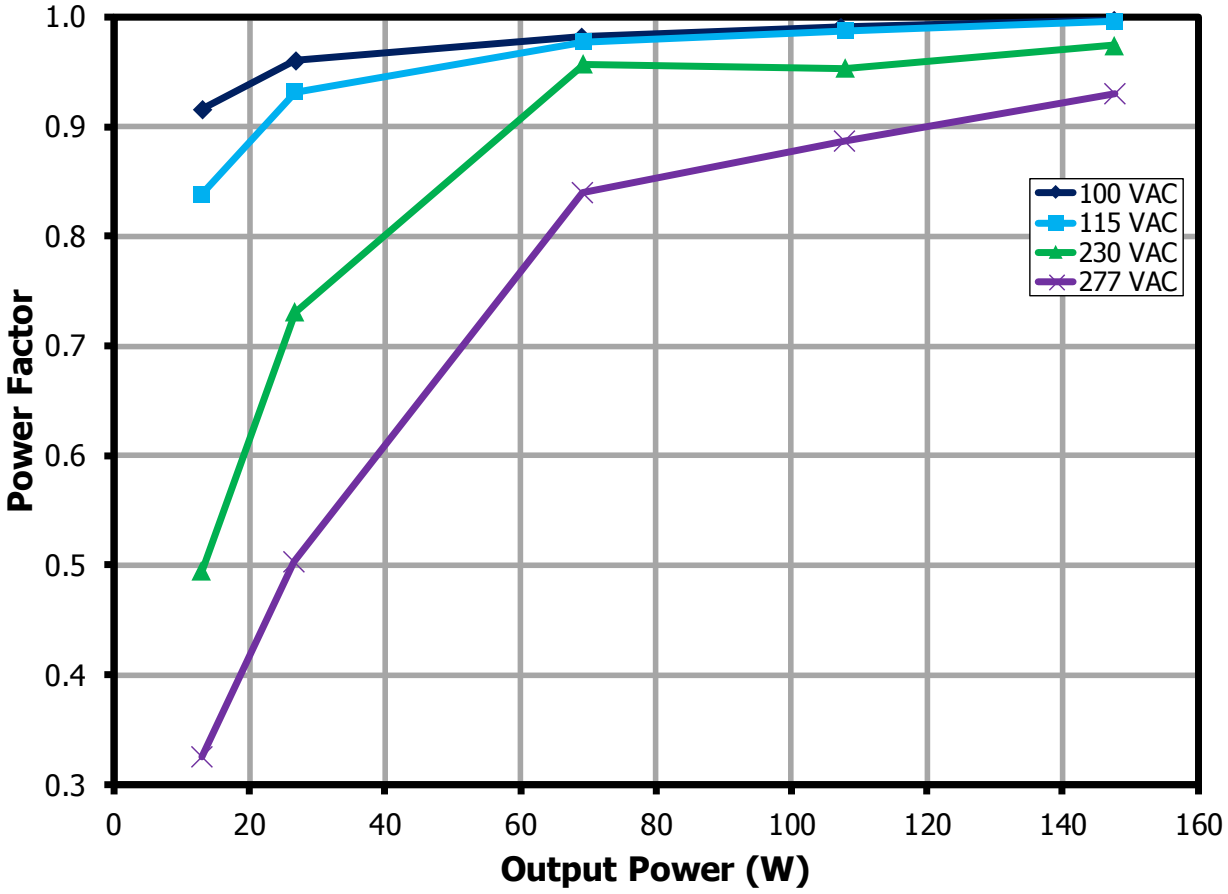

Figure 30 – Power Factor vs. Output Power.

13.6 *THD vs. Output Power*

THD was measured using an electronic load set for constant voltage mode, with a 2.3 Ω series resistor. Output voltage was adjusted for 54 V. Output current was adjusted using the dimming input and a wide duty cycle range pulser.

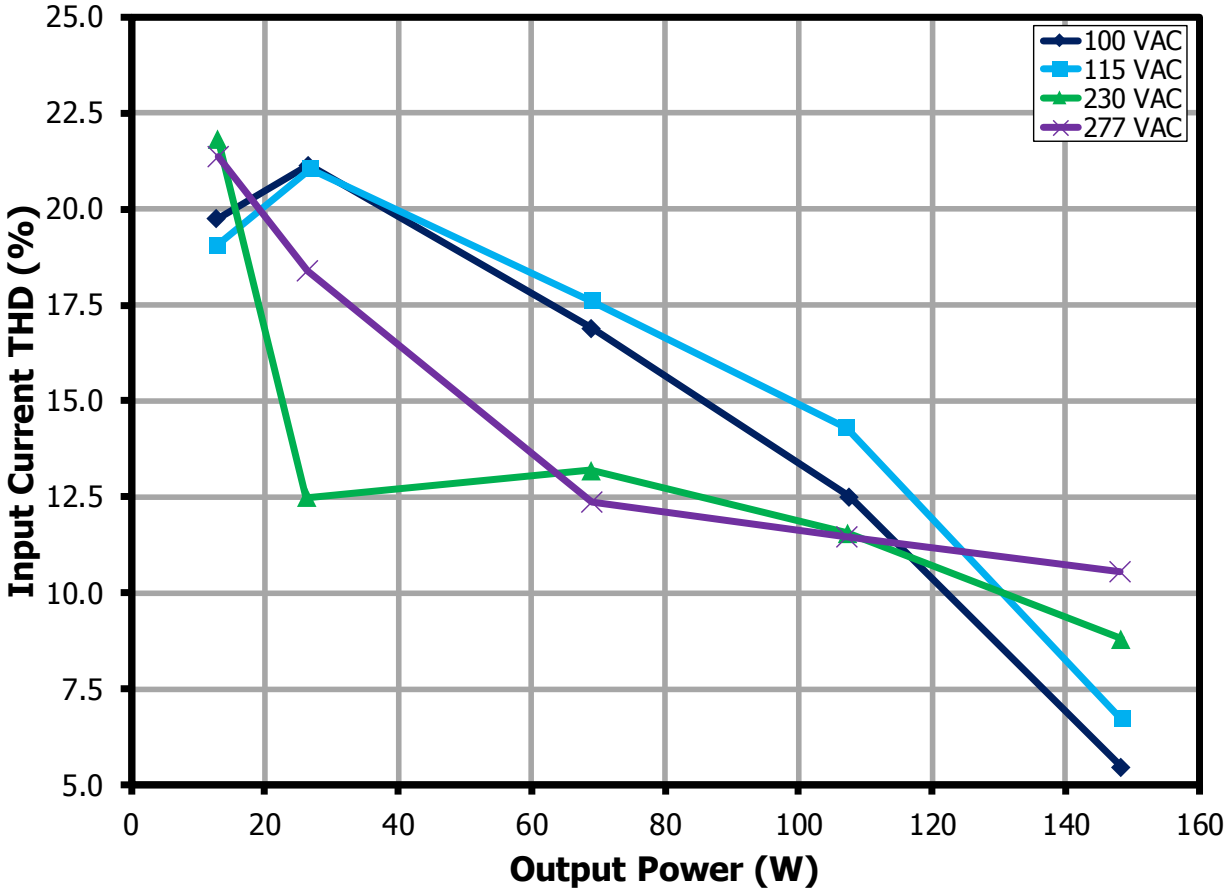

Figure 31 – Input Current THD vs. Output Power.

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13.7 *Output Current vs. Dimming PWM Duty Cycle*

Output dimming characteristics were measured using a sine wave AC source and an electronic load configured for constant voltage. Dimming signal was provided using the circuit shown in Figure 32, which acts as a ~1% to 99% duty pulse generator at a frequency of approximately 1 kHz. Diodes D3 and D4 clamp the output signal amplitude to ~1.2 V.

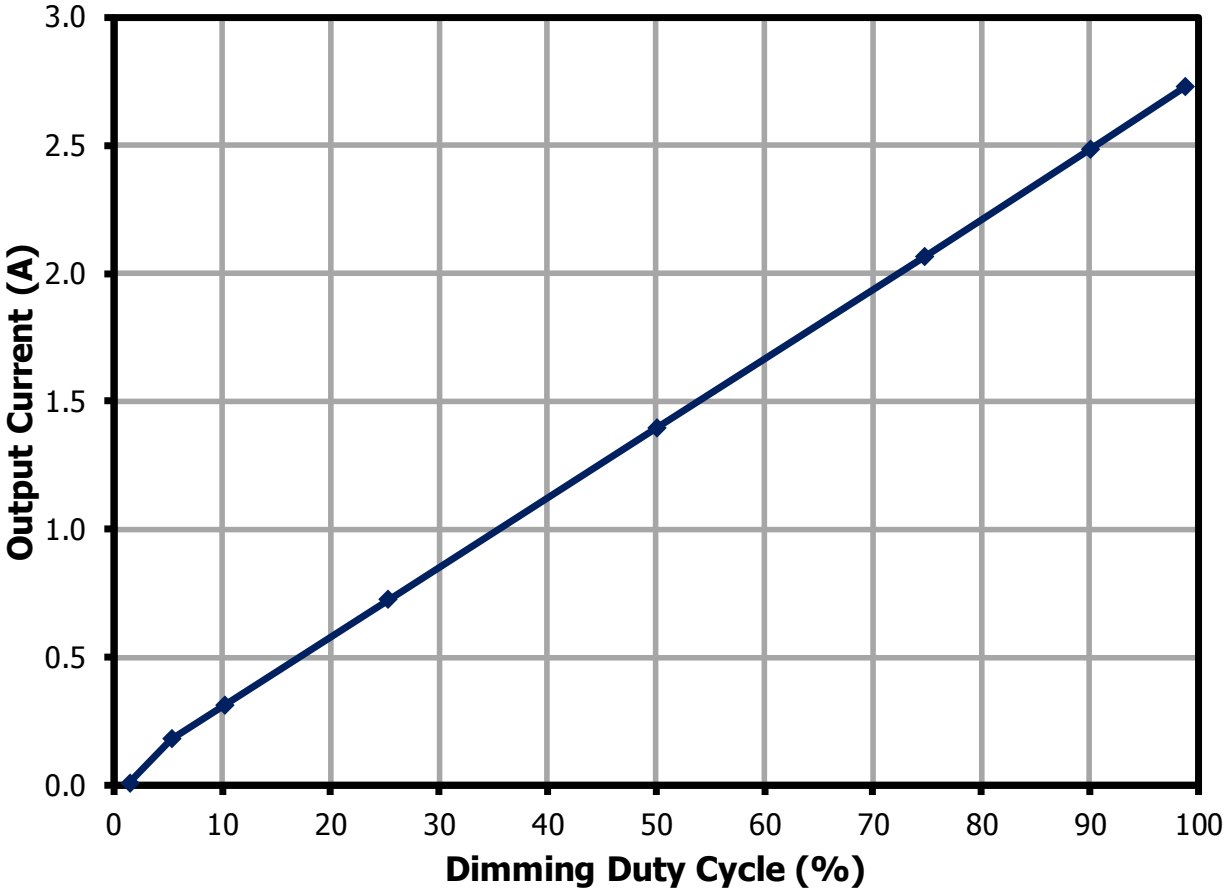

Figure 32 – Output Current vs. Dimming Duty Cycle.

The circuit shown in Figure 33 is based on a CMOS variant of the ubiquitous NE555 timing IC. Feeding back a resistor from the output of U1 to its THRESHOLD and TRIGGER pins with a timing capacitor (C1) to GND results in a simple square wave generator with near 50% duty cycle. This basic circuit is modified by splitting the charge and discharge paths for C1 via diodes D1 and D2. Potentiometer R1 is used to adjust the weighting of charge and discharge resistance to vary the output duty cycle over a wide range.

13.7.1.1 Schematic for Simple Wide Range PWM Generator

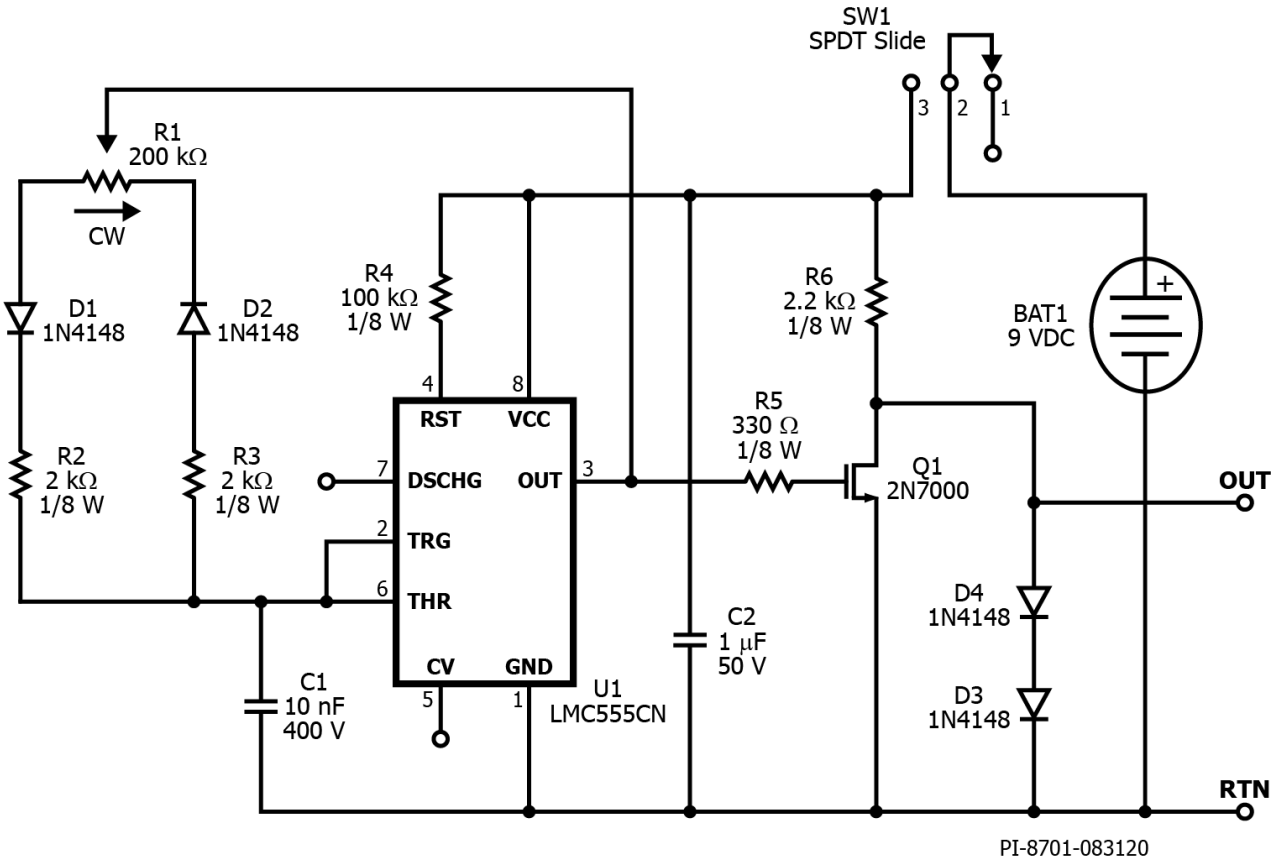

Figure 33 – Circuit for Generating Wide Range PWM Dimming Check Waveform.

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13.7.1.2 BOM for PWM Generator

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BAT1	Holder, Battery, 9 V, PC mount	BH9VPC	MPD
2	1	C1	10 nF, 400 V, Film	ECQ-E4103KF	Panasonic
3	1	C2	1 μF, 50 V, Ceramic, X7R	FK16X7R1H105K	TDK
4	4	D1 D2 D3 D4	75 V, 300 mA, Fast Switching, DO-35	1N4148TR	Vishay
5	1	Q1	MOSFET N-CH 60V 0.2A N-Channel, TO-92	2N7000-G	On Semi
6	1	R1	POT, 200 kΩ, 20%, 1/2 W, Square Trimming	3310Y-001-204L	BOURNS
7	2	R2 R3	RES, 2 kΩ, 5%, 1/8 W, Carbon Film	CF18JT2K00	Stackpole
8	1	R4	RES, 100 kΩ, 5%, 1/8 W, Carbon Film	CF18JT100K	Stackpole
9	1	R5	RES, 330 Ω, 5%, 1/8 W, Carbon Film	CF18JT330R	Stackpole
10	1	R6	RES, 2.2 kΩ, 5%, 1/8 W, Carbon Film	CF18JT2K20	Stackpole
11	1	SW1	SWITCH SLIDE SPDT 30 V, 2 A PC MNT	EG1218	E-Switch
12	1	U1	LMC555 CMOS TIMER 8-DIP	LMC555CN/NOPB	Texas Instruments

13.8 *Output V-I Characteristic*

The V-I characteristic is generated using an electronic load programmed for constant resistance, so that both the CV and CC portions of the characteristic curve can be viewed. Input voltage is 115 VAC, 60 Hz.

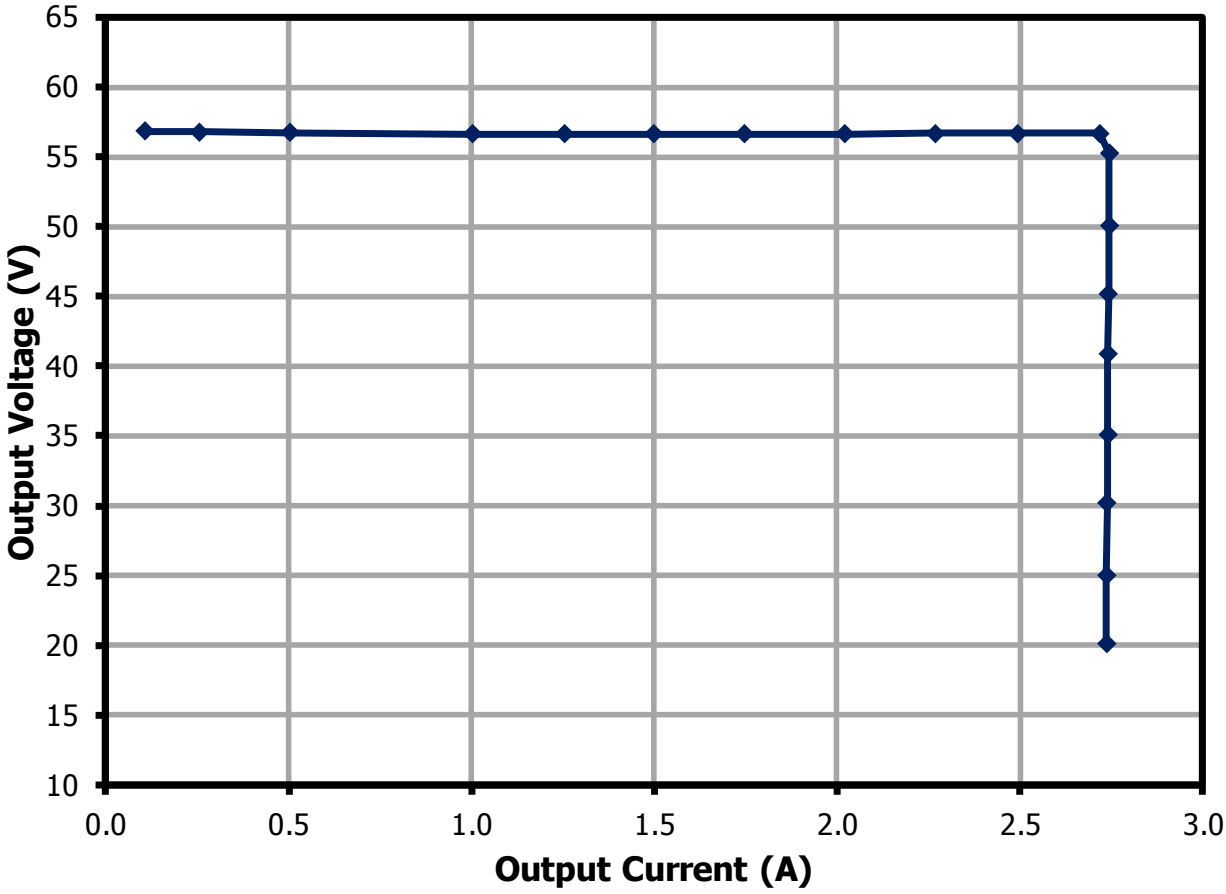

Figure 34 – Output V-I Characteristic.

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14 Waveforms

The input current waveform was measured using a CV output load with 2.3 Ω series resistance, with the output voltage adjusted to 54 V.

14.1 *Input Current, 100% Load*

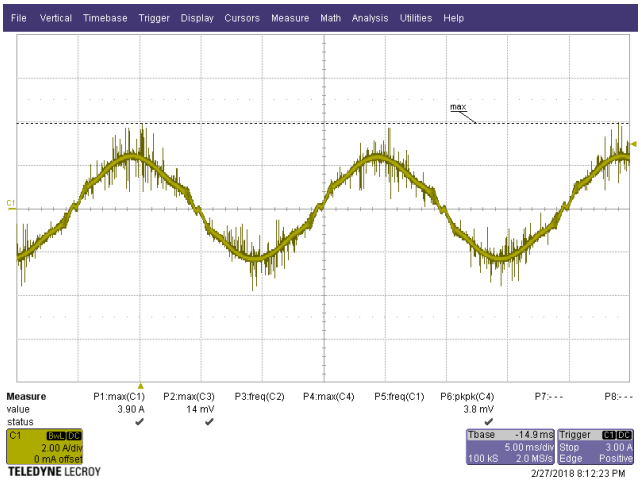

Figure 35 – Input Current, 100 VAC, 50 Hz, 150 W Load, 2 A, 5 ms / div.

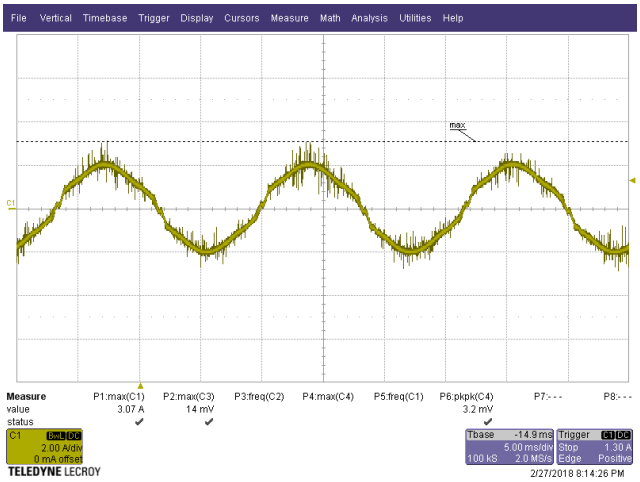

Figure 36 – Input Current, 115 VAC, 60 Hz, 150 W Load, 2 A, 5 ms / div.

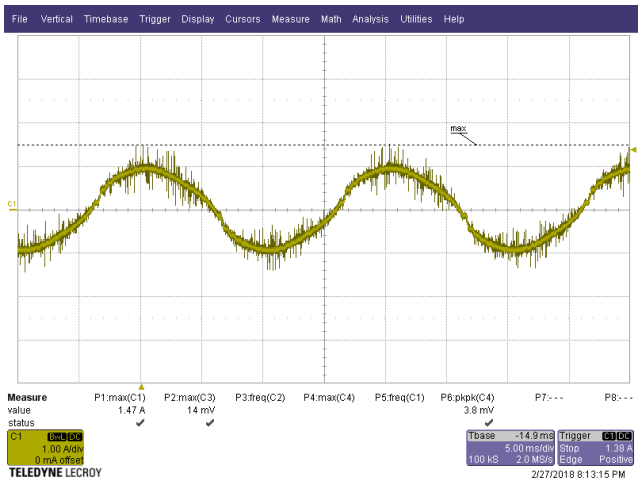

Figure 37 – Input Current, 230 VAC, 50 Hz, 150 W Load, 1 A, 5 ms / div.

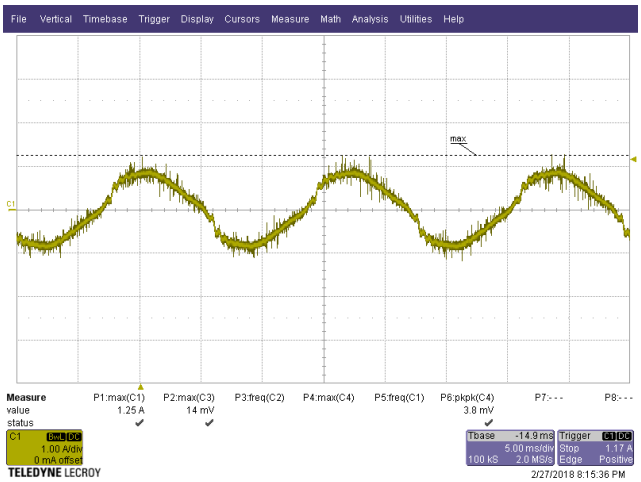

Figure 38 – Input Current, 277 VAC, 60 Hz, 150 W Load, 1 A, 5 ms / div.

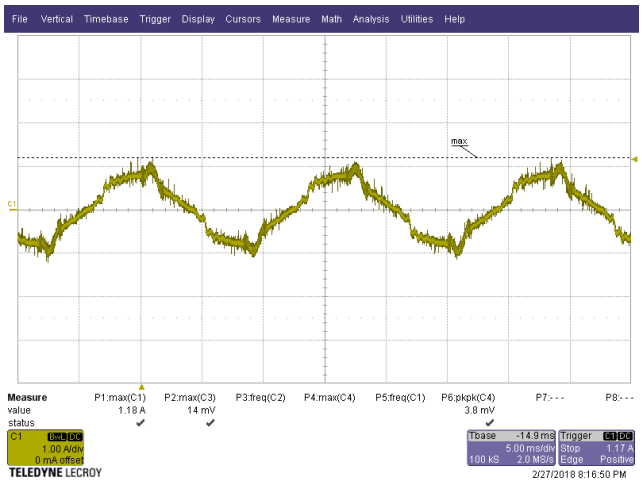

Figure 39 – Input Current, 300 VAC, 60 Hz, 150 W Load, 1 A, 5 ms / div.

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14.2 *LLC Primary Voltage and Current*

The LLC stage primary current was measured by inserting a current sensing loop in series with the ground side of resonating capacitor C30. The output was loaded with an electronic load set for constant voltage, with a series 2.3 Ω resistor to simulate the dynamic impedance of the LED array shown in Section 7. The load was adjusted for output voltages of 54 V, 46 V, and 39 V, representing the worst case maximum LED panel voltage, nominal voltage, and minimum. At 54 V, the LLC converter runs substantially below resonance. At 48 V output, the converter runs slightly below resonance, while at 39 V, it runs substantially above resonance.

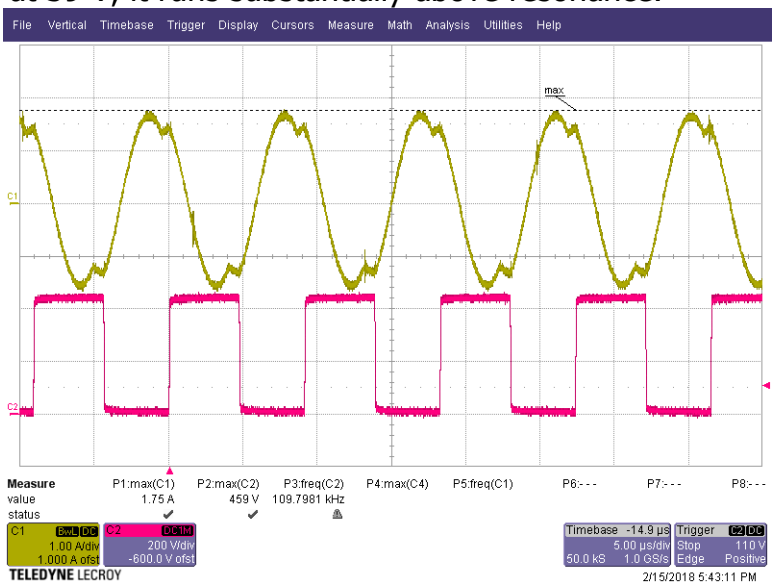

Figure 40 – LLC Stage Primary Voltage and Current, 100% Load, 54 V Output Voltage.
Upper: Current, 1 A / div.
Lower: Voltage, 200 V, 5 µs / div.

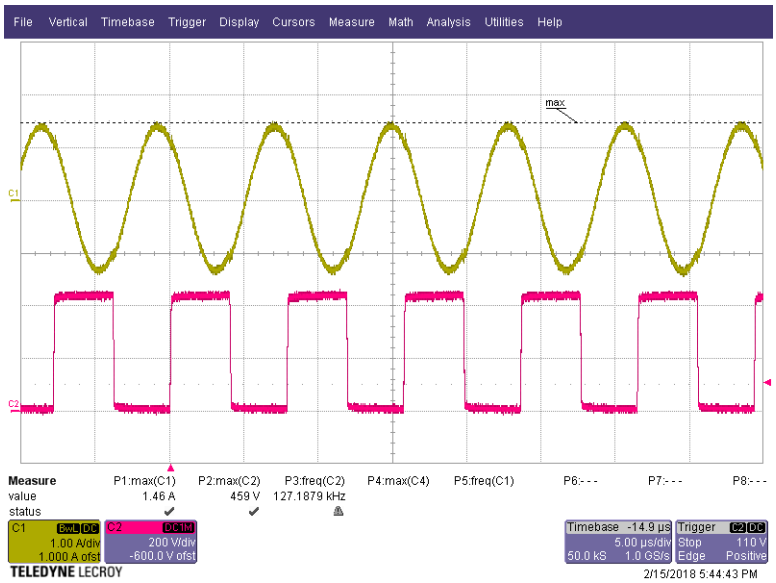

Figure 41 – LLC Stage Primary Voltage and Current, 100% Load, 46 V Output Voltage.
Upper: Current, 1 A / div.
Lower: Voltage, 200 V, 5 µs / div.

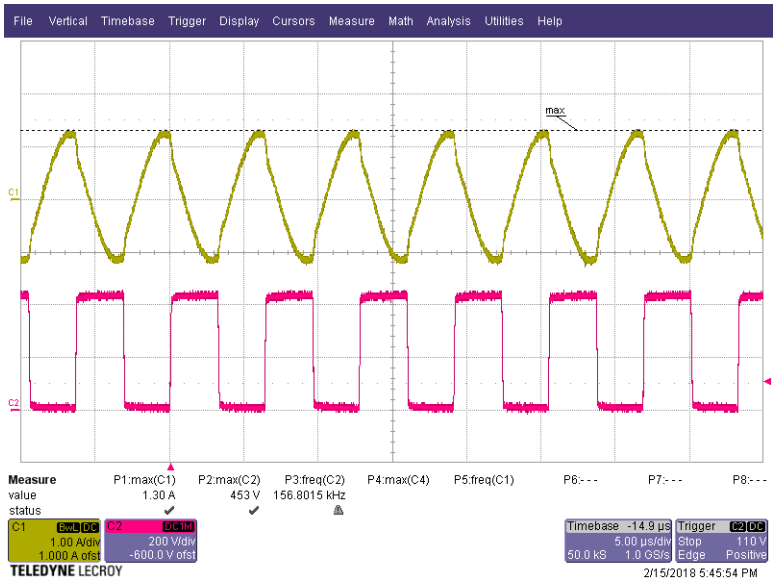

Figure 42 – LLC Stage Primary Voltage and Current, 100% Load, 39 V Output Voltage.
Upper: Current, 1 A / div.
Lower: Voltage, 200 V, 5 µs / div.

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14.3 *Output Rectifier Peak Reverse Voltage*

Voltage across output rectifiers D11 and D12 was measured using a CV load with 2.3 Ω series resistance, set for 54 V output (worst case).

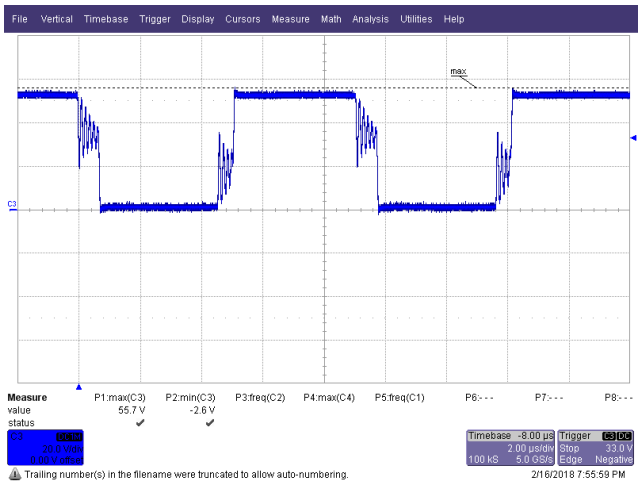

Figure 43 – Output Rectifier (D11) Reverse Voltage, 100% Load.
20 V, 2 µs / div.

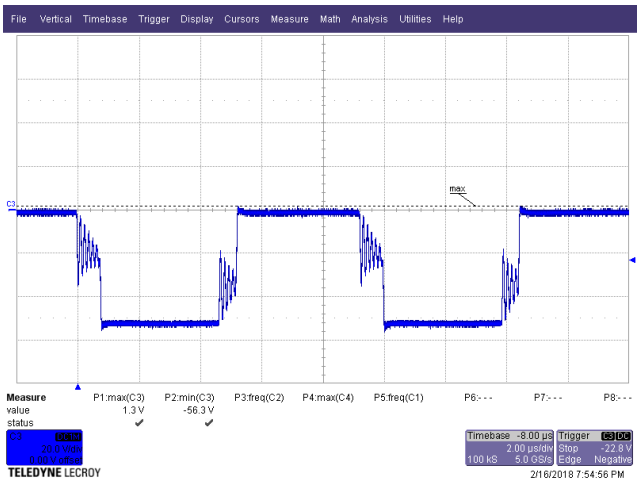

Figure 44 – Output Rectifier (D12) Reverse Voltage, 100% Load.
20 V, 2 µs / div.

14.4 *PFC Voltage and Current, 100% Load*

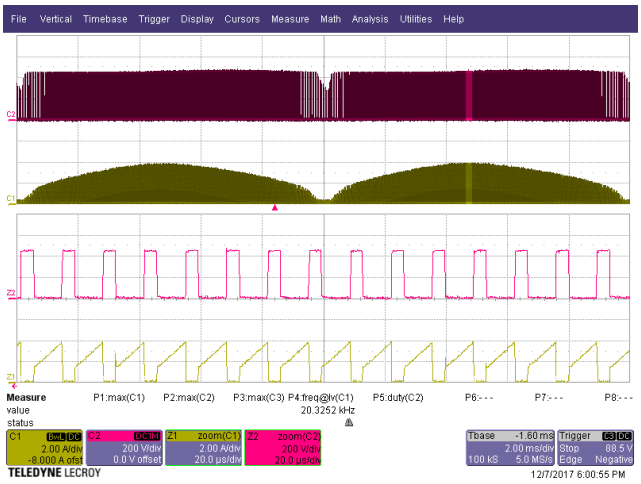

Figure 45 – PFC Stage Drain Voltage and Current, Full Load, 100 VAC, 50 Hz.
Upper: V_{DRAIN}, 200 V / div.
Lower: Switch Current, 2 A, 2 ms / div.

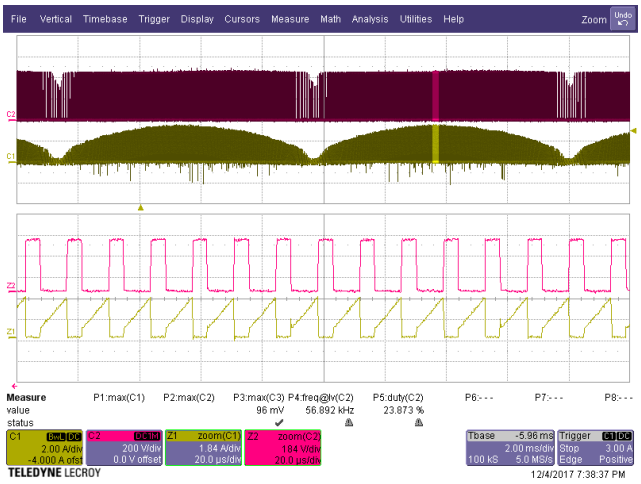

Figure 46 – PFC Stage Drain Voltage and Current, Full Load, 115 VAC, 60 Hz.
Upper: V_{DRAIN}, 200 V / div.
Lower: Switch Current, 2 A, 2 ms / div.

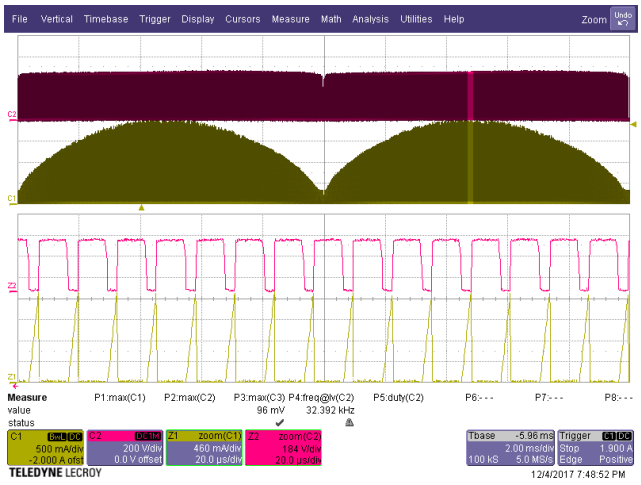

Figure 47 – PFC Stage Drain Voltage and Current, Full Load, 230 VAC, 50 Hz.
Upper: V_{DRAIN}, 200 V / div.
Lower: Switch Current, 0.5 A, 2 ms / div.

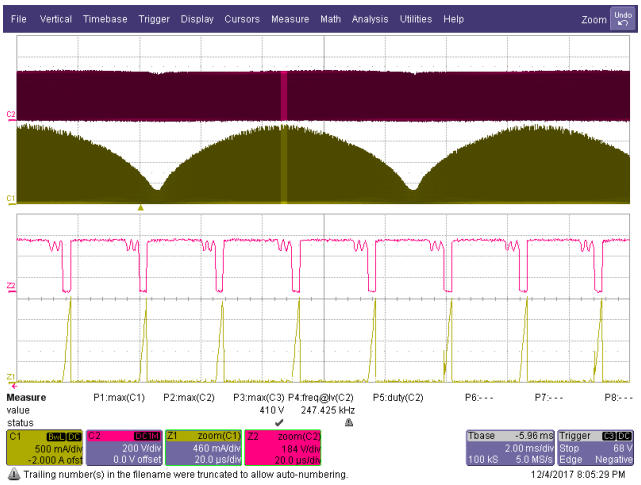

Figure 48 – PFC Stage Drain Voltage and Current, Full Load, 277 VAC, 60 Hz.
Upper: V_{DRAIN}, 200 V / div.
Lower: Switch Current, 0.5 A, 2 ms / div.

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14.5 *AC Input Current and PFC Output Voltage during Start-up*

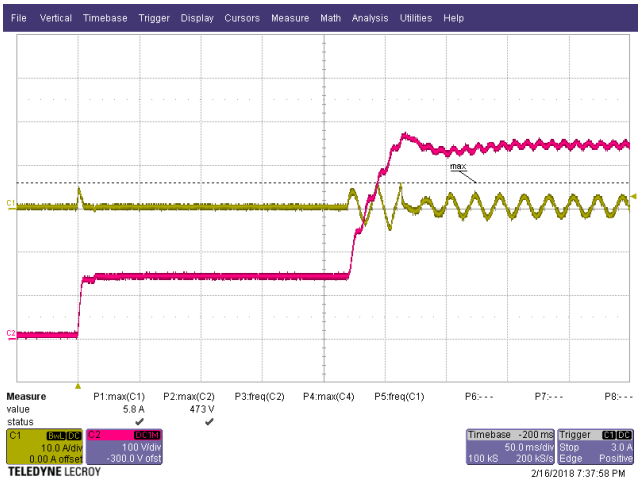

Figure 49 – AC Input Current vs. PFC Output Voltage at Start-up, Full Load, 100 VAC, 50 Hz.
Upper: AC Input Current, 10 A / div.
Lower: PFC Voltage, 100 V, 10 ms / div.

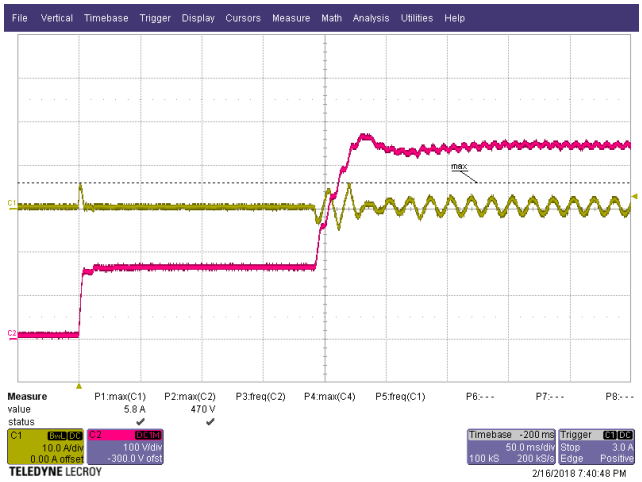

Figure 50 – AC Input Current vs. PFC Output Voltage at Start-up, Full Load, 115 VAC, 60 Hz.
Upper: AC Input Current, 10 A / div.
Lower: PFC Voltage, 100 V, 10 ms / div.

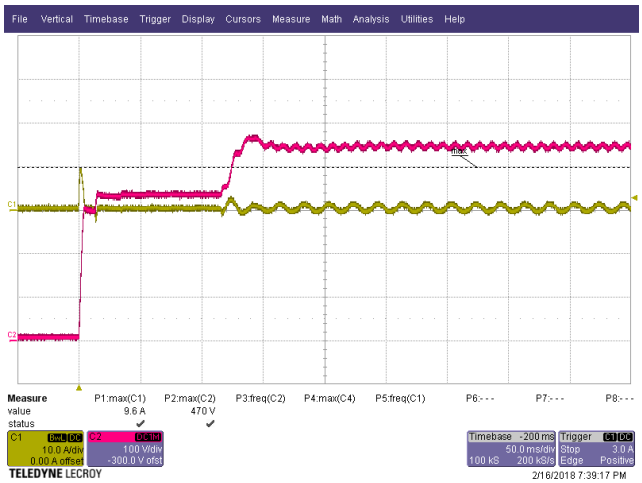

Figure 51 – AC Input Current vs. PFC Output Voltage at Start-up, Full Load, 230 VAC, 50 Hz.
Upper: AC Input Current, 10 A /div.
Lower: PFC Voltage, 100 V, 10 ms / div.

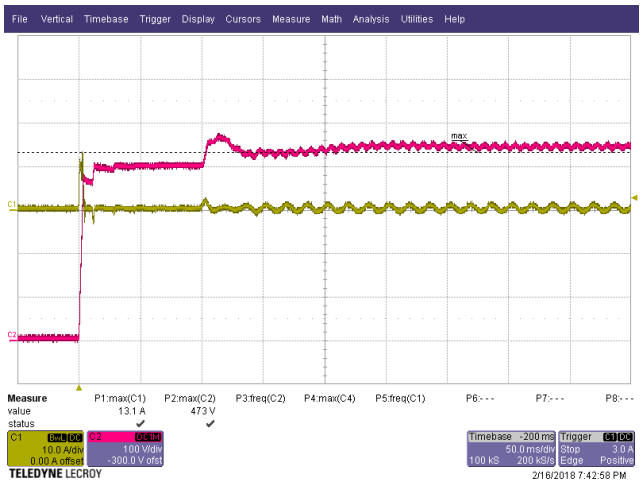

Figure 52 – AC Input Current vs. PFC Output Voltage at Start-up, Full Load, 277 VAC, 60 Hz.
Upper: AC Input Current, 10 A / div.
Lower: PFC Voltage, 100 V, 10 ms / div.

14.6 *LLC Start-up Waveforms Using Electronic Load Set for Constant Voltage*

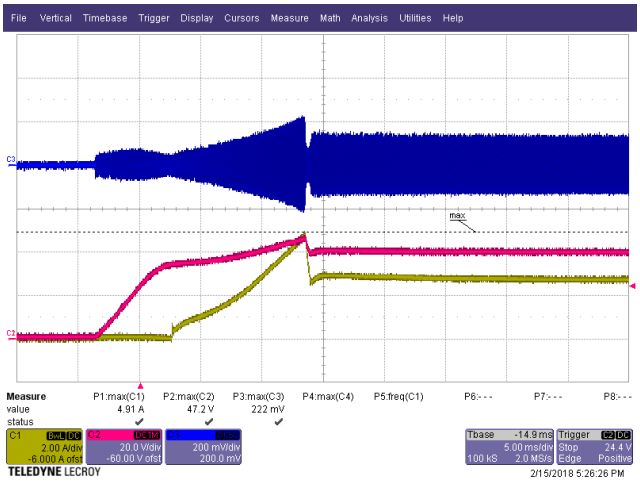

Figure 53 – LLC Start-up. 115 VAC, 100% Load, 32 V CV Load + 2.3 Ω Series Resistance (39 V).
Yellow: LLC I_{OUT}, 2 A / div.
Red: LLC V_{OUT}, 20 V / div.
Blue: LLC Primary Current, 200 mV (2 A), 5 ms / div.

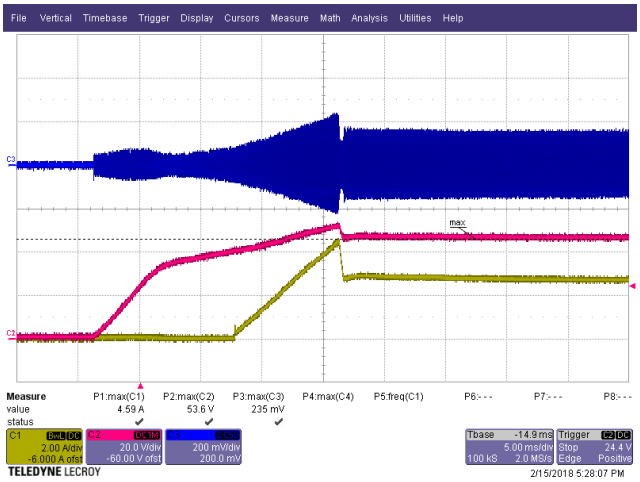

Figure 54 – LLC Start-up. 115 VAC, 100% Load, 39 V CV Load + 2.3 Ω Series Resistance (46 V).
Yellow: LLC I_{OUT}, 2 A / div.
Red: LLC V_{OUT}, 20 V / div.
Blue: LLC Primary Current, 200 mV (2 A), 5 ms / div.

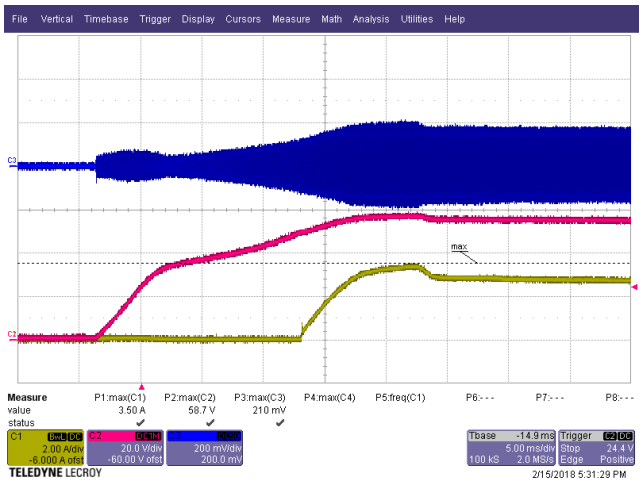

Figure 55 – LLC Start-up. 115 VAC, 100% Load, 47 V CV Load + 2.3 Ω Series Resistance (54 V).
Yellow: LLC I_{OUT}, 2 A / div.
Red: LLC V_{OUT}, 20 V / div.
Blue: LLC Primary Current, 200 mV (2 A), 5 ms / div.

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14.7 *Output Short-Circuit*

The figure below shows the effect of an output short circuit on the LLC primary current and on the output current. The UUT output was loaded with an electronic load configured for constant voltage, with a 2.3 Ω series resistor. Output voltage was set at 54 V for a worst-case load. The output lead to the electronic load and the lead connecting to the shorting relay were both bundled through the current probe used to sense the output current. The LLC primary current was monitored using a separate current probe. A mercury displacement relay was used to short the output to get a fast, bounce-free connection.

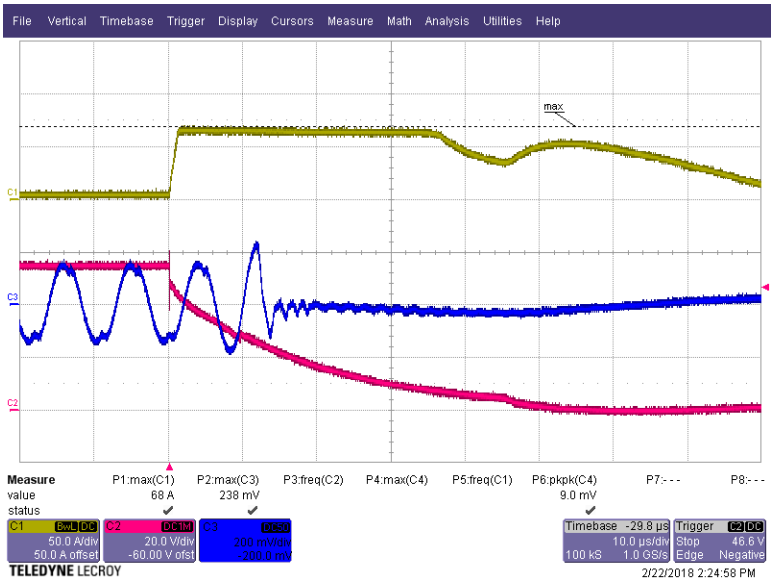

Figure 56 – Output Short-Circuit Test.
Upper: LLC Output Current, 50 A / div.
Middle: V_{OUT}, 20 V / div.
Lower: LLC Primary Current, 200 mV (2 A), 10 µs / div.

14.8 ***Output Ripple Measurements***

14.8.1 *Ripple Measurement Technique*

For DC output ripple measurements a modified oscilloscope test probe is used to reduce spurious signals. Details of the probe modification are provided in the figures below.

Tie two capacitors in parallel across the probe tip of the 4987BA probe adapter. A 0.1 μF / 100 V ceramic capacitor and 1.0 μF / 100 V aluminum electrolytic capacitor were used. The aluminum electrolytic capacitor is polarized, so always maintain proper polarity across DC outputs.

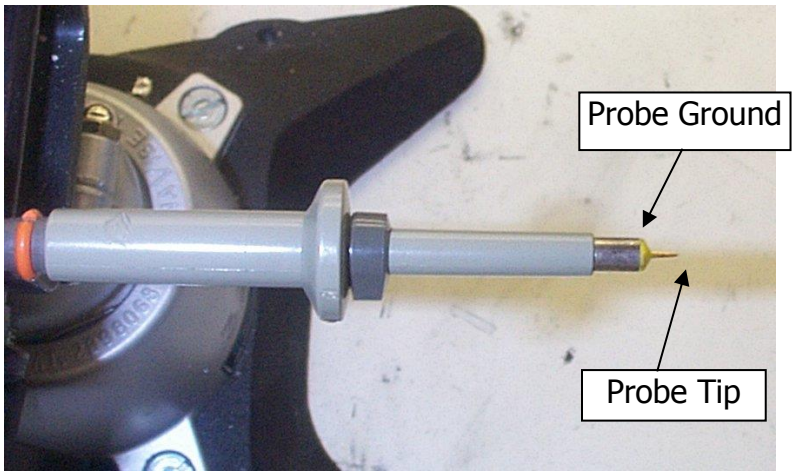

Figure 57 – Oscilloscope Probe Prepared for Ripple Measurement (End Cap and Ground Lead Removed).

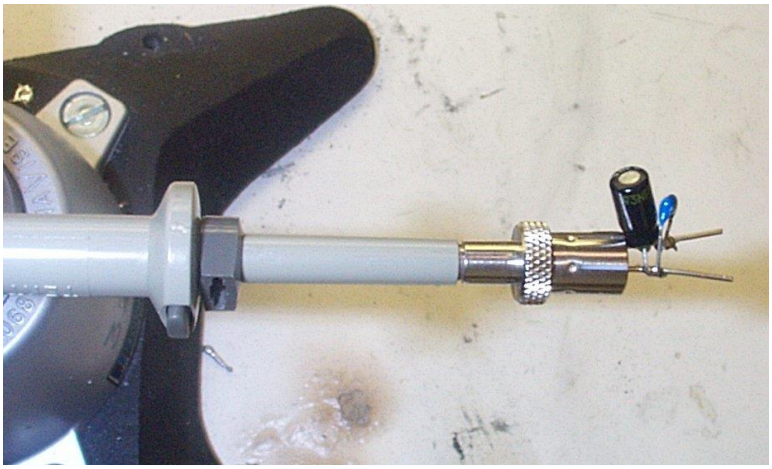

Figure 58 – Oscilloscope Probe with Probe Master 4987BA BNC Adapter (Modified with Wires for Probe Ground for Ripple measurement and Two Parallel Decoupling Capacitors Added).

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14.8.2 *Ripple Measurements*

The following pictures show output voltage and current ripple measures using an electronic load configured for constant voltage, with a 2.3 Ω series resistor to approximate the characteristics of an equivalent LED load. Measurements were taken at 54 V, 46 V, and 39 V output.

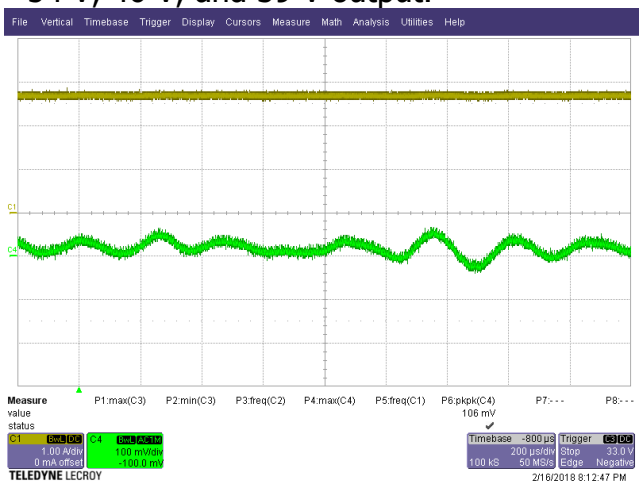

Figure 59 – Output Ripple, Full Load, 54 V_{OUT}, 115 VAC.
Upper: I_{OUT}, 1 A / div.
Lower: V_{OUT} Ripple, 100 mV, 200 µs / div.

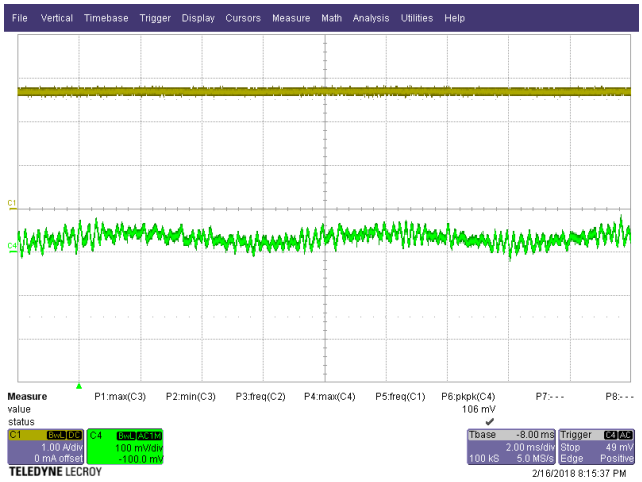

Figure 60 – Output Ripple, Full Load, 46 V_{OUT}, 115 VAC.
Upper: I_{OUT}, 1 A / div.
Lower: V_{OUT} Ripple, 100 mV, 2 ms / div.

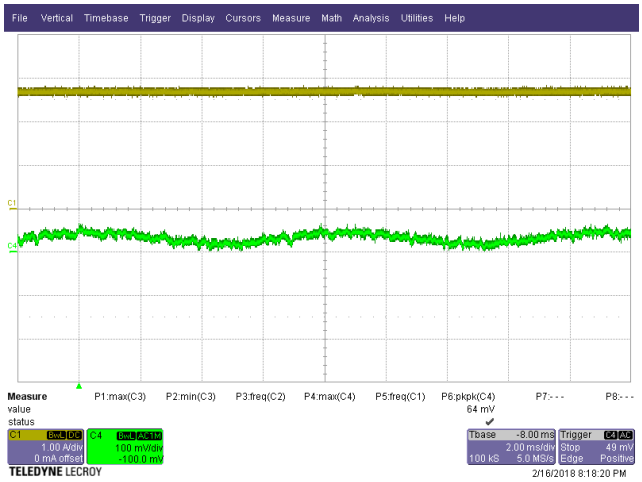

Figure 61 – Output Ripple, Full Load, 39 V_{OUT}, 115 VAC.
Upper: I_{OUT}, 1 A / div.
Lower: V_{OUT} Ripple, 100 mV, 2 ms / div.

15 Temperature Profiles

The board was operated at room temperature, with output set at the maximum 54 V, using a constant voltage load with additional 2.3 Ω series resistance. For each test condition the unit was allowed to thermally stabilize (~1 hr) before measurements were made.

15.1 *100 VAC, 50 Hz, 150 W Output, Room Temperature*

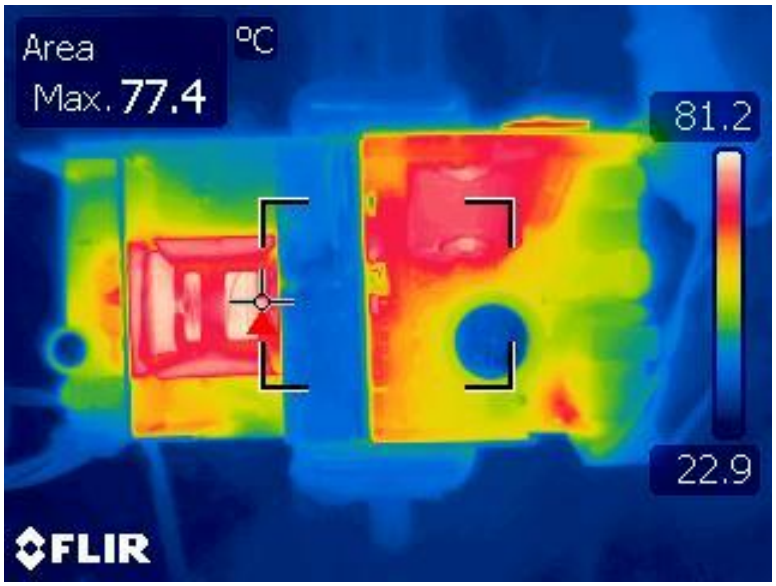

Figure 62 – Topside Thermal Picture, 100% Load, 100 VAC.

V_{IN}	Reference Designator	Temperature (°C)
100	U2	77.9
100	U4	82.1
100	D10, D11	81.5
100	D7	78
100	BR1	80.4
100	T1	79.9
100	T2	83.5

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15.2 *115 VAC, 60 Hz, 150 W Output, Room Temperature*

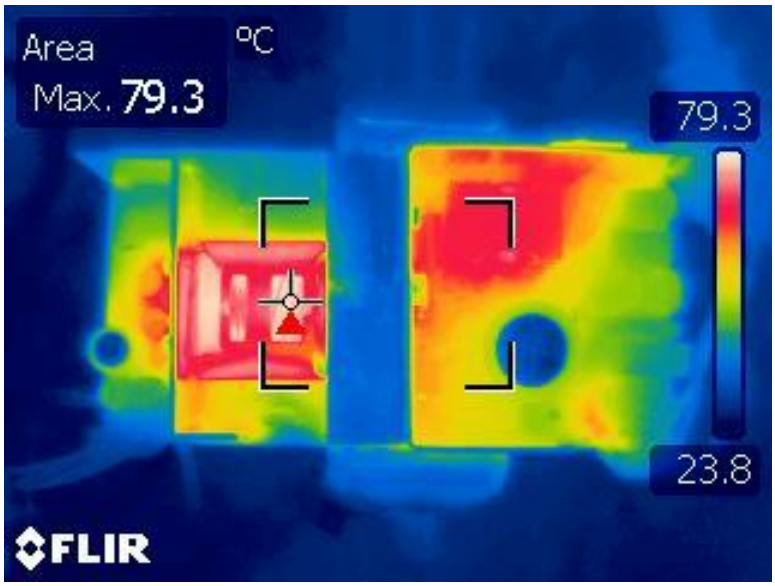

Figure 63 – Topside Thermal Picture, 100% Load, 115 VAC.

V_{IN}	Reference Designator	Temperature (°C)
115	U2	71.4
115	U4	74.5
115	D10, D11	80.1
115	D7	72
115	BR1	72.9
115	T1	73.1
115	T2	80.9

15.3 *230 VAC, 50 Hz, 150 W Output, Room Temperature*

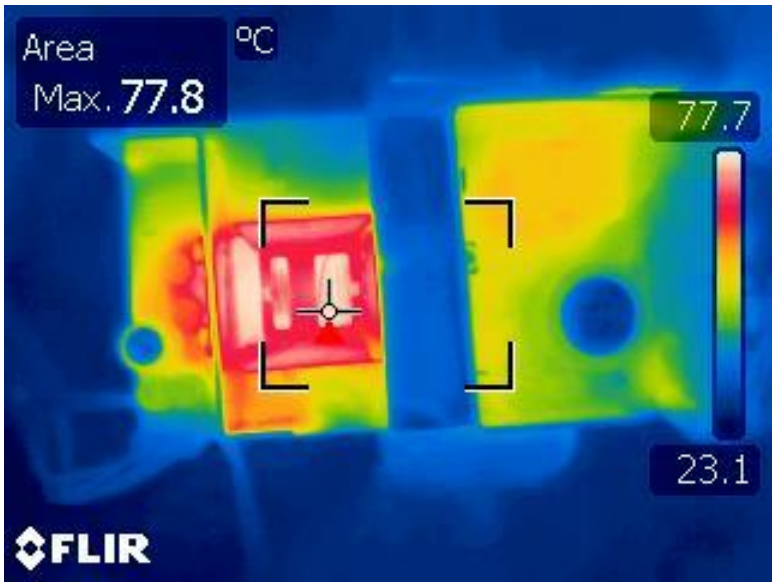

Figure 64 – Topside Thermal Picture, 100% Load, 230 VAC.

V_{IN}	Reference Designator	Temperature (°C)
230	U2	52.1
230	U4	60.3
230	D10, D11	80.2
230	D7	54.4
230	BR1	52.8
230	T1	51.4
230	T2	79.7

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15.4 *277 VAC, 60 Hz, 150 W Output, Room Temperature*

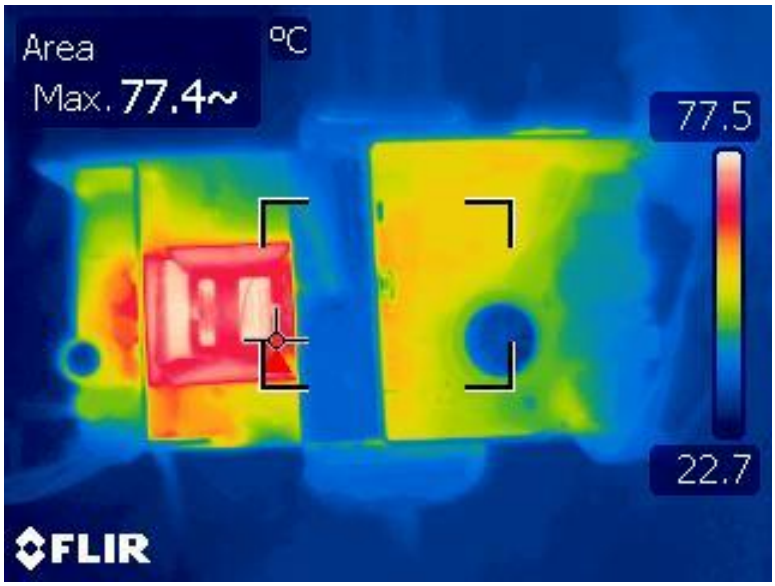

Figure 65 – Topside Thermal Picture, 100% Load, 277 VAC.

V_{IN}	Reference Designator	Temperature (°C)
277	U2	54.1
277	U4	62.3
277	D10, D11	79.5
277	D7	56.5
277	BR1	52.7
277	T1	48.3
277	T2	81

16 Conducted EMI

Conducted EMI tests used the LED load described in Section 7. The LED heat sink was connected to the LISN ground.

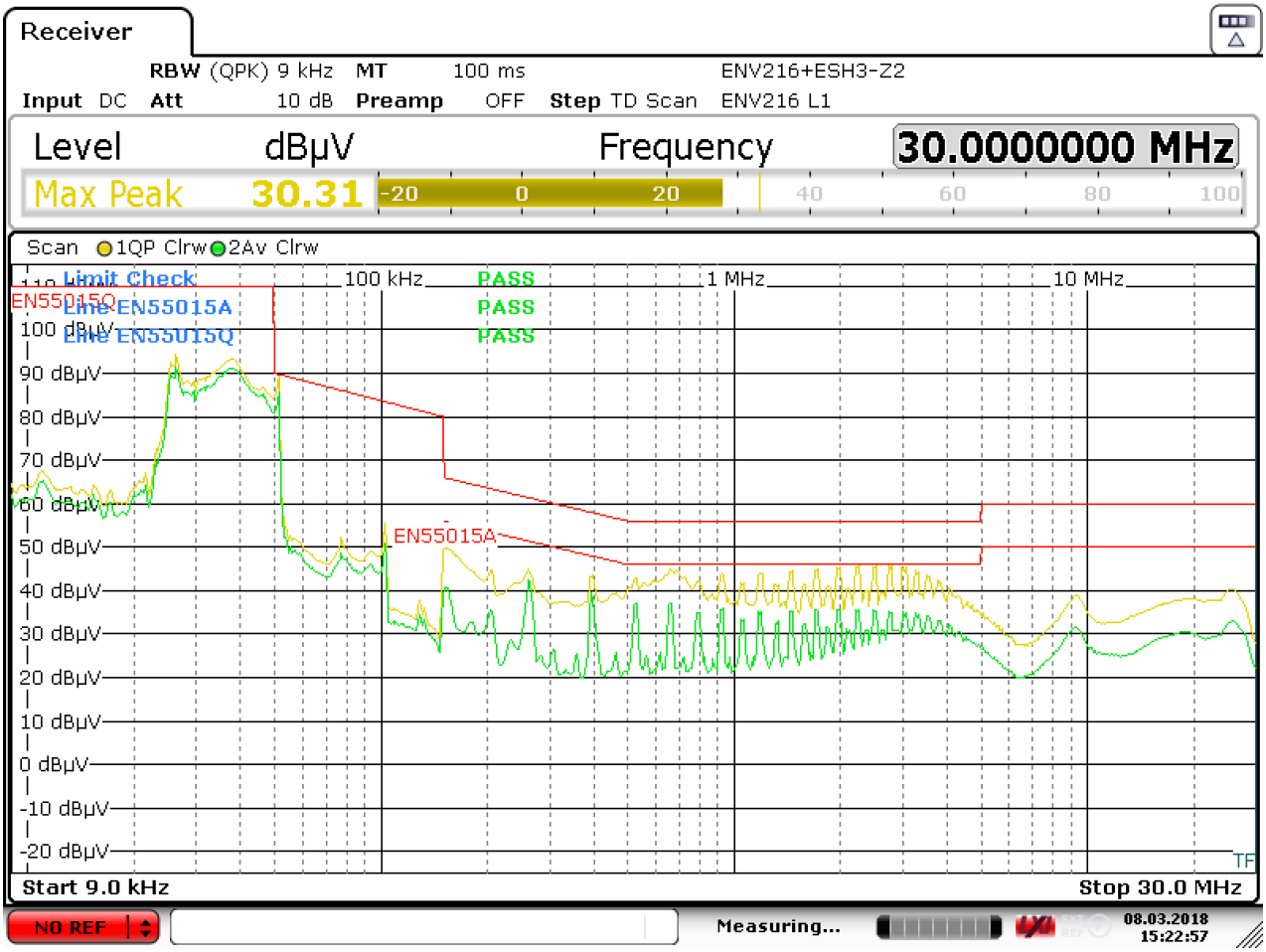

Figure 66 – Conducted EMI, 115 VAC, LED Load.

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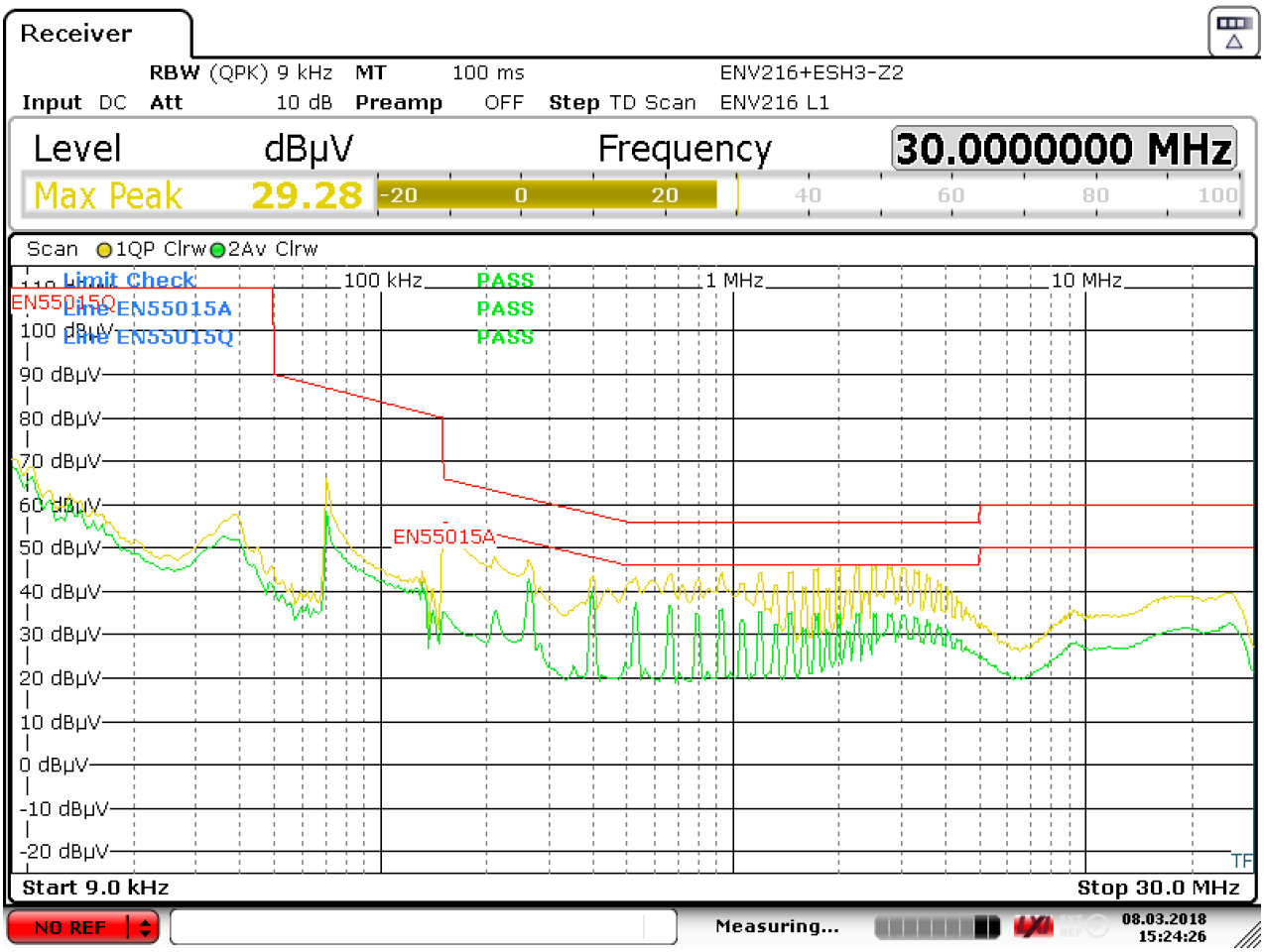

Figure 67 – Conducted EMI, 230 VAC, LED Load.

17 Line Surge Testing

17.1 *Line Surge Test Set-up*

The picture below shows the power supply set-up for surge testing. The supply is placed on a ground plane. A piece of single-sided copper clad printed circuit material was used in this case, but a piece of aluminum sheet with appropriate insulation would also work. An IEC AC connector was connected to the power supply AC input, with the safety ground connected to the ground plane. The CV output load (described in section 7) was placed on top of the ground plane so that it would capacitively couple to the safety ground. A 48 V fan powered by the UUT was located inside the plastic shroud shown in the figure, and used to cool the CV load during testing. The LED string used in the CV load was used as an output indicator, and to sense any output voltage dropout.

The UUT was tested using a Teseq NSG 3060 surge tester. Results of common mode and differential mode surge testing are shown below. A test failure was defined as a non-recoverable output interruption requiring supply repair or recycling AC input voltage.

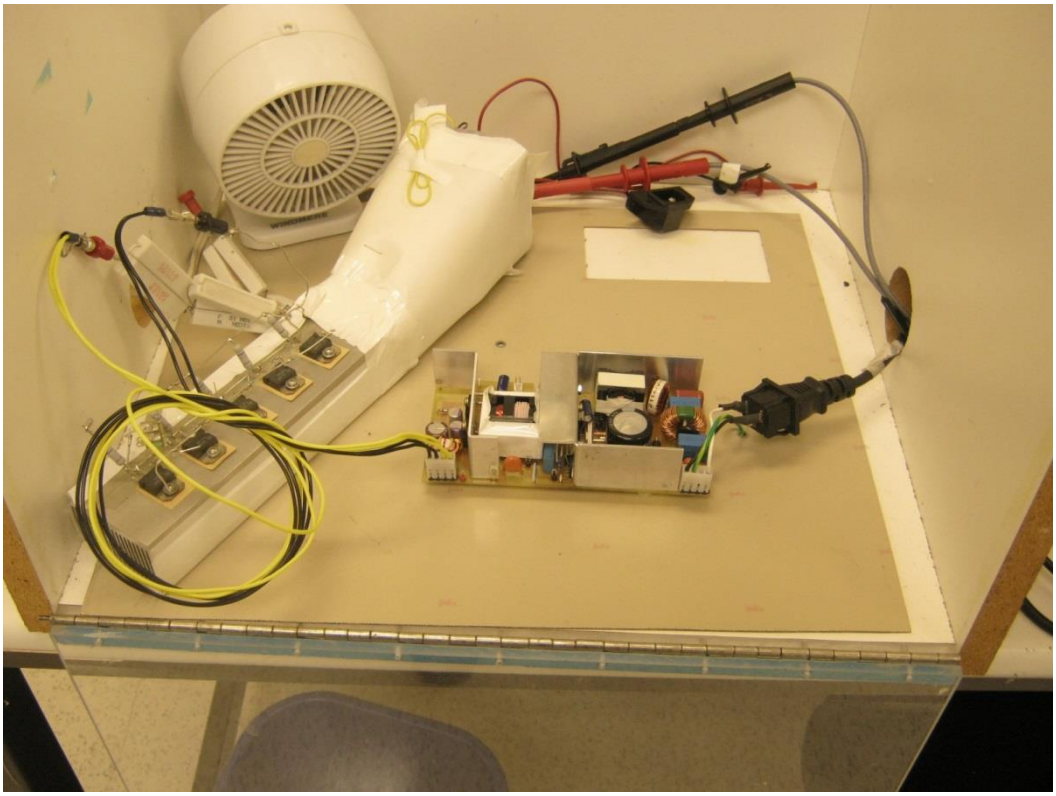

Figure 68 – Line Surge Physical Set-up.

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17.2 *Differential Mode Surge, 1.2 / 50 μsec*

AC Input Voltage (VAC)	Surge Voltage (kV)	Phase Angle (º)	Generator Impedance (Ω)	Number of Strikes	Test Result
115	+4	90	2	10	PASS
115	-4	90	2	10	PASS
115	+4	270	2	10	PASS
115	-4	270	2	10	PASS
115	+4	0	2	10	PASS
115	-4	0	2	10	PASS

AC Input Voltage (VAC)	Surge Voltage (kV)	Phase Angle (º)	Generator Impedance (Ω)	Number of Strikes	Test Result
230	+4	90	2	10	PASS
230	-4	90	2	10	PASS
230	+4	270	2	10	PASS
230	-4	270	2	10	PASS
230	+4	0	2	10	PASS
230	-4	0	2	10	PASS

17.3 *Common Mode Surge, 1.2 / 50 μsec*

AC Input Voltage (VAC)	Surge Voltage (kV)	Phase Angle (º)	Generator Impedance (Ω)	Number of Strikes	Test Result
115	+4	90	12	10	PASS
115	-4	90	12	10	PASS
115	+4	270	12	10	PASS
115	-4	270	12	10	PASS
115	+4	0	12	10	PASS
115	-4	0	12	10	PASS

AC Input Voltage (VAC)	Surge Voltage (kV)	Phase Angle (º)	Generator Impedance (Ω)	Number of Strikes	Test Result
230	+4	90	12	10	PASS
230	-4	90	12	10	PASS
230	+4	270	12	10	PASS
230	-4	270	12	10	PASS
230	+4	0	12	10	PASS
230	-4	0	12	10	PASS

18 Revision History

Date	Author	Revision	Description and Changes	Reviewed
07-May-18	RH	1.0	Initial Release	Apps & Mktg
07-Mar-20	KM	1.1	Added Alternates for C13 and Q2, Q4, Q5.	Apps & Mktg
30-Jul-20	KM	1.2	Converted to RDR.	Apps & Mktg
31-Aug-20	KM	1.3	Updated Figure 33.	Apps & Mktg
02-Sep-20	RH	1.4	Spec Table Update.	Apps & Mktg

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