# Design Example Report

| | |
|---|---|
| **Title** | ***0.25 W Non-Isolated Power Supply Without Electrolytic Capacitors Using LinkSwitch™-TNZ LNK3302D*** |
| **Specification** | 90 VAC – 132 VAC Input, 5 V, 50 mA Output |
| **Application** | Home and Building Automation |
| **Author** | Applications Engineering Department |
| **Document Number** | DER-971 |
| **Date** | January 23, 2023 |
| **Revision** | 1.0 |

## Summary and Features

- Highly integrated solution with LNK3302D
- No electrolytic capacitors
- Very wide ambient temperature operating range -40 to 70 °C
- Optimized for low audible noise <25 dB
- Low component count with integrated 725 V power MOSFET, current sensing and protection
- <120 μA standby input current across AC line
- Zero-crossing signal output synchronized to AC line
- Meets EN550022 conducted EMI
- Compact solution 1" x 1.20", 11 mm maximum height
- Load short-circuit protection



**Power Integrations**
5245 Hellyer Avenue, San Jose, CA 95138 USA.
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

# Table of Contents

**Important Note:** Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

# 1 Introduction

This engineering report describes a high-side buck converter designed to provide a nominal output voltage of 5 V at 50 mA load from a low-line input voltage range of 90 VAC to 132 VAC, as well as a zero-crossing detection (ZCD) signal. This power supply utilizes the LNK3302D from the LinkSwitch-TNZ family of ICs.

This document contains the complete power supply specifications, bill of materials, circuit schematic and printed circuit board layout, along with performance data and electrical waveforms.

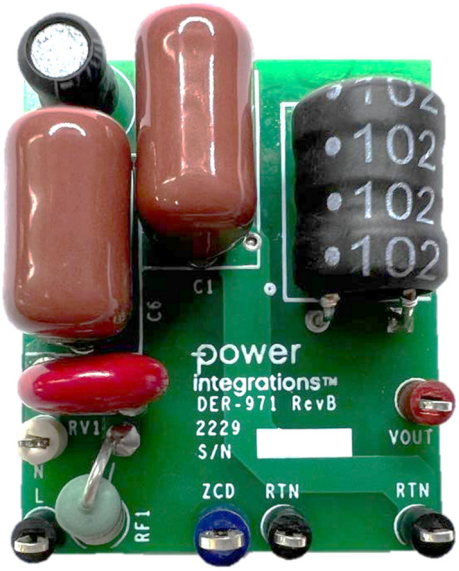


**Figure 1 –** Populated Circuit Board, Top View.

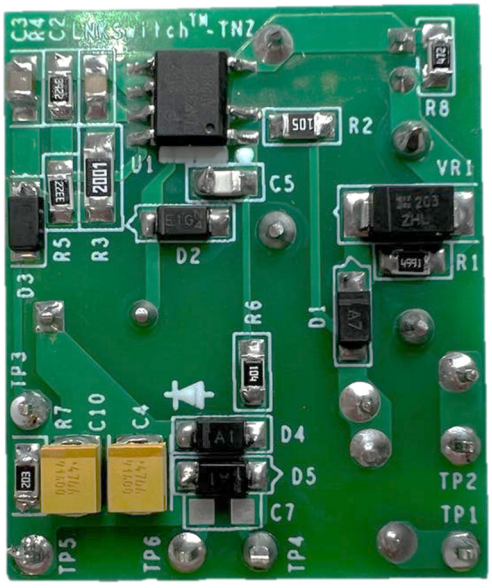


**Figure 2 –** Populated Circuit Board, Bottom View.

# 2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

| Description | Symbol | Min | Typ | Max | Units | Comment |
|---|---|---|---|---|---|---|
| **Input** | | | | | | |
| Voltage | $V_{IN}$ | 90 | | 132 | VAC | 2 Wire – no P.E. |
| Frequency | $f_{LINE}$ | 47 | 50/60 | 64 | Hz | |
| No-load Input Current | | | 113 | | μA | 115 VAC. |
| **Output** | | | | | | |
| Output Voltage | $V_{OUT}$ | | 5 | | V | ± 5%. |
| Output Current | $I_{OUT}$ | | 0.05 | | A | |
| **Total Output Power** | | | | | | |
| Continuous Output Power | $P_{OUT}$ | | 0.25 | | W | |
| **Efficiency** | | | | | | |
| Full Load | η | 66 | | | % | Measured at $P_{OUT}$ 25 °C. |
| **Environmental** | | | | | | |
| Conducted EMI | | Meets CISPR22B / EN55022B | | | | |
| Safety | | Designed to meet IEC 60950-1 | | | | |
| Surge | | | 1 | | kV | 1.2/50 μs surge, IEC 1000-4-5, Series Impedance: Surge: 2 Ω |
| Ring Wave | | | 2.5 | | kV | Ring Wave: 12 Ω |

# 3 Schematic

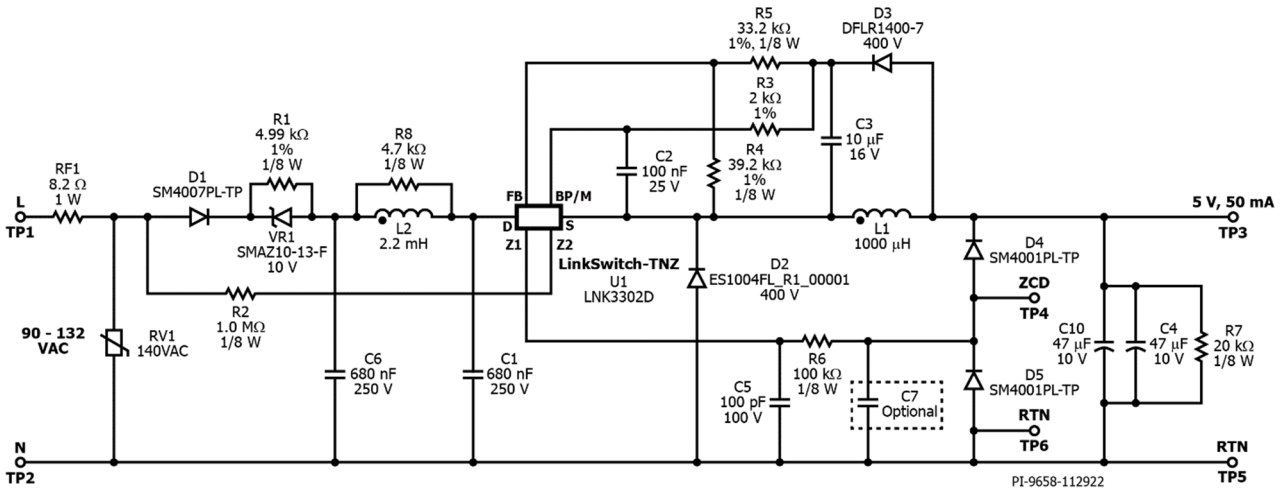


**Figure 3 –** Schematic.

# 4 Circuit Description

This circuit is configured as a high-side buck topology power supply utilizing the LNK3302D.

## *4.1 Input Rectifier and Filter*

The AC input voltage is half-wave rectified by a single diode D1. To correctly measure the zero-crossing signal, a single diode connection is recommended over putting the additional diode on the neutral line.

The rectified DC is then filtered by the bulk storage capacitors C1 and C6. For outdoor applications where operating temperatures are higher, a replacement for C1 and C6 is suggested in the bill of materials section under optional parts. Inductor L2, C1 and C6 form an input pi filter, which attenuates differential mode conducted EMI. The damping resistor R8 reduces the Q factor of the inductor L2 to allow noise filtering more effective at wider bandwidth.

## *4.2 Input Protection*

The fusible resistor RF1 provides safety protection against catastrophic circuit failures. It also reduces inrush current at start-up. Varistor RV1 protects against surge events.

## *4.3 Power Factor Circuit*

Power Integrations' RZ circuit, that is resistor R1 and Zener diode VR1, minimizes the no-load input current that is important in many 2-wire switch or dimmer applications. Zener diode VR1 is rated 1 W with a 10 V clamping voltage. Higher Zener voltage may reduce no-load input current further, but it might cause higher power dissipation during surge. Resistor R1 is tuned either at no-load or at standby, whichever is applicable. The resistance is set such as its peak voltage is just below the Zener voltage. This yields the lowest input current.

## *4.4 LNK3302D Power Supply Operation*

The LinkSwitch-TNZ IC combines a high-voltage power MOSFET switch, a power supply controller, and a Zero Crossing Detector in a single device. Unlike conventional PWM (pulse width modulator) controllers, the LinkSwitch-TNZ IC uses a simple ON/OFF control to regulate the output voltage. The LinkSwitch-TNZ controller consists of an oscillator, feedback (sense and logic) circuit, 5 V regulator, BYPASS pin undervoltage circuit, over-temperature protection, line and output overvoltage protection, frequency jittering, current limit circuit, leading edge blanking and a 725 V power MOSFET.

This design is configured as a high-side buck converter using U1 LNK3302D. At AC start-up, the device starts switching once the BYPASS (BP/M) pin voltage charges to $V_{BP}$. A 100 nF capacitor C2 connected to BP sets the current limit to standard.

When the power MOSFET turns ON, current flows to the load via inductor L1. Energy is stored in the inductor, and the output capacitors C4 and C10 gets charged. When the

MOSFET turns OFF, the stored energy from L1 is released to the load via free-wheeling diode D2. The charge stored in C4 and C10 supplies the current until the next switching event occurs. An internal current source attached to the DRAIN (D) pin charges C2 to provide power to the IC's controller. Once the output voltage has been set, the device controller will be powered from the output via a feedback diode D3 and a current-limiting resistor R3 to reduce losses.

### *4.5 Feedback and Output Voltage Regulation*

In this high-side buck, direct feedback configuration, the rectified voltage across L1 via D3 and C3 tracks the output voltage. Resistors R3 and R4 divides the voltage such that the FB pin is set to 2 V. When the current delivered into this pin exceeds $I_{FB}$ (49 μA), a low logic level (disable) is generated at the output of the feedback circuit. This output is sampled at the beginning of each cycle on the rising edge of the clock signal. If high, the power MOSFET is turned on for that cycle (enabled), otherwise the power MOSFET remains off (disabled). The current limit circuit senses the current in the power MOSFET. When this current exceeds the internal threshold ($I_{LIMIT}$), the power MOSFET is turned off for the remainder of that cycle.

Regulation is maintained by skipping switching cycles. As the output voltage rises, the current into the FEEDBACK pin will rise. If this exceeds $I_{FB}$ then subsequent cycles will be skipped until the current reduces below $I_{FB}$. Thus, as the output load is reduced, more cycles will be skipped and if the load increases, fewer cycles are skipped.

A small pre-load R7 is required to limit the output voltage to about 110% of the rated voltage during light load or no-load condition.

### *4.6 Zero-Crossing Detection*

The Z1 and Z2 pins are configured to provide a loss-less (<5 mW) zero-crossing detection (ZCD) circuit. Z2 is connected to one of the input AC lines through resistor R2 while Z1 forms the ZCD signal output.

When the AC voltage is more positive with respect to Neutral, D4 is forward-biased and clamps ZCD output to $V_{OUT}$ + 0.7 V. At the negative-going phase of the AC input, D5 is forward-biased and clamps ZCD output to -0.7 V.

The passive components comprised of R2, C5, R6, and optional C7 provide noise filtering to ensure clean ZCD signal. C7 is a placeholder for the additional filter if needed. Diode D5 has capacitance that helps avoid adding the extra capacitor. However, too much capacitance will cause more delay.

# 5 PCB Layout

| | |
|---|---|
| Number of layers: | 2 |
| PCB Board thickness: | 1.59 mm / 0.062 inches |
| Material: | FR4 |
| Copper thickness: | 2 oz |

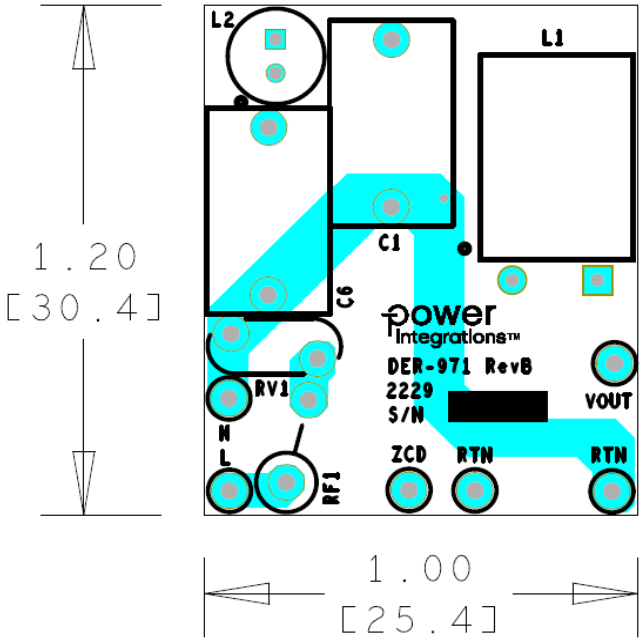


**Figure 4 –** Populated Circuit Board, Top View.

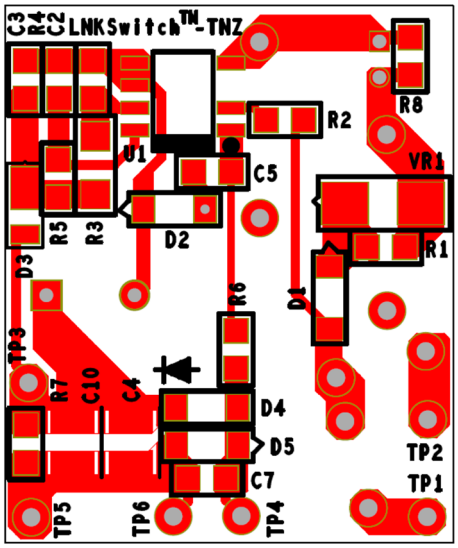


**Figure 5 –** Populated Circuit Board, Bottom View.

# 6 Bill of Materials

## 6.1 Electrical Parts

| Item | Qty | Ref Des | Description | Mfg Part Number | Mfg |
|---|---|---|---|---|---|
| 1 | 1 | C1 | 0.68 µF Film 125V 250V Polyester, Metallized Radial, (12.30 mm x 7.30 mm) | ECQ-E2684KB | Panasonic |
| 2 | 1 | C2 | 100 nF, 25 V, Ceramic, X7R, 0805 | 08053C104KAT2A | AVX |
| 3 | 1 | C3 | 10 µF, ±10%, 16V, X7R, Ceramic, SMT, MLCC 0805 | CL21B106KOQNNNE | Samsung |
| 4 | 1 | C4 | 47 µF, Molded Tantalum, 10 V, 1411, 1210, 250 mΩ | TPSB476K010R0250 | AVX |
| 5 | 1 | C5 | 100 pF, 100 V, Ceramic, COG, 0805 | C0805C101J1GACTU | Kemet |
| 6 | 1 | C6 | 0.68 µF Film 125V 250V Polyester, Metallized Radial, (12.30mm x 7.30mm) | ECQ-E2684KB | Panasonic |
| 7 | 1 | C10 | 47 µF, Molded Tantalum, 10 V, 1411, 1210, 250 mΩ | TPSB476K010R0250 | AVX |
| 8 | 1 | D1 | 1000V, 1 A, Standard Recovery, SOD-123FL | SM4007PL-TP | Micro Commercial |
| 9 | 1 | D2 | Diode, Standard, 400 V, 1A, SMT SOD-123FL | ES1004FL_R1_00001 | Panjit |
| 10 | 1 | D3 | 400 V, 1 A, Rectifier, Glass Passivated, POWERDI123 | DFLR1400-7 | Diodes, Inc. |
| 11 | 1 | D4 | Diode, GEN PURP, 50 V, 1 A, SOD-123F, SOD123FL | SM4001PL-TP | Micro Commercial |
| 12 | 1 | D5 | Diode, GEN PURP, 50 V, 1 A, SOD-123F, SOD123FL | SM4001PL-TP | Micro Commercial |
| 13 | 1 | L1 | 1000 µH, 0.510 A | RLB9012-102KL | Bourns |
| 14 | 1 | L2 | 2.2 mH, 0.046 A, 20% | RL-5480-1-2200 | Renco |
| 15 | 1 | R1 | RES, 4.99 kΩ, 1%, 1/8 W, Thick Film, 0805 | ERJ-6ENF4991V | Panasonic |
| 16 | 1 | R2 | RES, 1.0 MΩ, 5%, 1/8 W, Thick Film, 0805 | ERJ-6GEYJ105V | Panasonic |
| 17 | 1 | R3 | RES, 2 kΩ, 1%, 1/4 W, Thick Film, 1206 | ERJ-8ENF2001V | Panasonic |
| 18 | 1 | R4 | RES, 39.2 kΩ, 1%, 1/8 W, Thick Film, 0805 | ERJ-6ENF3922V | Panasonic |
| 19 | 1 | R5 | RES, 33.2 kΩ, 1%, 1/8 W, Thick Film, 0805 | ERJ-6ENF3322V | Panasonic |
| 20 | 1 | R6 | RES, 100 kΩ, 5%, 1/8 W, Thick Film, 0805 | ERJ-6GEYJ104V | Panasonic |
| 21 | 1 | R7 | RES, 20 kΩ, 5%, 1/8 W, Thick Film, 0805 | ERJ-6GEYJ203V | Panasonic |
| 22 | 1 | R8 | RES, 4.7 kΩ, 5%, 1/8 W, Thick Film, 0805 | ERJ-6GEYJ472V | Panasonic |
| 23 | 1 | RF1 | RES, 8.2 Ω, 1 W, 5%, Fusible/Flame Proof Wire Wound | FKN1WSJR-52-8R2 | Yageo |
| 24 | 1 | RV1 | 140 VAC, 12 J, 7 mm, RADIAL | V140LA2P | Littlefuse |
| 25 | 1 | U1 | LinkSwitch-TNZ, SO8 | LNK3302D | Power Integrations |
| 26 | 1 | VR1 | Diode, ZENER, 10 V, ±5%, 1 W, DO-214AC, SMA | SMAZ10-13-F | Diodes, Inc. |

## 6.2 Optional Part

| Item | Qty | Ref Des | Description | Mfg Part Number | Mfg |
|---|---|---|---|---|---|
| 1 | 1 | C7 | 100 pF, 100 V, Ceramic, COG, 0805 | C0805C101J1GACTU | Kemet |
| 2 | 2 | C1 C6 | 0.68 µF Film 160 V 250 V Polyester (55 °C ~ 125 °C) (18.00 mm x 7.00 mm) | B32522C3684K189 | EPCOS |

## 6.3 Mechanical Parts

| Item | Qty | Ref Des | Description | Mfg Part Number | Mfg |
|---|---|---|---|---|---|
| 1 | 1 | TP1 | Test Point, BLK, Miniature THRU-HOLE MOUNT | 5001 | Keystone |
| 2 | 1 | TP2 | Test Point, WHT, Miniature THRU-HOLE MOUNT | 5002 | Keystone |
| 3 | 1 | TP3 | Test Point, RED, Miniature THRU-HOLE MOUNT | 5000 | Keystone |
| 4 | 1 | TP4 | Test Point, BLUE, Miniature THRU-HOLE MOUNT | 5117 | Keystone |
| 5 | 1 | TP5 | Test Point, BLK, Miniature THRU-HOLE MOUNT | 5001 | Keystone |
| 6 | 1 | TP6 | Test Point, BLK, Miniature THRU-HOLE MOUNT | 5001 | Keystone |

# 7 Design Spreadsheet

| 1 | ACDC_LinkSwitchTNZ_Buck_052621; Rev.1.0; Copyright Power Integrations 2021 | INPUT | INFO | OUTPUT | UNIT | ACDC LinkSwitch-TNZ Buck |
|---|---|---|---|---|---|---|
| **2** | **ENTER APPLICATION VARIABLES** | | | | | |
| 3 | LINE VOLTAGE RANGE | | | Custom | | AC line voltage range |
| 4 | VACMIN | 90.00 | | 90.00 | V | Minimum AC line voltage |
| 5 | VACMAX | 132.00 | | 132.00 | V | Maximum AC line voltage |
| 6 | fL | 60.00 | | 60.00 | Hz | AC mains frequency |
| 7 | LINE RECTIFICATION TYPE | H | | H | | Line rectification type: select "F" if full wave rectification or "H" if half wave rectification |
| 8 | VOUT | 5.00 | | 5.00 | V | Output voltage |
| 9 | IOUT | 0.050 | | 0.050 | A | Average output current |
| 10 | EFFICIENCY_ESTIMATED | | | 0.80 | | Efficiency estimate at output terminals |
| 11 | EFFICIENCY_CALCULATED | | | 0.69 | | Calculated efficiency based on real components and operating point |
| 12 | POUT | | | 0.25 | W | Continuous output power |
| 13 | CIN | | | 1.50 | uF | Input capacitor |
| 14 | VMIN | | | 90.6 | V | Valley voltage of the rectified minimum AC line voltage |
| 15 | VMAX | | | 186.7 | V | Peak voltage of the maximum AC line voltage |
| 16 | INPUT STAGE RESISTANCE | | | 10 | Ohms | Input stage resistance in ohms (includes thermistor, filtering components, etc) |
| 17 | PLOSS_INPUTSTAGE | | | 0.000 | W | Maximum input stage loss |
| **21** | **ENTER LINKSWITCH-TNZ VARIABLES** | | | | | |
| 22 | OPERATION MODE | | | MDCM | | Mostly continuous mode of operation |
| 23 | CURRENT LIMIT MODE | STD | | STD | | Choose 'RED' for reduced current limit or 'STD' for standard current limit |
| 24 | PACKAGE | NO | | NO | | Select the device package |
| 25 | DEVICE SERIES | | | SO-8C | | Generic LinkSwitch-TNZ device |
| 26 | DEVICE CODE | LNK3302 | | LNK3302 | | Required LinkSwitch-TNZ device |
| 27 | ILIMITMIN | | | LNK3302D | A | Minimum current limit of the device |
| 28 | ILIMITTYP | | | 0.126 | A | Typical current limit of the device |
| 29 | ILIMITMAX | | | 0.136 | A | Maximum current limit of the device |
| 30 | RDSON | | | 0.146 | ohms | Primary switch on-time drain to source resistance at 100degC |
| 31 | FSMIN | | | 88.40 | Hz | Minimum switching frequency |
| 32 | FSTYP | | | 62000 | Hz | Typical switching frequency |
| 33 | FSMAX | | | 66000 | Hz | Maximum switching frequency |
| 34 | BVDSS | | | 725 | V | Device breakdown voltage |
| **38** | **SWITCH PARAMETERS** | | | | | |
| 39 | VDSON | | | 2.00 | V | Switch on-time drain to source voltage estimate |
| 40 | VDSOFF | | | 196.0 | V | Switch off-time drain-to-source voltage stress |
| 41 | DUTY | | | 0.050 | | Maximum duty cycle |
| 42 | TIME_ON_MIN | | | 0.717 | us | Switch minimum on-time |
| 43 | IPED_SWITCH | | | 0.000 | A | Maximum switch pedestal current |
| 44 | IRMS_SWITCH | | | 0.018 | A | Maximum switch RMS current |
| 45 | PLOSS_SWITCH | | | 0.048 | W | Maximum switch loss |
| 46 | THERMAL RESISTANCE OF SWITCH | | | 100 | degC/W | Net thermal resistance of the switch |
| 47 | T_RISE_SWITCH | | | 4.8 | degC | Maximum temperature rise of the switch in degrees Celsius |
| **51** | **BUCK INDUCTOR PARAMETERS** | | | | | |
| 52 | INDUCTANCE_MIN | | | 900 | uH | Minimum design inductance required for current delivery |
| 53 | INDUCTANCE_TYP | AUTO | | 1000 | uH | Typical design inductance required for current delivery |
| 54 | INDUCTANCE_MAX | | | 1100 | uH | Maximum design inductance required for current delivery |
| 55 | TOLERANCE_INDUCTANCE | | | 10 | % | Tolerance of the design inductance |

| | | | | | | |
|---|---|---|---|---|---|---|
| 56 | DC RESISTANCE OF INDUCTOR | | | 2.0 | ohms | DC resistance of the buck inductor |
| 57 | FACTOR_KLOSS | | | 0.50 | | Factor that accounts for "off-state" power loss to be supplied by inductor (usually between 50% to 66%) |
| 58 | IRMS_INDUCTOR | | | 0.077 | A | Maximum inductor RMS current |
| 59 | PLOSS_INDUCTOR | | | 0.012 | W | Maximum inductor losses |
| **63** | **FREEWHEELING DIODE PARAMETERS** | | | | | |
| 64 | VF_FREEWHEELING | | | 0.70 | V | Forward voltage drop across the freewheeling diode |
| 65 | PIV_RATING | | | 400.0 | V | Peak inverse voltage rating of the freewheeling diode |
| 66 | TRR | | | 75 | ns | Reverse recovery time of the freewheeling diode |
| 67 | PIV_CALCULATED | | | 233.3 | V | Computed peak inverse voltage across the freewheeling diode |
| 68 | IRMS_DIODE | | | 0.076 | A | Maximum diode RMS current |
| 69 | PLOSS_DIODE | | | 0.061 | W | Maximum freewheeling diode loss |
| 70 | RECOMMENDED DIODE | | | MUR140 | | Recommended freewheeling diode |
| **74** | **BIAS/FEEDBACK PARAMETERS** | | | | | |
| 75 | VF_BIAS | | | 0.70 | V | Forward voltage drop of the bias diode |
| 76 | RBIAS | 39200 | | 39200 | Ohms | Bias resistor (connected across FB and S pin). Results into IFB_BIAS value of 49.751 uA |
| 77 | RBP | | | N/A | Ohms | BP pin resistor |
| 78 | CBP | | | 0.1 | uF | BP pin capacitor |
| 79 | RFB | | | 30100 | Ohms | Feedback resistor |
| 80 | CFB | | | 10 | uF | Feedback capacitor |
| 81 | C_SOFTSTART | | | N/A | uF | No soft-start capacitor required |
| 82 | PLOSS_FEEDBACK | | | 0.000 | W | Maximum feedback component losses |
| **86** | **X-CAPACITOR DISCHARGE COMPONENTS** | | | | | |
| 87 | XCAP REQUIRED | NO | | NO | | Select whether an X-capacitor is required or not |
| 88 | XCAP | | | N/A | nF | X-capacitor in the input |
| 89 | TOLERANCE_RZ | 0.05 | | N/A | | Tolerance of the X-capacitor discharge resistors |
| 90 | RZ1 | | | N/A | MOhms | X-capacitor discharge resistor connected from the input line to Z1 pin of LinkSwitch-TNZ device |
| 91 | RZ2 | | | N/A | MOhms | X-capacitor discharge resistor connected from the input neutral to Z2 pin of LinkSwitch-TNZ device |
| 92 | t_XCAP_DISCHARGE | | | N/A | sec | Actual time (worst-case) to discharge the X-capacitor to 60 V after AC input disconnection |
| **96** | **OUTPUT CAPACITOR** | | | | | |
| 97 | OUTPUT VOLTAGE RIPPLE | | | 100 | mV | Desired output voltage ripple |
| 98 | IRMS_COUT | | | 0.059 | A | Maximum output capacitor RMS current |
| 99 | PLOSS_COUT | | | 0.003 | W | Maximum output capacitor power loss |
| 100 | ESR_COUT | | | 778 | mOhms | ESR of the output capacitor |

# 8 Performance Data

## *8.1 Efficiency*

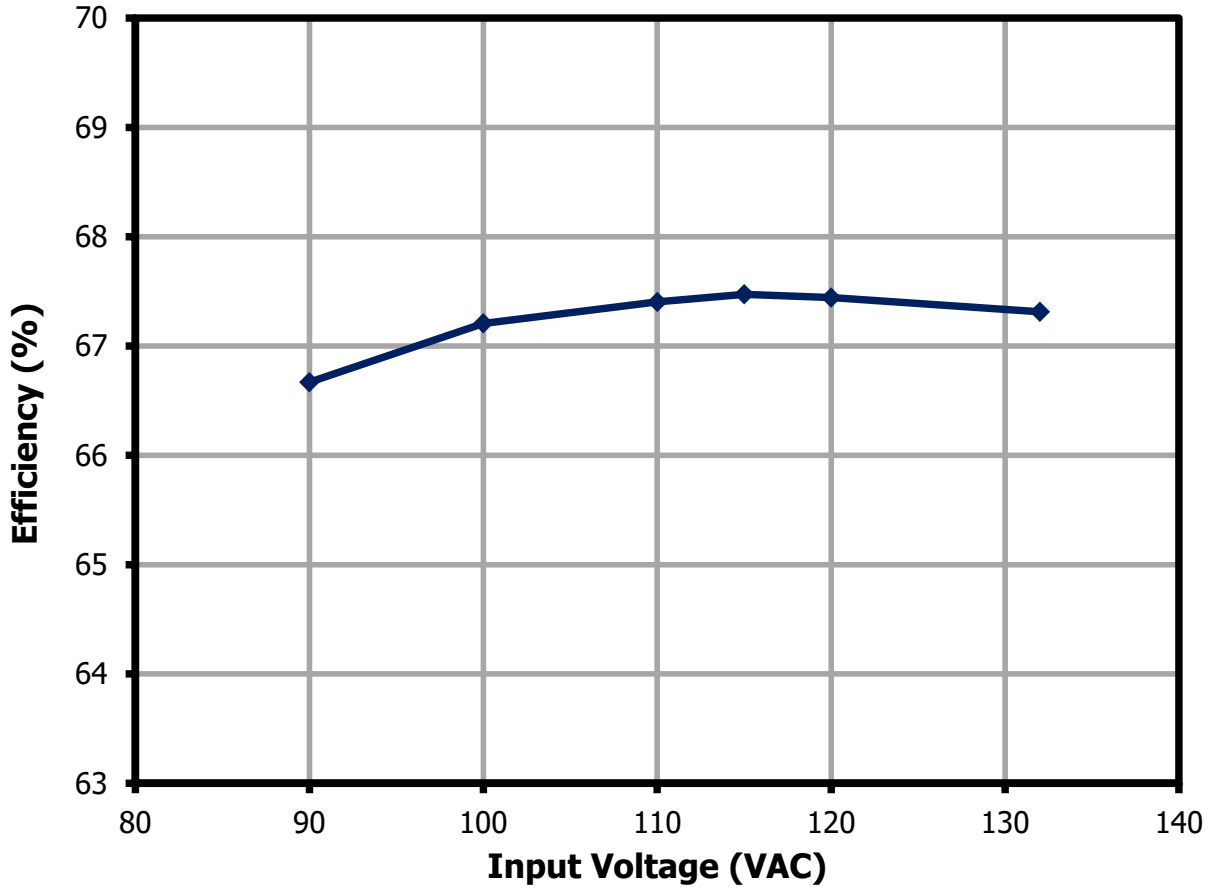


**Figure 6 –** Full Load Efficiency vs. Line.

### *8.2 No-Load Input Current*

Test Condition: Soak for 5 minutes each line and use Fluke DMM.

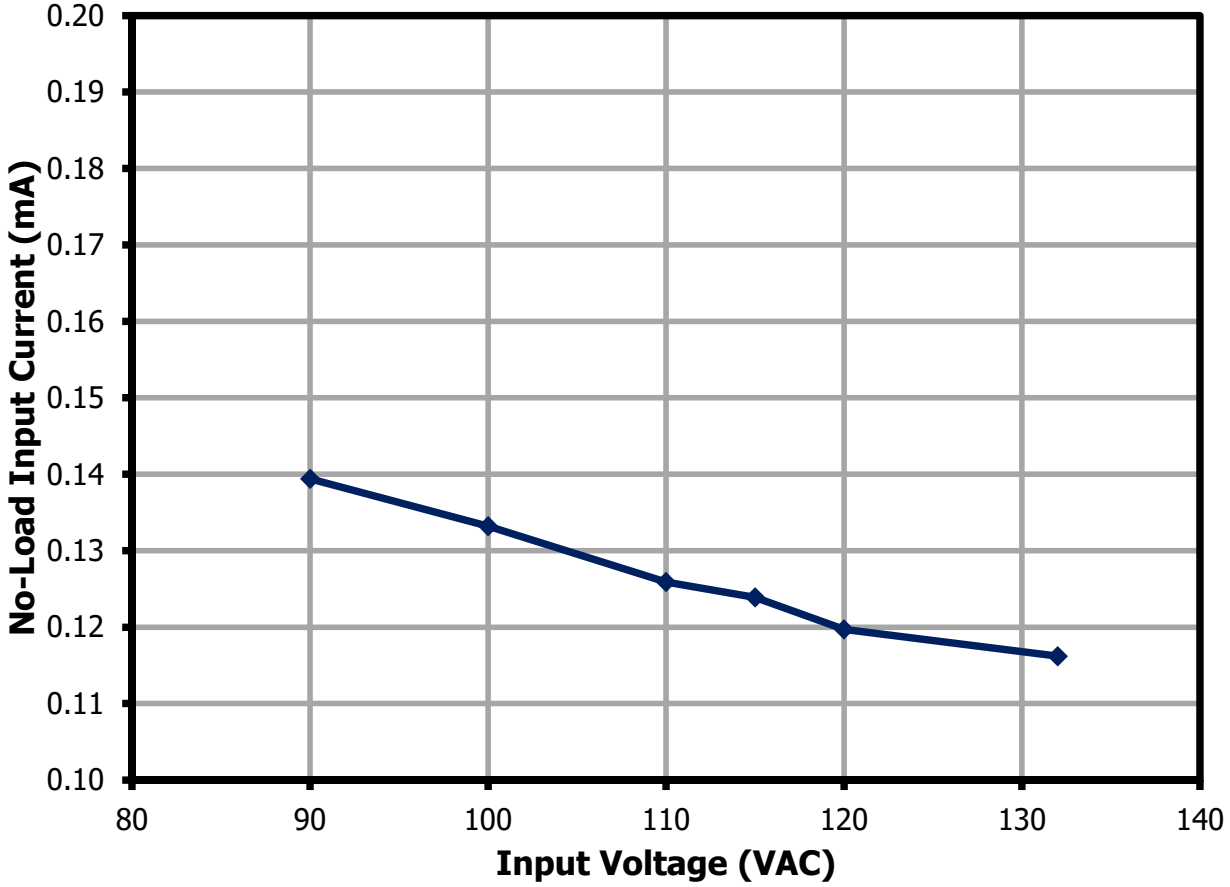


**Figure 7 –** No-Load Input Current vs. Line.

## *8.3 Line Regulation at Different Ambient Temperatures*

### 8.3.1 Line Regulation Performance at Room Ambient Temperature

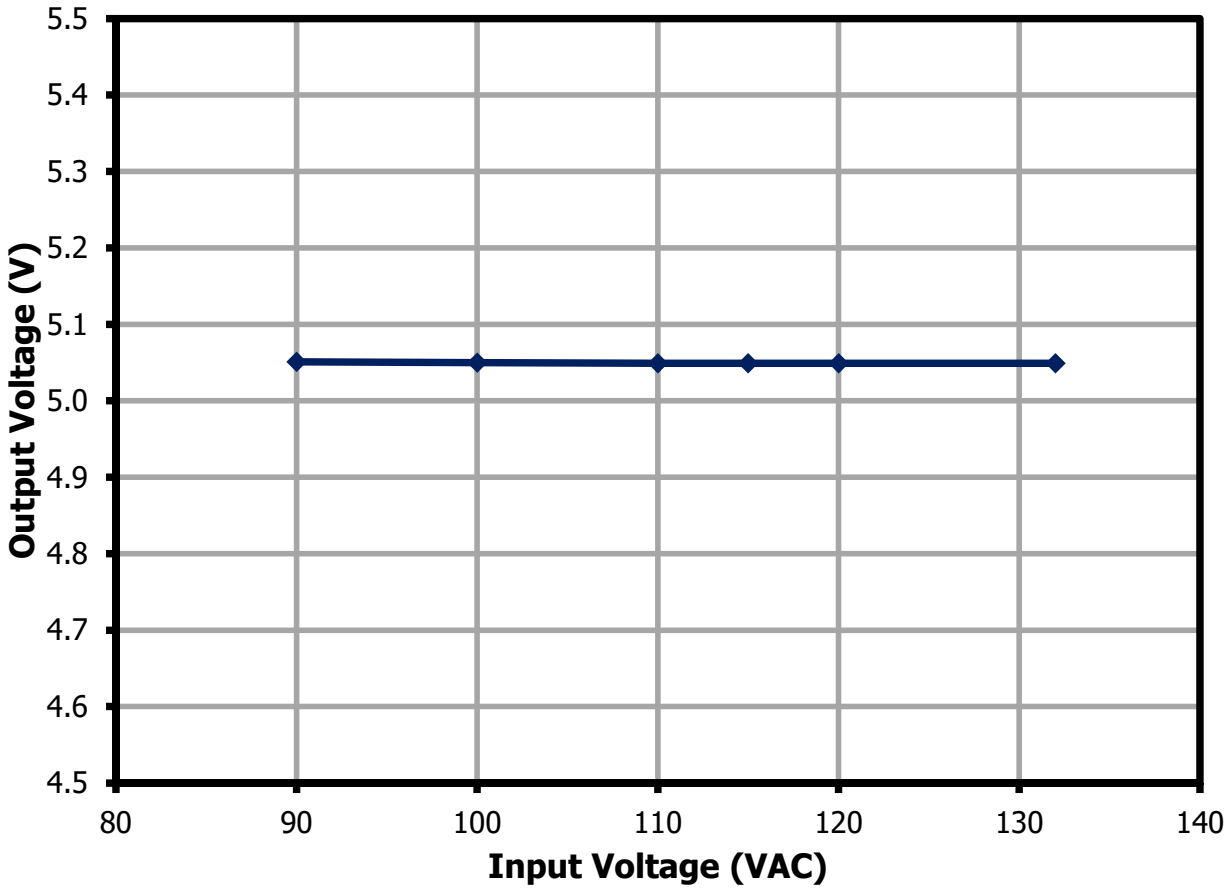


**Figure 8 –** Output Voltage vs. Line Voltage.

### 8.3.2 Line Regulation Performance at 70 °C Ambient Temperature

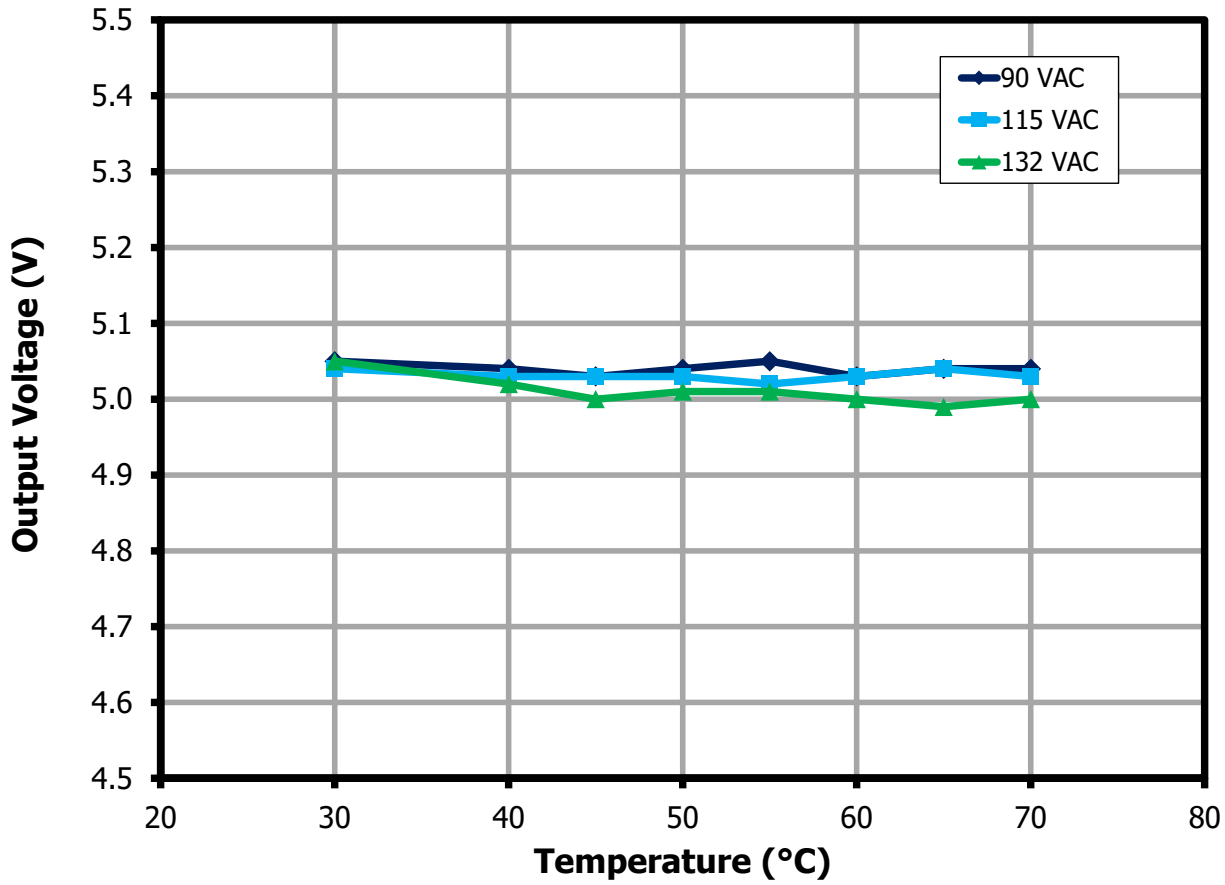


**Figure 9 –** Output Voltage vs. Temperature.

### 8.3.3 Line Regulation Performance at -40°C Ambient Temperature

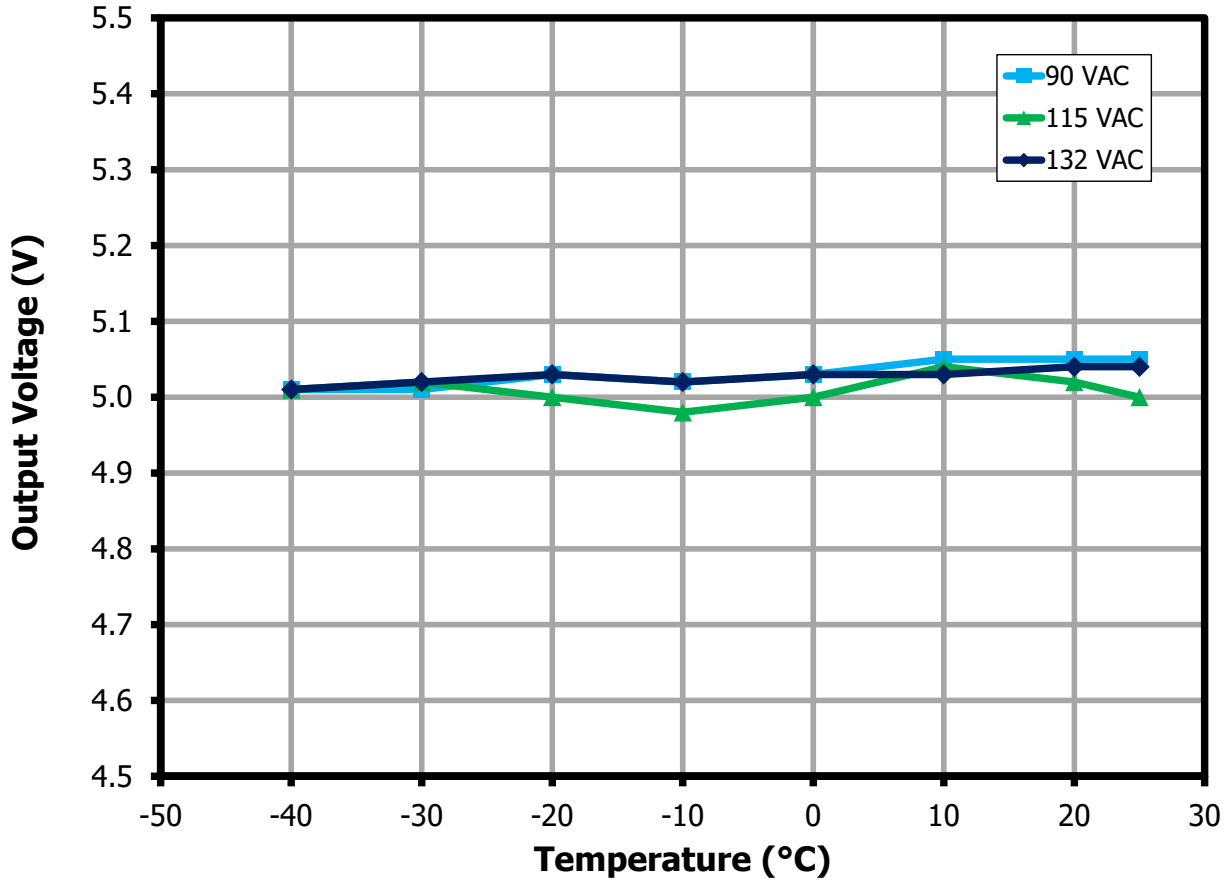


**Figure 10 –** Output Voltage vs. Temperature.

### *8.4 Load Regulation*

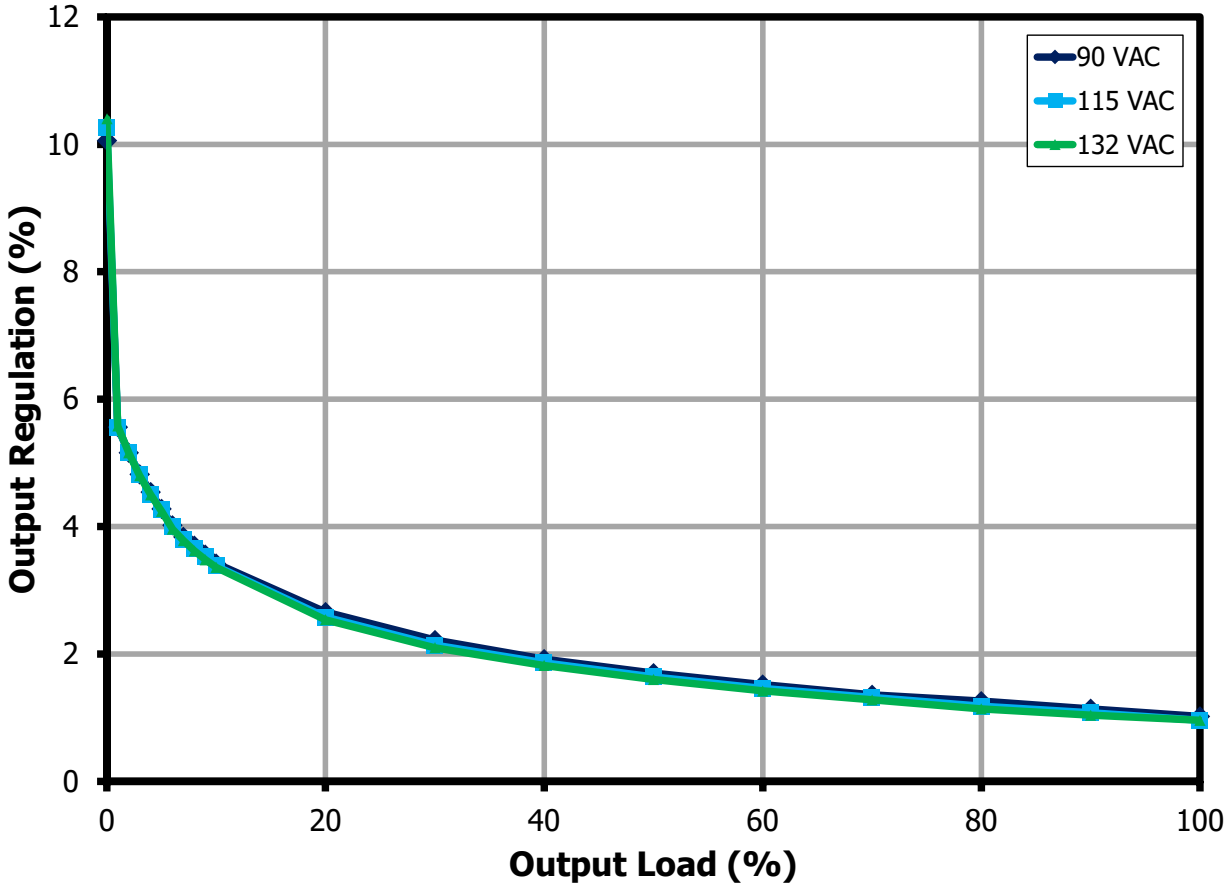


**Figure 11 –** Output Voltage vs. Percent Load.

# 9 Waveforms

## *9.1 Zero-Crossing Detection*

### 9.1.1 Zero-Crossing Detection at Normal Operation

#### 9.1.1.1 100% Load

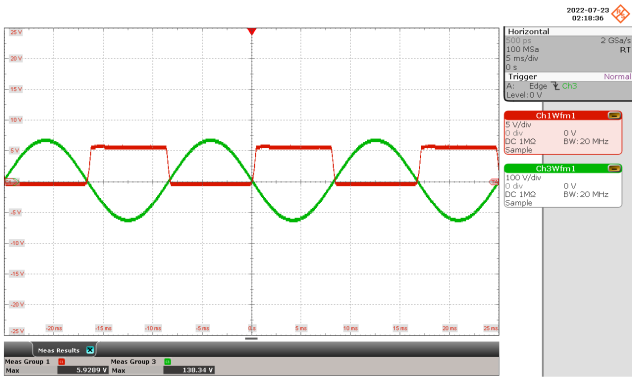

**Figure 12 –** 90 VAC 60 Hz.
CH1: ZCD, 5 V / div., 5 ms / div.
CH3: $V_{IN}$, 100 V / div., 5 ms / div.

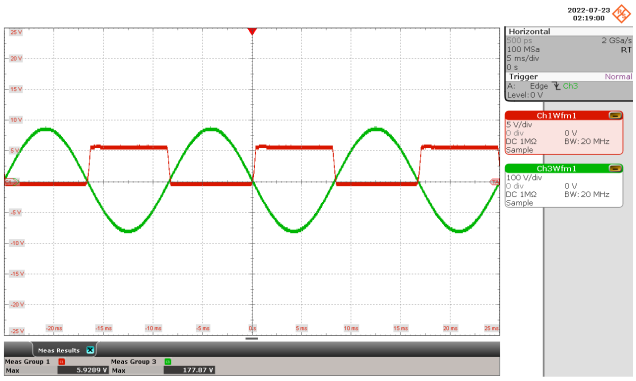

**Figure 13 –** 115 VAC 60 Hz.
CH1: ZCD, 5 V / div., 5 ms / div.
CH3: $V_{IN}$, 100 V / div., 5 ms / div.

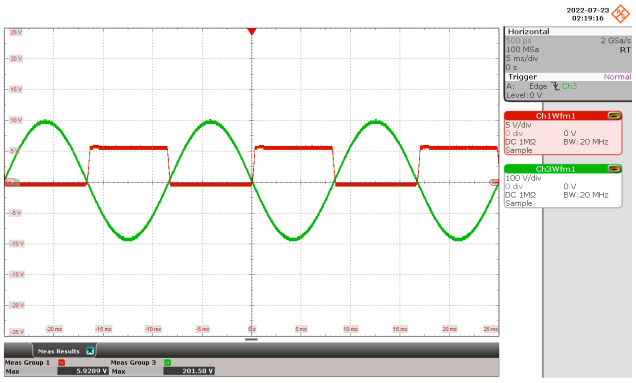

**Figure 14 –** 132 VAC 50 Hz.
CH1: ZCD, 5 V / div., 5 ms / div.
CH3: $V_{IN}$, 100 V / div., 5 ms / div.

### 9.1.1.2 0% Load

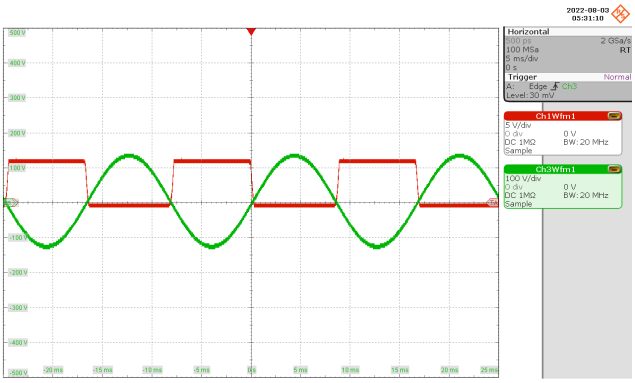

**Figure 15 –** 90 VAC 60 Hz.
CH1: ZCD, 5 V / div., 5 ms / div.
CH3: $V_{IN}$, 100 V / div., 5 ms / div.

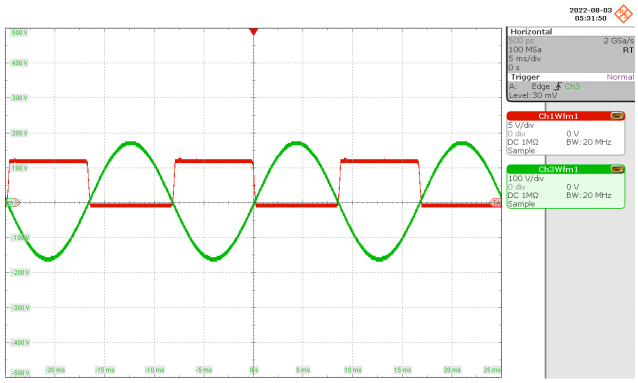

**Figure 16 –** 115 VAC 60 Hz.
CH1: ZCD, 5 V / div., 5 ms / div.
CH3: $V_{IN}$, 100 V / div., 5 ms / div.

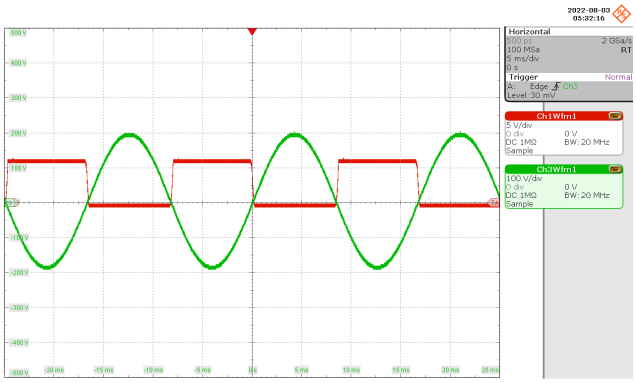

**Figure 17 –** 132 VAC 60 Hz.
CH1: ZCD, 5 V / div., 5 ms / div.
CH3: $V_{IN}$, 100 V / div., 5 ms / div.

### 9.1.2 Zero-Crossing Detection at Start-up

#### 9.1.2.1 0° Start-up Phase

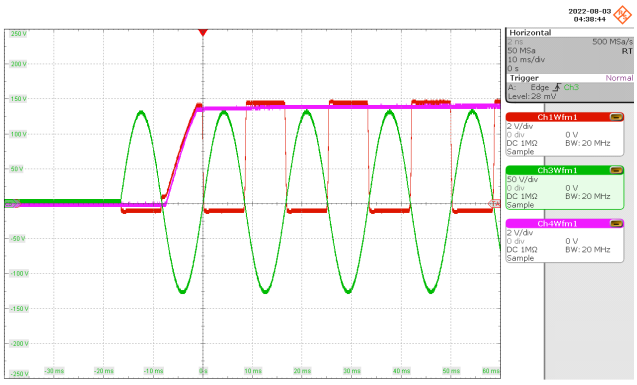

**Figure 18 –** 90 VAC 60 Hz, No-Load.
CH1: ZCD, 2 V / div., 10 ms / div.
CH3: $V_{IN}$, 50 V / div., 10 ms / div.
CH4: $V_{OUT}$, 2 V / div., 10 ms / div.

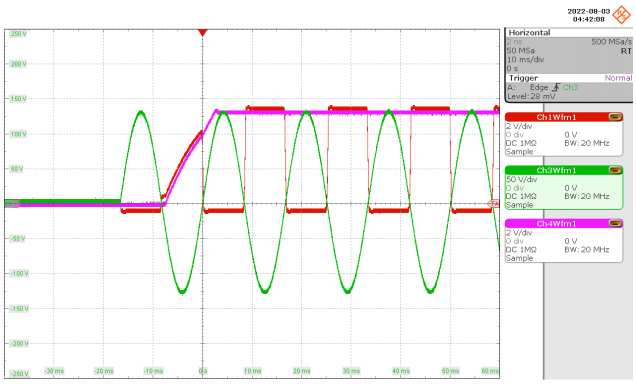

**Figure 19 –** 90 VAC 60 Hz, Full Load.
CH1: ZCD, 2 V / div., 10 ms / div.
CH3: $V_{IN}$, 50 V / div., 10 ms / div.
CH4: $V_{OUT}$, 2 V / div., 10 ms / div.

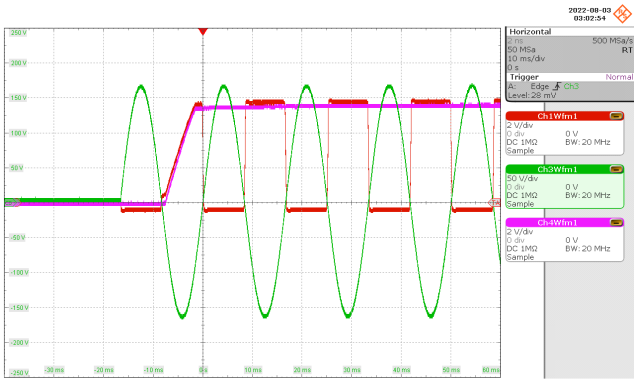

**Figure 20 –** 115 VAC 50 Hz, No-Load.
CH1: ZCD, 2 V / div., 10 ms / div.
CH3: $V_{IN}$, 50 V / div., 10 ms / div.
CH4: $V_{OUT}$, 2 V / div., 10 ms / div.

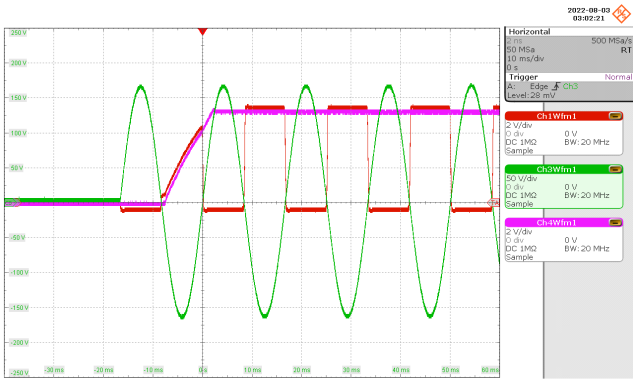

**Figure 21 –** 115 VAC 50 Hz, Full Load.
CH1: ZCD, 2 V / div., 10 ms / div.
CH3: $V_{IN}$, 50 V / div., 10 ms / div.
CH4: $V_{OUT}$, 2 V / div., 10 ms / div.

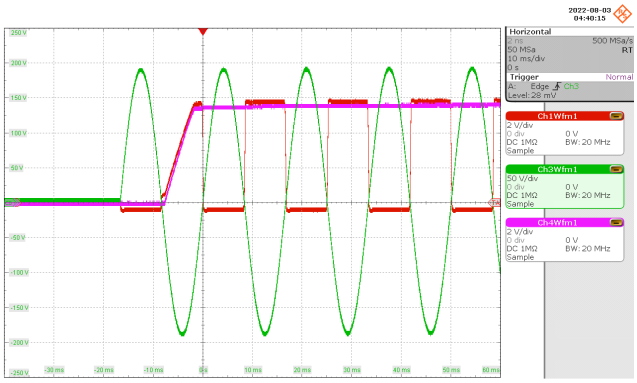

**Figure 22 –** 132 VAC 60 Hz, No-Load.
CH1: ZCD, 2 V / div., 10 ms / div.
CH3: $V_{IN}$, 50 V / div., 10 ms / div.
CH4: $V_{OUT}$, 2 V / div., 10 ms / div.

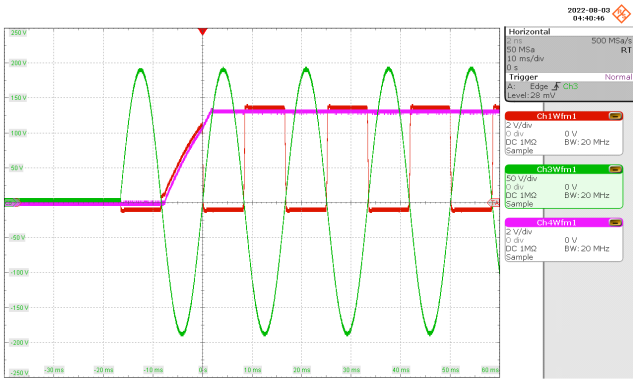

**Figure 23 –** 132 VAC 60 Hz, Full Load.
CH1: ZCD, 2 V / div., 10 ms / div.
CH3: $V_{IN}$, 50 V / div., 10 ms / div.
CH4: $V_{OUT}$, 2 V / div., 10 ms / div.

### 9.1.2.2 90° Start-up Phase

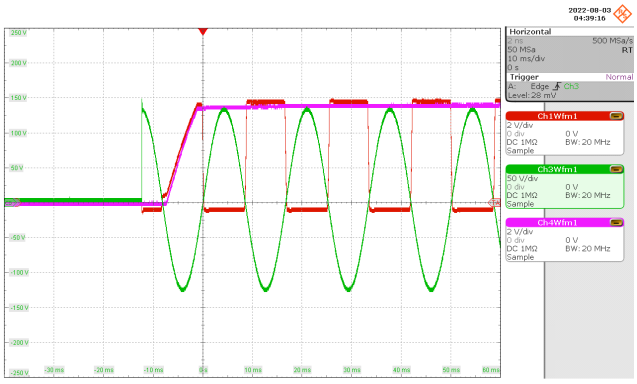

**Figure 24 –** 90 VAC 60 Hz, No-Load.
CH1: ZCD, 2 V / div., 10 ms / div.
CH3: $V_{IN}$, 50 V / div., 10 ms / div.
CH4: $V_{OUT}$, 2 V / div., 10 ms / div.

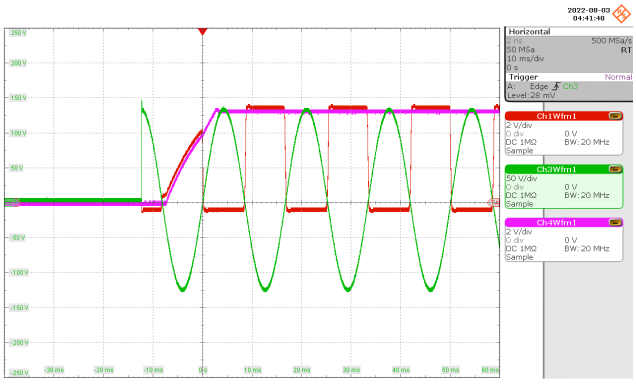

**Figure 25 –** 90 VAC 60 Hz, Full Load.
CH1: ZCD, 2 V / div., 10 ms / div.
CH3: $V_{IN}$, 50 V / div., 10 ms / div.
CH4: $V_{OUT}$, 2 V / div., 10 ms / div.

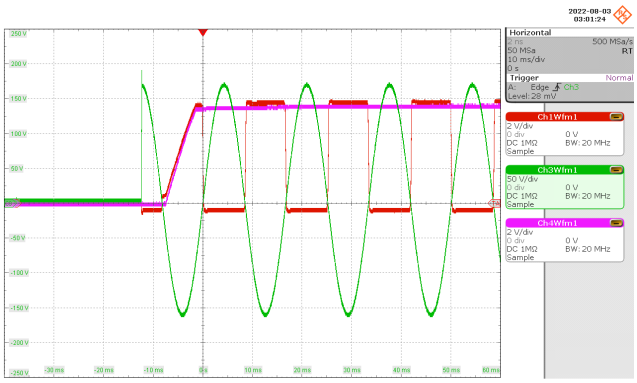

**Figure 26 –** 115 VAC 60 Hz, No-Load.
CH1: ZCD, 2 V / div., 10 ms / div.
CH3: $V_{IN}$, 50 V / div., 10 ms / div.
CH4: $V_{OUT}$, 2 V / div., 10 ms / div.

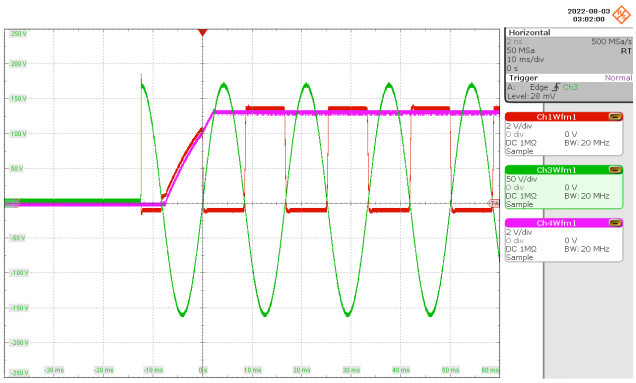

**Figure 27 –** 115 VAC 60 Hz, Full Load.
CH1: ZCD, 2 V / div., 10 ms / div.
CH3: $V_{IN}$, 50 V / div., 10 ms / div.
CH4: $V_{OUT}$, 2 V / div., 10 ms / div.

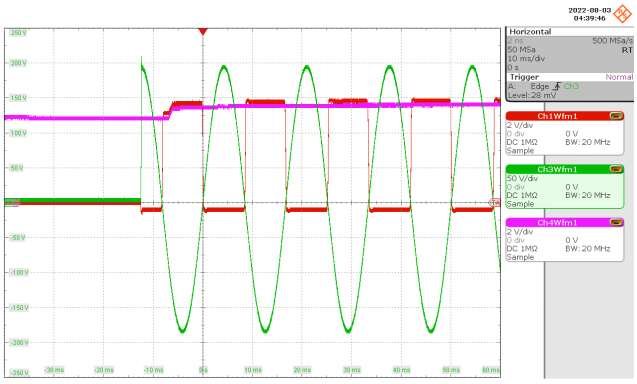

**Figure 28 –** 132 VAC 60 Hz, No-Load.
CH1: ZCD, 2 V / div., 10 ms / div.
CH3: $V_{IN}$, 50 V / div., 10 ms / div.
CH4: $V_{OUT}$, 2 V / div., 10 ms / div.

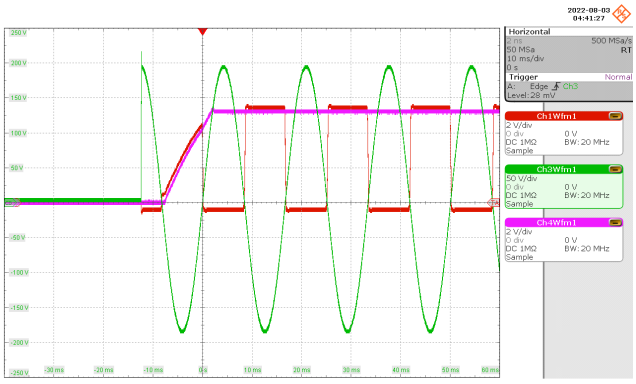

**Figure 29 –** 132 VAC 60 Hz, Full Load.
CH1: ZCD, 2 V / div., 10 ms / div.
CH3: $V_{IN}$, 50 V / div., 10 ms / div.
CH4: $V_{OUT}$, 2 V / div., 10 ms / div.

### 9.1.3 Zero Crossing Detection Delay

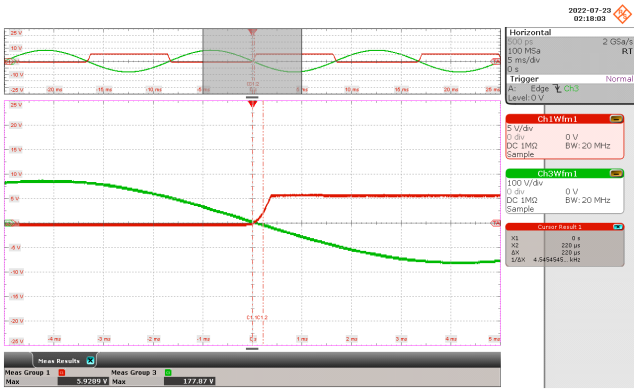

**Figure 30 –** 115 VAC 60 Hz.
CH1: ZCD, 5 V / div., 5 ms / div.
CH2: $V_{IN}$, 100 V / div., 5 ms / div.
Rising Edge Delay = 220 μs.

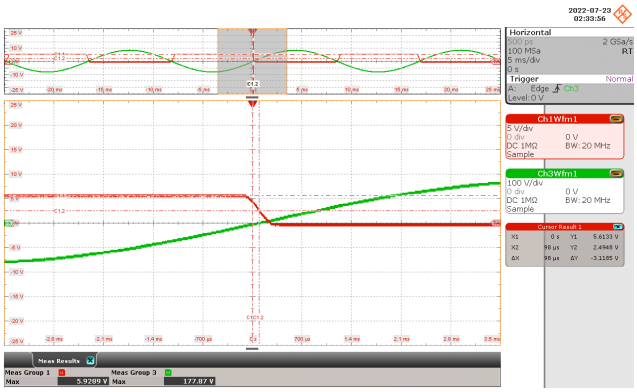

**Figure 31 –** 115 VAC 60 Hz.
CH1: ZCD, 5 V / div., 5 ms / div.
CH2: $V_{IN}$, 100 V / div., 5 ms / div.
Falling Edge Delay = 98 μs.

## 9.2 Output Voltage at Start-up

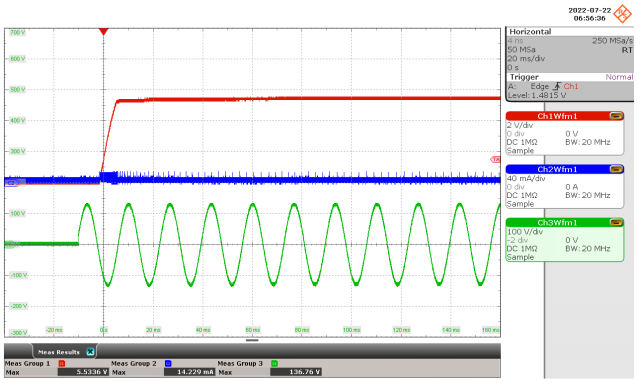

**Figure 32 –** 90 VAC 60 Hz, No-load.
CH1: $V_{OUT}$, 2 V / div., 20 ms / div.
CH2: $I_{OUT}$, 40 mA V / div., 20 ms / div.
CH3: $V_{IN}$, 100 V / div., 20 ms / div.

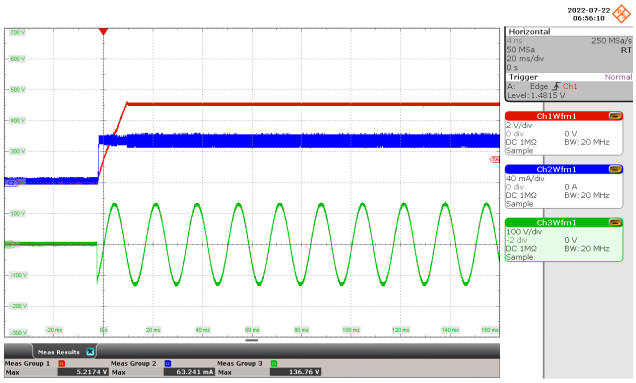

**Figure 33 –** 90 VAC 60 Hz, Full load.
CH1: $V_{OUT}$, 2 V / div., 20 ms / div.
CH2: $I_{OUT}$, 40 mA V / div., 20 ms / div.
CH3: $V_{IN}$, 100 V / div., 20 ms / div.

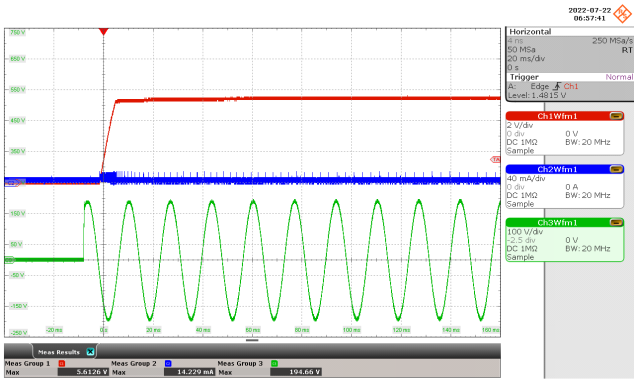

**Figure 34 –** 132 VAC 60 Hz, No-load.
CH1: $V_{OUT}$, 2 V / div., 20 ms / div.
CH2: $I_{OUT}$, 40 mA V / div., 20 ms / div.
CH3: $V_{IN}$, 100 V / div., 20 ms / div.

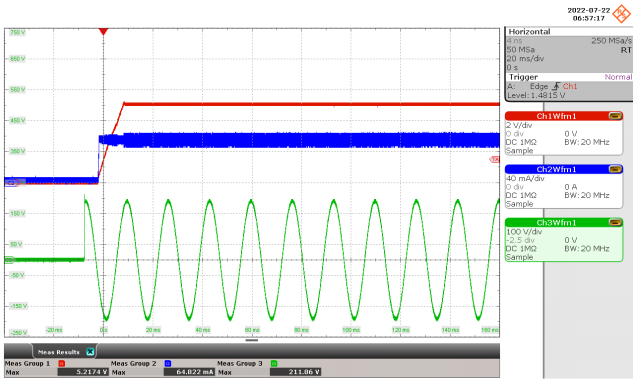

**Figure 35 –** 132 VAC 60 Hz, Full load.
CH1: $V_{OUT}$, 2 V / div., 20 ms / div.
CH2: $I_{OUT}$, 40 mA V / div., 20 ms / div.
CH3: $V_{IN}$, 100 V / div., 20 ms / div.

## *9.3 Switching Waveforms*

### 9.3.1 Primary MOSFET Drain-Source Voltage and Current at Normal Operation

#### 9.3.1.1 100% Load

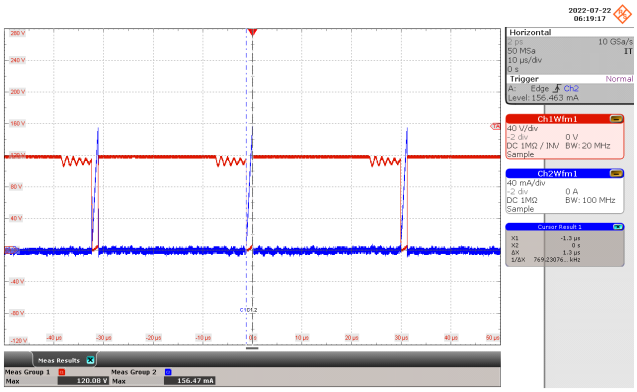

**Figure 36 –** 90 VAC 60 Hz.
CH1: $V_{DS}$, 40 V / div., 10 µs / div.
CH2: $I_{DS}$, 40 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 120.08 V.
$I_{DS(MAX)}$ = 156.47 mA.

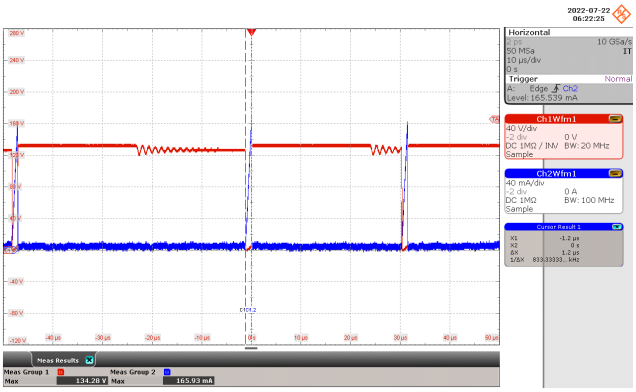

**Figure 37 –** 115 VAC 60 Hz.
CH1: $V_{DS}$, 40 V / div., 10 µs / div.
CH2: $I_{DS}$, 40 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 132.28 V.
$I_{DS(MAX)}$ = 165.93 mA.

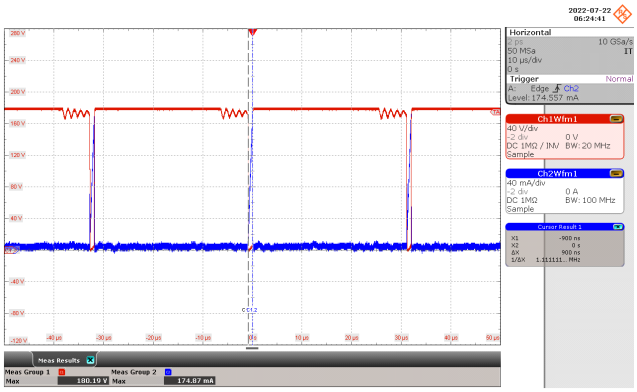

**Figure 38 –** 132 VAC 60 Hz.
CH1: $V_{DS}$, 40 V / div., 10 µs / div.
CH2: $I_{DS}$, 40 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 180.19 V.
$I_{DS(MAX)}$ = 174.87 mA.

### 9.3.1.2 0% Load

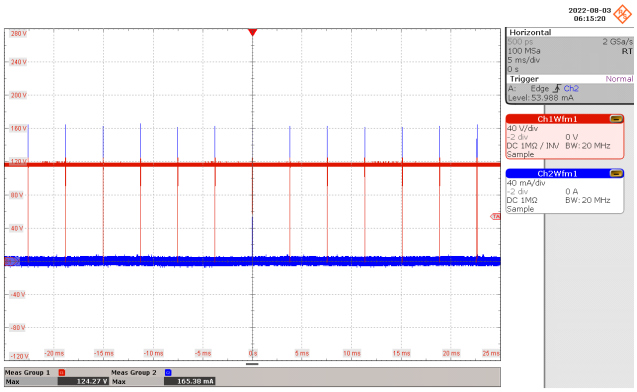

**Figure 39 –** 90 VAC 60 Hz.
CH1: $V_{DS}$, 40 V / div., 5 ms / div.
CH2: $I_{DS}$, 40 mA / div., 5 ms / div.
$V_{DS(MAX)}$ = 124.27 V.
$I_{DS(MAX)}$ = 165.38 mA.

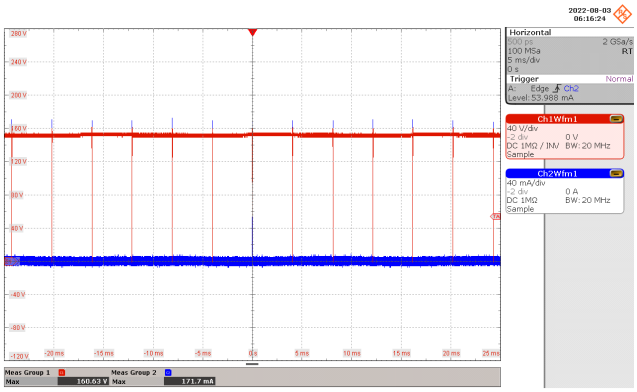

**Figure 40 –** 115 VAC 60 Hz.
CH1: $V_{DS}$, 40 V / div., 5 ms / div.
CH2: $I_{DS}$, 40 mA / div., 5 ms / div.
$V_{DS(MAX)}$ = 160.63 V.
$I_{DS(MAX)}$ = 171.7 mA.

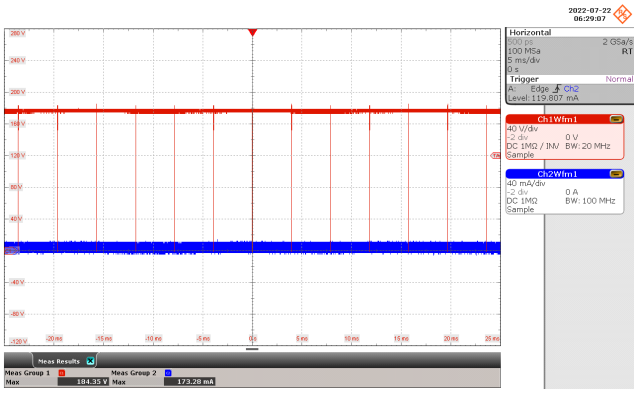

**Figure 41 –** 132 VAC 60 Hz.
CH1: $V_{DS}$, 40 V / div., 5 ms / div.
CH2: $I_{DS}$, 40 mA / div., 5 ms / div.
$V_{DS(MAX)}$ = 184.35 V.
$I_{DS(MAX)}$ = 173.28 mA.

### 9.3.2 Primary MOSFET Drain-Source Voltage and Current at Start-up Operation

#### 9.3.2.1 100% Load

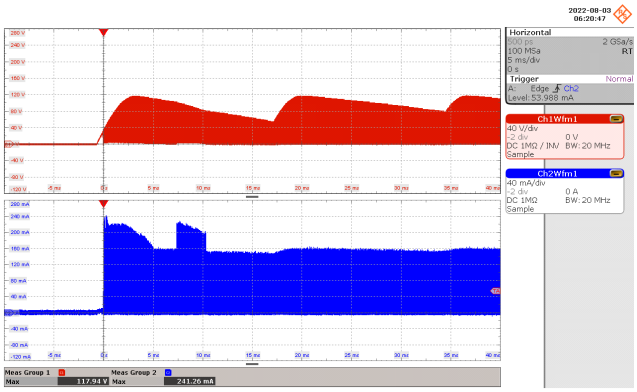

**Figure 42 –** 90 VAC 60 Hz.
CH1: $V_{DS}$, 40 V / div., 5 ms / div.
CH2: $I_{DS}$, 40 mA / div., 5 ms / div.
$V_{DS(MAX)}$ = 117.94 V.
$I_{DS(MAX)}$ = 241.26 mA.

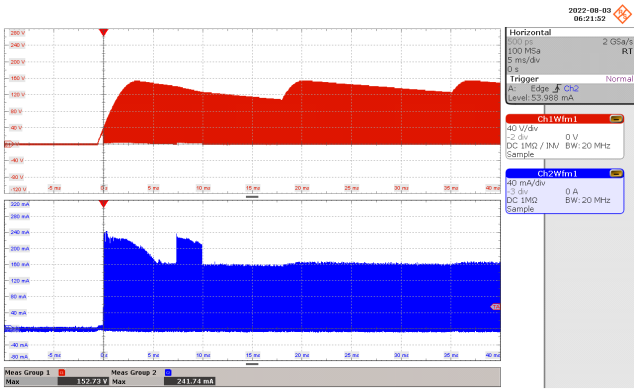

**Figure 43 –** 115 VAC 60 Hz.
CH1: $V_{DS}$, 40 V / div., 5 ms / div.
CH2: $I_{DS}$, 40 mA / div., 5 ms / div.
$V_{DS(MAX)}$ = 152.73 V.
$I_{DS(MAX)}$ = 241.74 mA.

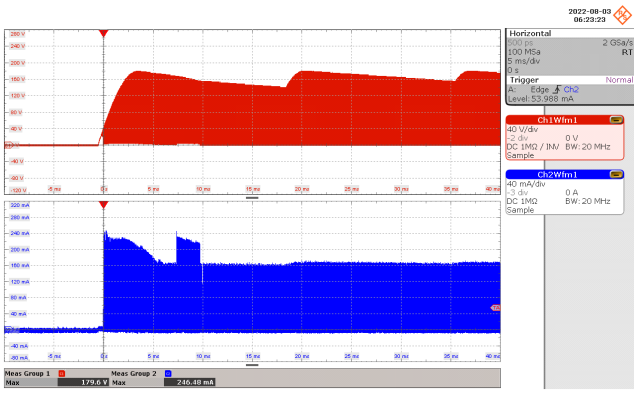

**Figure 44 –** 90 VAC 60 Hz.
CH1: $V_{DS}$, 40 V / div., 5 ms / div.
CH2: $I_{DS}$, 40 mA / div., 5 ms / div.
$V_{DS(MAX)}$ = 179.6 V.
$I_{DS(MAX)}$ = 246.48 mA.

### 9.3.2.2 0% Load

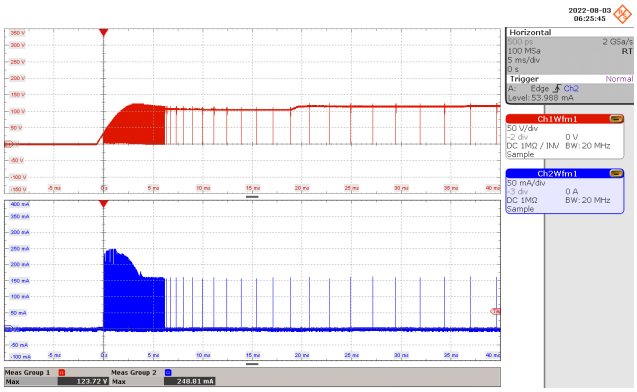

**Figure 45 –** 90 VAC 60 Hz.
CH1: $V_{DS}$, 50 V / div., 5 ms / div.
CH2: $I_{DS}$, 50 mA / div., 5 ms / div.
$V_{DS(MAX)}$ = 123.72 V.
$I_{DS(MAX)}$ = 248.81 mA.

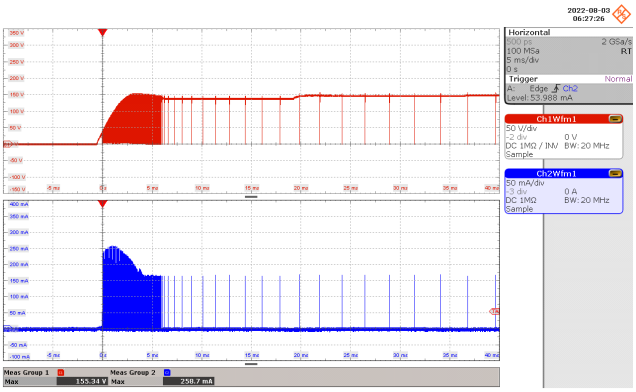

**Figure 46 –** 115 VAC 60 Hz.
CH1: $V_{DS}$, 50 V / div., 5 ms / div.
CH2: $I_{DS}$, 50 mA / div., 5 ms / div.
$V_{DS(MAX)}$ = 155.34 V.
$I_{DS(MAX)}$ = 258.7 mA.

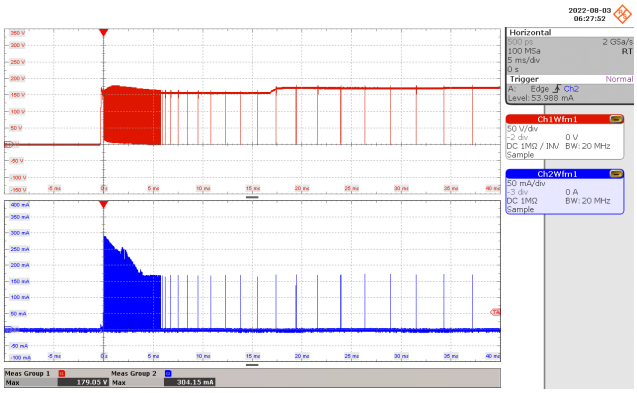

**Figure 47 –** 132 VAC 60 Hz.
CH1: $V_{DS}$, 50 V / div., 5 ms / div.
CH2: $I_{DS}$, 50 mA / div., 5 ms / div.
$V_{DS(MAX)}$ = 179.05 V.
$I_{DS(MAX)}$ = 304.15 mA.

# 10 Thermal Performance

Test Condition: This was performed inside a thermal chamber, and the DUT is contained within a metal box. The DUT was soaked for 2 hours each line, exposed to high ambient temperature (70 °C) and room temperature, and the results were recorded using a thermocouple and datalogger (GL840 GRAPHTEC).

## *10.1 Test Set-up*


**Figure 48 –** Thermal Chamber Test Set-up.

### 10.1.1 Thermal Performance (70 ºC Ambient Temperature)

| **Full Load (5 V 50 mA)<br>70 ºC Ambient** | | |
|---|---|---|
| **Component** | **Case Temperature (°C)** | |
| | **90 VAC** | **132 VAC** |
| VR1 | 54.5 | 53.2 |
| Freewheeling Diode | 55.3 | 54.8 |
| Output Inductor | 53.9 | 53.6 |
| Input Capacitor | 52.9 | 52.2 |
| LinkSwitch-TNZ | 54.3 | 53.9 |

### 10.1.2 Thermal Performance (-40 ºC Ambient Temperature)

| Full Load (5 V 50 mA) -40 ºC Ambient | | |
|---|---|---|
| **Component** | **Case Temperature (°C)** | |
| | **90 VAC** | **132 VAC** |
| VR1 | -34.1 | -35.6 |
| Freewheeling Diode | -32.5 | -33.4 |
| Output Inductor | -34.9 | -35.6 |
| Input Capacitor | -35.7 | -36.6 |
| LinkSwitch-TNZ | -34.9 | -35.7 |

### 10.1.3 Thermal Performance (70 ºC Ambient Temperature)

| Full Load (5 V 50 mA) 70 ºC Ambient | | |
|---|---|---|
| **Component** | **Case Temperature (°C)** | |
| | **90 VAC** | **132 VAC** |
| VR1 | 71 | 70.4 |
| Freewheeling Diode | 71.5 | 71.6 |
| Output Inductor | 70.3 | 70.6 |
| Input Capacitor | 69.3 | 69.4 |
| LinkSwitch-TNZ | 70.9 | 71 |

### 10.1.4 Thermal Performance (Room Ambient Temperature)

| Full Load (5 V 50 mA) Room Temperature | | |
|---|---|---|
| **Component** | **Case Temperature (°C)** | |
| | **90 VAC** | **132 VAC** |
| VR1 | 29.05 | 27.8 |
| Freewheeling Diode | 29.05 | 29.05 |
| Output Inductor | 27.6 | 27.6 |
| Input Capacitor | 26.55 | 26.05 |
| LinkSwitch-TNZ | 28.05 | 28 |

# 11 Conducted EMI

## *11.1 Test Set-up*

EMI measurement was done using a resistor load.

## *11.2 Equipment and Load Used*

1. Rohde and Schwarz ENV216 two-line V-network.
2. Rohde and Schwarz ESRP EMI test receiver.
3. Variable voltage transformer set at 115 VAC

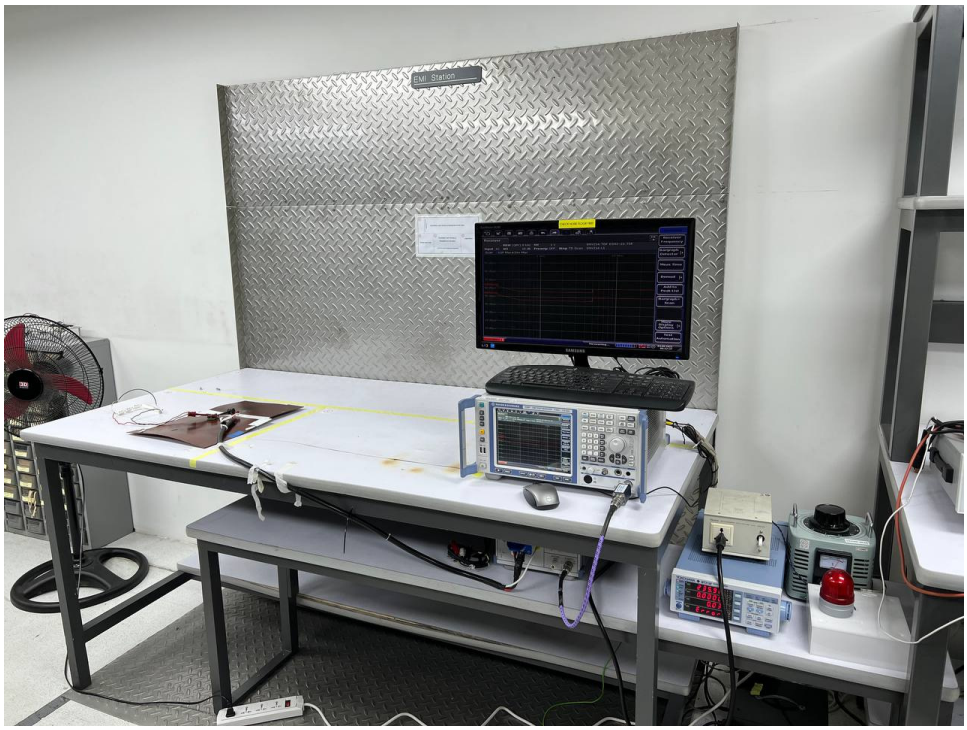


**Figure 49 –** Conducted EMI Test Set-up.

## 11.3 Conducted EMI Test Results

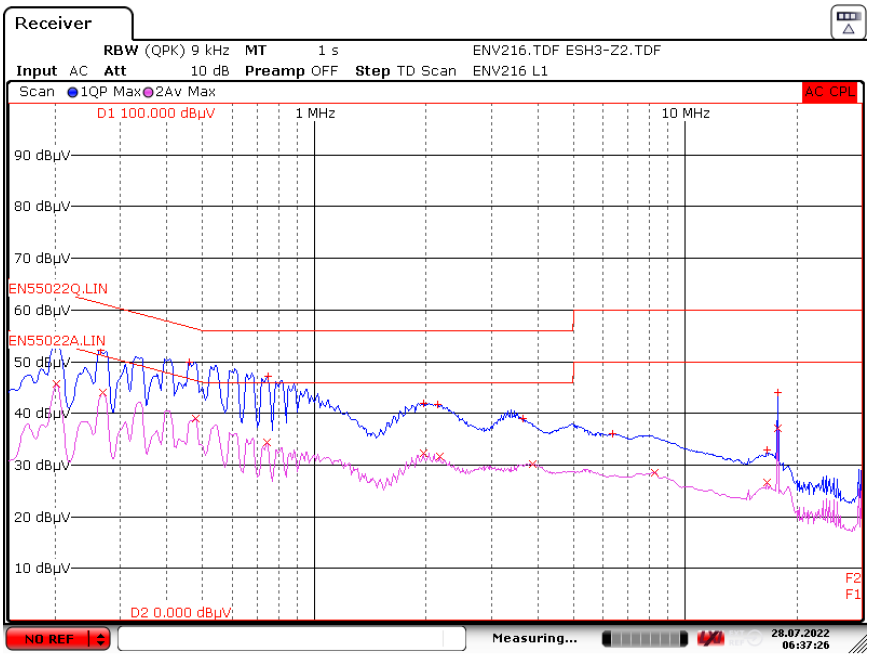


**Figure 50 –** LINE.
115 VAC 60 Hz.

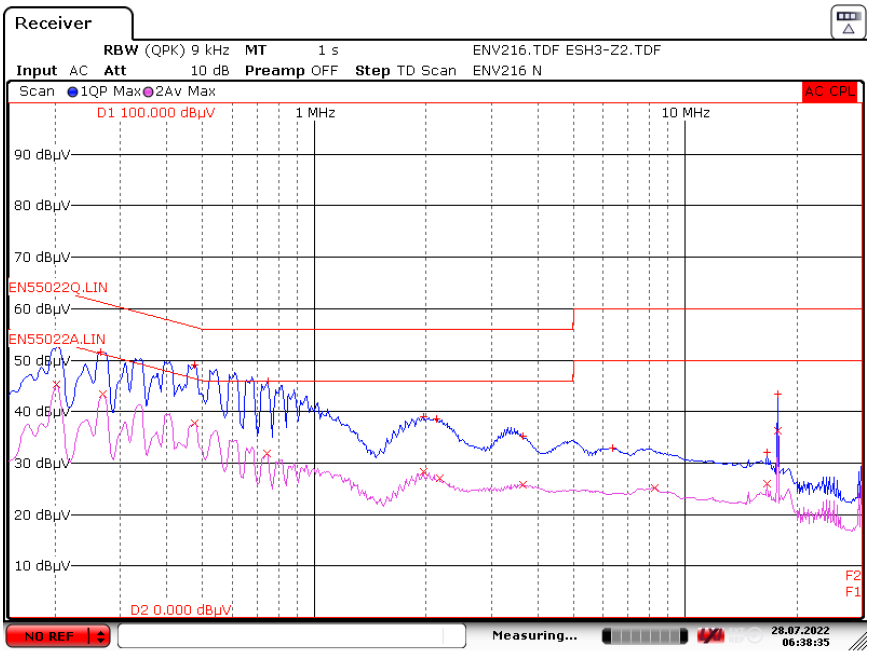


**Figure 51 –** NEUTRAL.
115 VAC 60 Hz.

# 12 Line Surge

Differential mode input line surge testing was completed on a single test unit to IEC61000-4-5. Input voltage was set at 115 VAC / 60 Hz. Output was loaded at full load (5V/50mA) using a 100 Ω fixed resistor and operation was verified following each surge event.

## *12.1 Differential Surge Test Results*

Source Impedance: 2Ω
Repetition Rate: 1/30 s
No. of surge strike per location: 10 strikes

| DM Surge Level (V) | Input Voltage (VAC) | Injection Location | Injection Phase (º) | Test Result (Pass/Fail) |
|---|---|---|---|---|
| +1000 | 115 | L to N | 0 | Pass |
| -1000 | 115 | L to N | 0 | Pass |
| +1000 | 115 | L to N | 90 | Pass |
| -1000 | 115 | L to N | 90 | Pass |
| +1000 | 115 | L to N | 180 | Pass |
| -1000 | 115 | L to N | 180 | Pass |
| +1000 | 115 | L to N | 270 | Pass |
| -1000 | 115 | L to N | 270 | Pass |

**Note:** In all PASS results, no damage and no auto-restart was observed.

## *12.2 Ring Wave Surge Test Results*

Source Impedance: 12 Ω
Repetition Rate: 1/30 s
No. of surge strike per location: 10 strikes

| Surge Level (V) | Input Voltage (VAC) | Injection Location | Injection Phase (º) | Test Result (Pass/Fail) |
|---|---|---|---|---|
| +2500 | 115 | L to N | 0 | Pass |
| -2500 | 115 | L to N | 0 | Pass |
| +2500 | 115 | L to N | 90 | Pass |
| -2500 | 115 | L to N | 90 | Pass |
| +2500 | 115 | L to N | 180 | Pass |
| -2500 | 115 | L to N | 180 | Pass |
| +2500 | 115 | L to N | 270 | Pass |
| -2500 | 115 | L to N | 270 | Pass |

**Note:** In all PASS results, no damage and no auto-restart was observed.

# 13 Audible Noise

To reduce audible noise further, an off-the-shelf dog-bone or barrel type inductor is recommended. Horizontal mounting helps minimize PCB vibration that may amplify audible noise. DUT is encased in a dimming case to replicate real-life condition. The DUT was placed inside a sound isolated chamber fitted with a microphone for audible noise measurements. The microphone was placed approximately 10 cm on top of the DUT. Audible noise was tested at 115VAC at all load conditions.

## *13.1 Audible Noise Test Set-up*

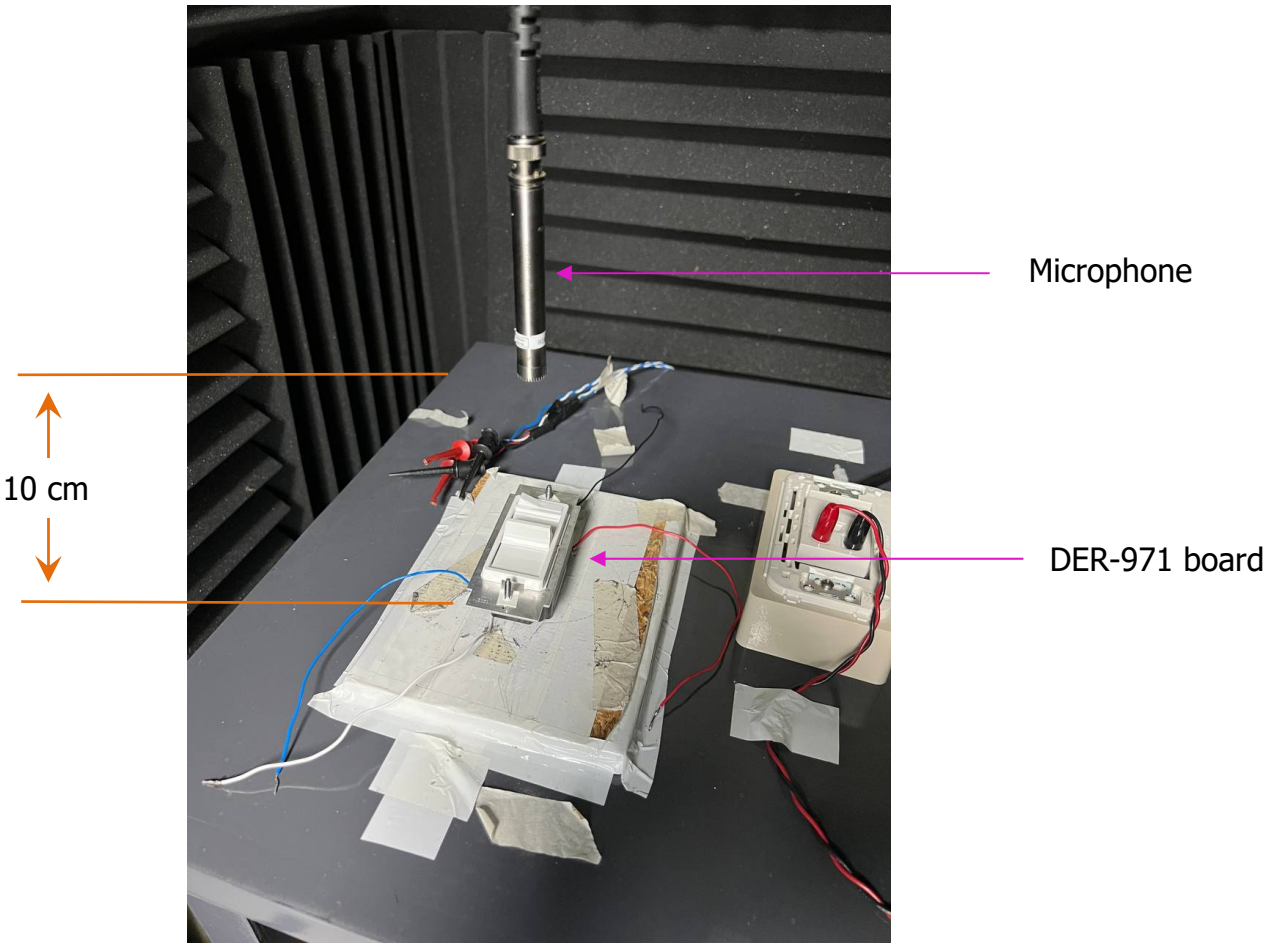


**Figure 52 –** Audible Noise Measurement Set-up Pictures.

## *13.2 Audible Noise Measurements*

### 13.2.1 Audible Noise Scan

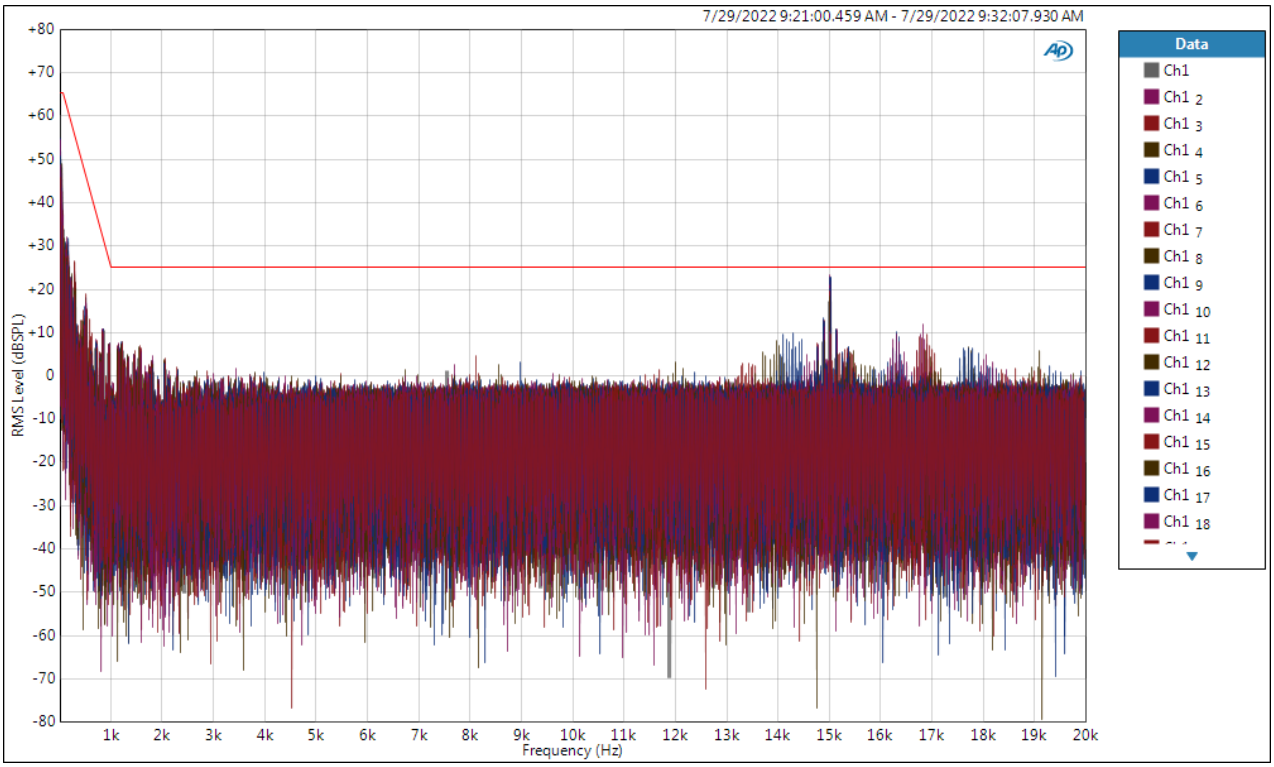


**Figure 53 –** Audible Noise Measurements at 115 VAC.

# 14 Revision History

| Date | Author | Revision | Description and Changes | Reviewed |
|---|---|---|---|---|
| 23-Jan-23 | JEE | 1.0 | Initial Release. | Apps & Mktg |
| | | | | |
| | | | | |
| | | | | |

## For the latest updates, visit our website: www.power.com



## Power Integrations Worldwide Sales Support Locations

**WORLD HEADQUARTERS**
5245 Hellyer Avenue
San Jose, CA 95138, USA.
Main: +1-408-414-9200
Customer Service:
Worldwide: +1-65-635-64480
Americas: +1-408-414-9621
e-mail: usasales@power.com

**CHINA (SHANGHAI)**
Rm 2410, Charity Plaza, No. 88,
North Caoxi Road,
Shanghai, PRC 200030
Phone: +86-21-6354-6323
e-mail: chinasales@power.com

**CHINA (SHENZHEN)**
17/F, Hivac Building, No. 2, Keji
Nan 8th Road, Nanshan District,
Shenzhen, China, 518057
Phone: +86-755-8672-8689
e-mail: chinasales@power.com

**GERMANY** (AC-DC/LED Sales)
Einsteinring 24
85609 Dornach/Aschheim
Germany
Tel: +49-89-5527-39100
e-mail: eurosales@power.com

**GERMANY** (Gate Driver Sales)
HellwegForum 1
59469 Ense
Germany
Tel: +49-2938-64-39990
e-mail: igbt-driver.sales@
power.com

**INDIA**
#1, 14th Main Road
Vasanthanagar
Bangalore-560052
India
Phone: +91-80-4113-8020
e-mail: indiasales@power.com

**ITALY**
Via Milanese 20, 3rd. Fl.
20099 Sesto San Giovanni (MI) Italy
Phone: +39-024-550-8701
e-mail: eurosales@power.com

**JAPAN**
Yusen Shin-Yokohama 1-chome Bldg.
1-7-9, Shin-Yokohama, Kohoku-ku
Yokohama-shi,
Kanagawa 222-0033 Japan
Phone: +81-45-471-1021
e-mail: japansales@power.com

**KOREA**
RM 602, 6FL
Korea City Air Terminal B/D,
159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728 Korea
Phone: +82-2-2016-6610
e-mail: koreasales@power.com

**SINGAPORE**
51 Newton Road,
#19-01/05 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
e-mail: singaporesales@power.com

**TAIWAN**
5F, No. 318, Nei Hu Rd.,
Sec. 1
Nei Hu District
Taipei 11493, Taiwan R.O.C.
Phone: +886-2-2659-4570
e-mail: taiwansales@power.com

**UK**
Building 5, Suite 21
The Westbrook Centre
Milton Road
Cambridge
CB4 1YG
Phone: +44 (0) 7823-557484
e-mail: eurosales@power.com