Design Example Report

Title	***3-Phase Inverter Using BridgeSwitch™ BRD1260C and LinkSwitch™-TN2 LNK3202D in Sinusoidal Control Scheme***
Specification	310 VDC Input, 40 W Inverter Output, 0.2 A Motor RMS Current, 1500 RPM for 8-Pole Brushless DC Motors
Application	High-Voltage Brushless DC (BLDC) Motor for Fan Application
Author	Applications Engineering Department
Document No.	DER-749
Date	January 9, 2019
Revision	1.0

Summary and Features

- BridgeSwitch – High-voltage half-bridge motor driver
    - Integrated 600 V FREDFETs with ultra-soft, fast recovery diodes
- Hall sensor based sinusoidal control scheme using Princeton Technology Corp. IC (PT2505)
- +24 V motor control chip aux supply circuit using LinkSwitch-TN2 in buck configuration
- Fully self-biased operation - no auxiliary power supply needed on the BridgeSwitch devices
- Lossless over-current protection using BridgeSwitch instantaneous phase current output
- Integrated high-side and low-side cycle-by-cycle current limit on each BridgeSwitch devices
- Device over-temperature protection
- Fault protection mechanisms (overvoltage and undervoltage protection, over-current protection, system over-temperature and motor lock protection)
- On-board programming interface for parameter setting and one-time programming (OTP)
- Voltage controlled speed input and pulse output signal for speed information
- PCB size customized for a 40 W inverter fan design
- No external heat sink

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Important Note:
During operation, the design example board is subject to hazards including high voltages, rotating parts, bare wires, and hot surfaces. Energized DC bus capacitors require time to discharge after DC input disconnection.

All testing should use an isolation transformer to provide the DC input to the board.

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1 Introduction

This document is an engineering report describing a 40 W, >93% efficiency sinusoidal control 3-phase inverter for a high-voltage brushless DC (BLDC) motor drive. The design incorporates a complete inverter stage and a control stage to drive a 3-phase BLDC motor for fan applications.

The inverter stage is implemented using three fully integrated BridgeSwitch (BRD1260C) devices in a small footprint surface mount InSOP-24C package with exposed pads that enable heat sinking through PCB.

The control part uses a hall sensor based sine wave driving scheme control chip from Princeton Technology Corp. (PT2505) in SSOP28 package. Sinusoidal commutation allows electrical audible noise reduction in motor phase commutation. The PT2505 operates at 20 kHz PWM frequency and comes with a BLDC user interface kit that allows parameter settings and one-time programming directly on the inverter board.

This document contains the inverter and motor specifications, schematic, bill of materials, printed circuit board layout, the inverter performance, fault protections, parameter settings and test setup.

Figure 1 – Populated Circuit Board Photograph.

2 Specifications

The table below provides the electrical specification of the 3-phase inverter design. The results section provides actual performance data.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	280	310	340	V	High-Voltage DC Bus.
Power	P_{IN}		43		W	
Speed Control Voltage	V_{SP}	2.1		5.4	V	External DC Supply.
Output						
Continuous Power	P_{OUT}		40		W	Inverter Output Tested At 0.2 N-m 1500 RPM.
Peak Power[1]	P_{OUT-PK}		60		W	Inverter Output Tested At 0.2 N-m 2400 RPM.
Motor Current	I_{MOTOR}		0.2		Arms	At 0.2 N-m Torque.
Output Speed	ω		1500	2400	RPM	
PWM Carrier Frequency	F_{PWM}		20		kHz	Self-Supplied Operation.
Speed Pulse Output[2]	FG		300		Hz	FG Terminal Output.
Efficiency						
Full load	ζ		93		%	Inverter Efficiency at 0.2 N-m Torque at 1500 RPM.
Motor Specifications						
Number of Poles	N_{POLES}		8		P	
Rated Power	P_{MOTOR}		40		W	
Rated Speed	ω_{MOTOR}		1500		RPM	
Environmental						
Ambient Temperature	T_{AMB}	0	25	40	°C	Free Convection.
Protection						
Undervoltage Threshold	V_{UV}		240		V	
Overvoltage Threshold	V_{OV}		390		V	
Internal HS/LS FREDFET Over-current Threshold[3]	I_{OC}		0.7		A	BridgeSwitch Integrated Feature.
System Over-current	I_{SYS-OC}		0.5		A	Motor Current Sensed Through IPH Pin.
System Over-temperature[4]	T_{SYS}		95		°C	Hysteretic – Operation Restarts at 45 °C Ambient Temperature.

Notes:
[1] Peak power duration depends on the application consideration of the motor case temperature - needs verification in the actual application
[2] Speed pulse output frequency relation: 5 pulses per mechanical revolution – FG terminal pulled up to external supply (5 V to 15 V)
[3] Externally programmable through XL/XH pin resistors (44.2 kΩ default at 0.7 A)
[5] Temperature sensed through external NTC thermistor - needs verification in the actual application

Table 1 – Inverter Specification.

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3 Schematic

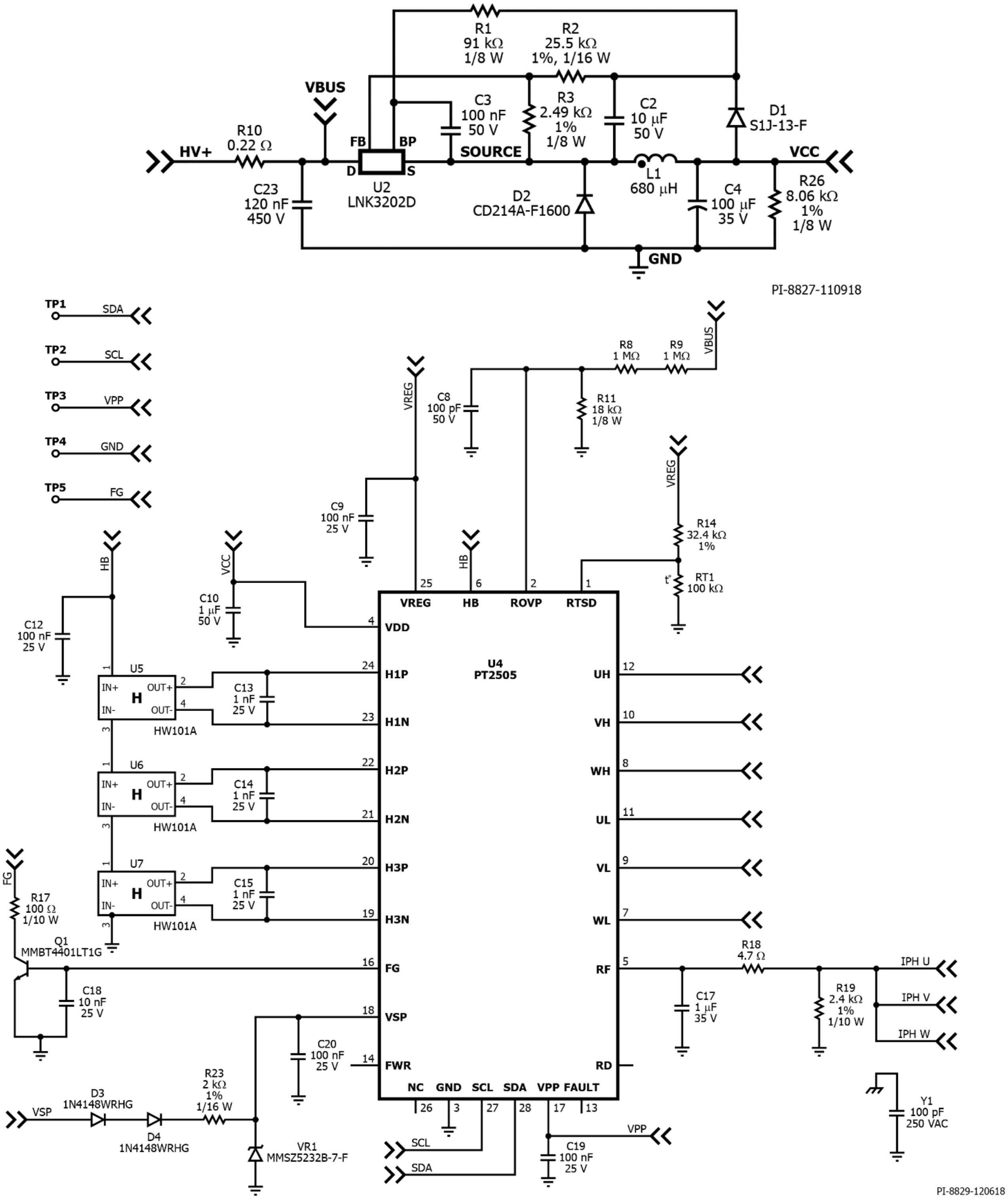

Figure 2 – BridgeSwitch 3-Phase Inverter Input Stage and Controller Schematic.

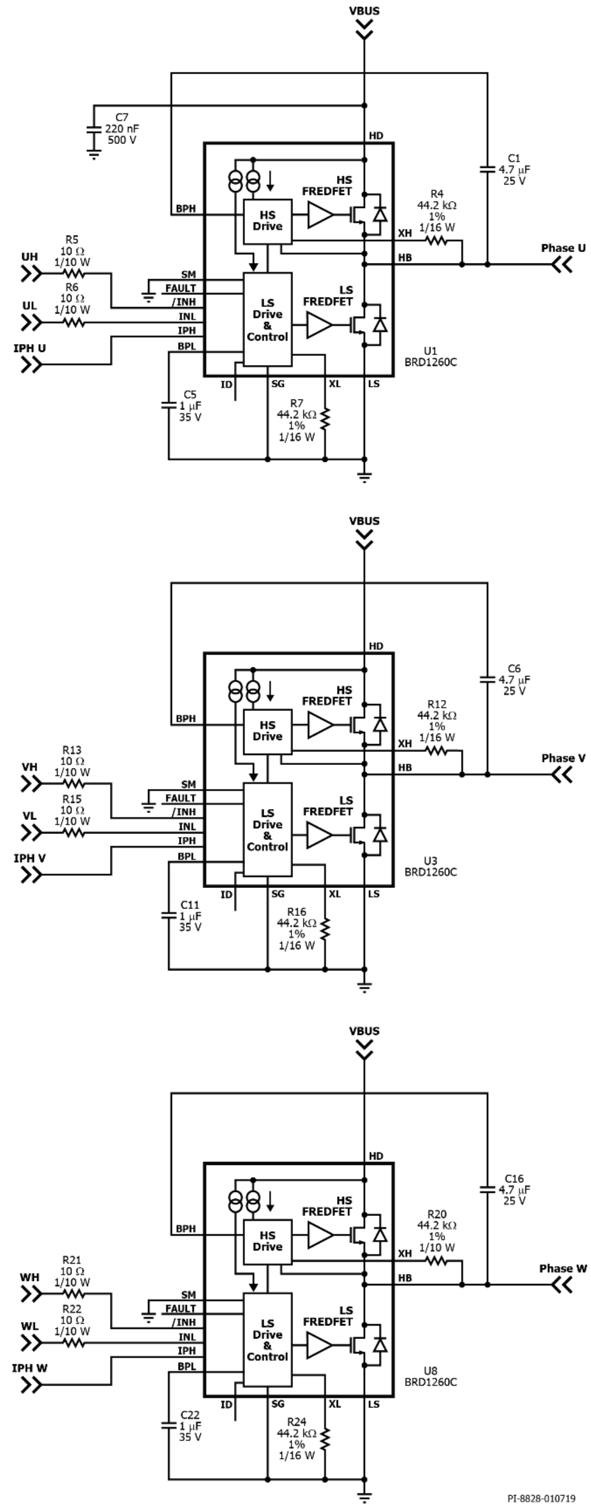

Figure 3 – BridgeSwitch 3-Phase Power Stage Schematic.

4 Circuit Description

The schematic in Figure 2 and 3 shows a 3-phase inverter employing three BRD1260C devices driven by a hall sensor based motor control chip (PT2505) in a sinusoidal commutation scheme. The circuit enables driving a high-voltage, 3-phase brushless DC (BLDC) motor from a rectified AC input voltage ideal for a fan application. BridgeSwitch combines two N-channel 600 V rated power FREDFETs, gate drivers and controllers into a low profile surface mount package. The power FREDFETs feature ultra-soft, fast recovery diodes ideally suited for hard switched inverter drives. Both drivers are fully self-supplied eliminating the need for an external power supply for the design. Integrated on the board is the LinkSwitch-TN2 (LNK3202D) in a buck converter configuration used to provide power to the motor control chip. The inverter board operates without using external heat sinks.

4.1 *Input and Output Terminals*

The high-voltage DC input connects to the input terminals J1 and the power ground to J2 terminal. Terminal J3 provides the input for the voltage control speed input. Output pulse signal proportional to the motor speed is provided through J4 terminal.

4.2 *Decoupling Capacitors and Input Protection*

The input stage provides local decoupling of the rectified AC mains through capacitor C23. A film capacitor was chosen because it offers high temperature capacity, excellent stability and higher reliability against mechanical vibrations from the motor operation. Resistor R10 provides a low cost protection mechanism for any occurring abnormal high current faults in the inverter board.

4.3 *LinkSwitch-TN2 (LNK3202D) IC Supply Stage*

The LNK3202D IC tapped to the high-voltage input in a non-isolated buck configuration powers the motor control chip PT2505 at +24 V. LinkSwitch-TN2 integrates a 725 V power MOSFET and control circuitry into a single low cost IC. The device is self-starting from the DRAIN (D) pin with local supply decoupling provided by capacitor C3 connected to the BYPASS (BP) pin. During normal operation, the device is powered from output via a current limiting resistor R1. Output rectification is provided by L1 and C4 with D2 as freewheeling diode. The voltage across L1 is rectified and smoothed by D1 and C2. Feedback is provided by R1 and R2 and connected to the FB pin to provide the nominal output voltage of 24 V. Resistor R26 is placed across the output as a pre-load resistor.

4.4 *PT2505 Controller Stage*

4.4.1 Power Supply and Decoupling Capacitors

The power is provided to the motor control chip from the output of LNK3202D buck circuit. Bypass capacitor C10 is placed close to the VDD pin for decoupling to improve chip performance. C9 and C19 provides decoupling to the +5 V LDO output pin (VREG) and +7.5 V OTP programming pin (VPP) respectively.

4.4.2 Speed Control Interface

IC PT2505 has I^2C, external DC and PWM control input to change the motor speed via VSP pin. In this application DC voltage input (V_{SP}) is used. The control parameter setting and V_{SP} range (V_{SPMAX} and V_{SPMIN}) are controlled via register settings. Diodes D3 and D4 in series are optional which is used to achieve a 2.1 V $V_{SPMIN.}$ VR1 provides the clamping action when V_{SP} exceeds maximum setting with R23 as the current limiting resistor.

4.4.3 Hall Sensor Interface

IC PT2505 supports two hall configurations (hall element or hall sensor IC) at 60 degrees or 120 degrees electrical spacing. This application example uses three hall elements (U5, U6, U7) at 120 degrees electrical spacing selected through a register internal setting. Capacitor C12 provides decoupling of the hall bias supply (HB) while C13, C14, and C15 provide high frequency bypass for each hall element output to the IC input pins respectively.

4.4.4 Pulse Output for Speed Information

Output pin FG provides revolution pulse output proportional to the motor speed. Q1, C18, and R17 provide an interface to the FG terminal output, which is to be connected to an external pull up supply. Resistor R17 limits the sinking current to the FG pin <5 mA. Acceptable pullup voltage range is 5 V to 15 V. Pulse output and speed relation can be set through registers internal setting.

4.4.5 PWM Output

The respective high-side and low-side PWM outputs UH, VH, WH, UL, VL, WL connect to each BrigeSwitch devices \INH and INL pins controlling the high-side and low-side FREDFET switching state to commutate the motor.

4.4.6 System Overvoltage and Undervoltage Protection

The system over/under voltage protection is achieved through voltage sensing of the ROVP pin. Any voltage over the OV and under UV threshold will stop the motor operation. OC PT2505 supports multi-level undervoltage thresholds to achieve different operation range through register internal settings.

4.4.7 System and Internal Over-current Protection

The PT2505 has a two-level current protection function via sensed voltage on the RF pin (V_{RF}). In this design example, the instantaneous phase current information (IPH) - internal feature of each BridgeSwitch device was used to provide a reference voltage V_{RF} - that represents the instantaneous motor current. Resistor R19 provides the IPH output voltage scaling with its output fed to a low pass filter through R18 and C17. V_{OCPL} threshold will result to a PWM duty cycle reduction until V_{RF} is less that V_{OCPL} while V_{OCPH} threshold will result to PWM turnoff and the motor will go in lock on protection. These threshold settings can be configured via controller register settings.

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Internal programmable overcurrent protection on both high-side and low-side FREDFET of BridgeSwitch provides an independent, hardware based level over-current protection in case of any abnormal condition such a motor winding short, stalled motor and phase disconnection.

4.4.8 System Over-temperature Protection

The PT2505 supports external or internal over-temperature protection through register internal settings. This application utilizes the external over-temperature protection using an NTC thermistor (RT1) in a resistor divider configuration with R14.

4.4.9 PTC BLDC UI Kit Interface

The on-board terminals SDA, SCL, VPP, FG' and GND provide the interface to the PTC BLDC UI Kit connected to PC via USB interface enabling the use PTC Graphical User Interface (GUI). It allows performing various actions such as registers parameter modification, registers parameter reading, OTP parameter reading and burning, motor instant control and status display. This capability offers the control flexibility for different application requirement using the same type of motor.

4.5 *Three-phase Inverter Stage*

The three BridgeSwitch devices U1, U3, and U8 form the 3-phase inverter. The outputs of the inverter connect to each phase of the motor respectively.

4.5.1 Self-Supply Operation

Capacitors C5, C11, and C22 provide self-supply decoupling for the integrated low-side controller and gate driver. Internal high-voltage current sources recharge them as soon as the voltage level starts to dip. Capacitors C1, C6, and C16 provide self-supply decoupling for the integrated high-side controller and gate driver. Internal high-voltage current sources recharge them whenever the half-bridge point of the respective device drops to the low-side Source voltage level (i.e. the low-side FREDFET turns on).

4.5.2 PWM Input

Input signals UH, UL, VH, VL, WH, and WL control the switching state of the integrated high side and low side power FREDFETs. Series gate resistors R5, R6, R13, R15, R21 and R22 are placed to maintain the PWM outputs signal integrity.

4.5.3 Local Decoupling Capacitor

Capacitor C7 provide decoupling of the high-voltage DC bus local to BridgeSwitch devices U1, U3, and U8. Capacitor C7 provides a local decoupling on the inverter circuit to help reducing the induced negative voltage spikes on the half-bridge due to parasitic inductances.

4.5.4 Cycle-by-Cycle Current Limit

Resistors R7, R16, R24, R4, R12, and R20 set the cycle-by-cycle current limit level for the integrated low-side and high-side power FREDFETs. The selected value of 44.2 kΩ sets it to 100% of the default level or 0.7 A.

4.5.5 Instantaneous Phase Current Information

Each BRD1260C provides instantaneous phase current information through its IPH output tied together across resistor R19. The voltage across R19 is fed to a low pass filter then to the controller current limit voltage sense (RF) pin to provide the over-current protection mechanism. The device IPH current gain is 400 μA/A.

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5 Printed Circuit Board Layout

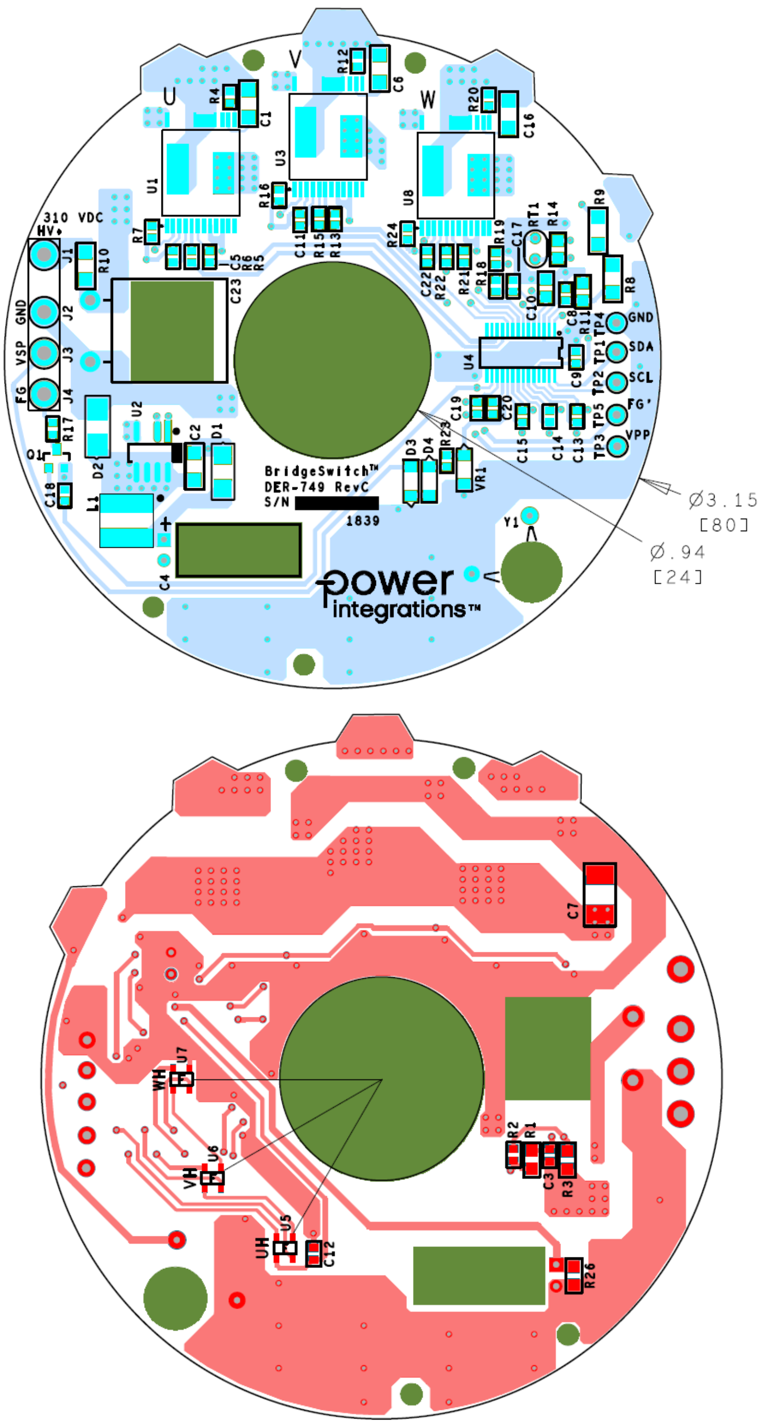

Figure 4 – Printed Circuit Board Layout Top and Bottom View.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	R10	RES, 0.22 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ8RQJR22U	Panasonic
2	1	R8	RES, 1 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ105 V	Panasonic
3	1	R9	RES, 1 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ105 V	Panasonic
4	3	C13, C14, C15	1 nF, 25 V, Ceramic, X7R, 0603	GRM188R71E102KA01D	Murata
5	5	C5, C10, C11, C17, C22	1 uf 35 V, Ceramic, X7R, 0603	C1608X7R1V105M	TDK
6	1	C10	1 uf 50 V, Ceramic, X7R, 0805	08055D105KAT2A	AVX
7	6	R5, R6, R13, R15, R21, R22	RES, 10 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ100V	Panasonic
8	1	C18	10 nF, 0.01 μF, ±10%, 25 V, Ceramic, X7R, 0603	CL10B103KA8NFNC	Samsung
9	1	C2	10 μF, 10%, 50V, Ceramic, X7R, 1206	CL31B106KBHNNNE	Samsung
10	1	R17	RES, 100 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ101V	Panasonic
11	1	RT1	NTC Thermistor, 100 kΩ, 1%, 30 mm leads, -40 C to +125 C	NXFT15WF104FA1B030	Murata
12	5	C3, C9, C12, C19, C20	100 nF 25 V, Ceramic, X7R, 0603	VJ0603Y104KNXAO	Vishay
13	1	C8	100 pF 50 V, Ceramic, NP0, 0603	CC0603JRNPO9BN101	Yageo
14	1	Y1	100 pF, 250 VAC, Film, X1Y1	DE1B3KX101KB4BN01F	TDK
15	1	C4	100 μF, 35 V, Electrolytic, Low ESR, 180 mΩ, (6.3 x 15)	ELXZ350ELL101MF15D	Nippon Chemi-Con
16	1	C23	FILM, 0.12 μF, 5%, 450 VDC, RADIAL	ECW-FD2W124J4	Panasonic
17	1	R11	RES, 18 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ183V	Panasonic
18	2	D3, D4	Diode, GEN PURP, 100 V, 150 mA, SOD123	1N4148W RHG	Taiwan Semi
19	1	R23	RES, 2 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF2001V	Panasonic
20	1	R19	RES, SMD, 2.4 KΩ, 1%, 1/10W, 0603	RC0603FR-072K4L	Yageo
21	1	R3	RES, 2.49 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF2491V	Panasonic
22	1	C7	220 nF, 500 V, Ceramic, X7R, 1812	C1812C224KCRACTU	Kemet
23	1	R2	RES, 25.5 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF2552V	Panasonic
24	1	R14	RES, 32.4 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF3242V	Panasonic
25	1	R18	RES, 4.7 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ4R7V	Panasonic
26	3	C1, C6, C16	4.7 μF, ±10%, 25 V, Ceramic, X7R, 1206	GCM31CR71E475KA55L	Murata
27	6	R4, R7, R12, R16, R20, R24	RES, 44.2 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF4422V	Panasonic
28	1	L1	680 μH, ±20%, Shielded, Wire wound, 165 mA, 3.77 Ω	PA4300.684NLT	Pulse
29	1	R26	RES, 8.06 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF8061V	Panasonic
30	1	R1	RES, 91 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ913V	Panasonic
31	5	TP1, TP2, TP3, TP4, TP5	Test Point, BLK, Miniature THRU-HOLE MOUNT	5001	Keystone
32	3	U1, U3, U8	BridgeSwitch, Full Featured, Max. BLDC Motor Current 0.7 A (RMS)	BRD1260C	Power Integrations
33	1	D2	600 V, 1 A, Glass Passivated, DO-214AC	CD214A-F1600	Bourns
34	4	J1, J2, J3, J4	Flying Lead , Hole size 70mils	N/A	N/A
35	3	U5, U6, U7	IC, Hall Effect Sensor, Single Axis, Linear, Analog 4-SOP	HW101A	AKM Semi
36	1	U2	LinkSwitch-TN2, LNK3202D, SO-8C	LNK3202D	Power Integrations
37	1	Q1	NPN, Small Signal BJT, GP, 40V, 600 mA, 250 MHz, 300 mW , SOT-23,	MMBT4401LT3G	On Semi
38	1	VR1	DIODE ZENER 5.6V 500MW SOD123	MMSZ5232B-7-F	Diodes, Inc.
39	1	U4	IC, DC motor control, 3 phase, hall sensor, sinusoidal, brushless DC	PT2505	Princeton
40	1	D1	600 V, 1 A, Standard Recovery, SMA	S1J-13-F	Diodes, Inc.

Table 2 – Bill of Materials.

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7 Performance Data

This section presents waveform plots and performance data gathered on the DER-749. The HV bus voltage level is 310 VDC unless stated otherwise. A 400V 120 μF bulk capacitor is placed at the HV bus input. All measurements were performed at room ambient temperature.

7.1 *Start-up Operation*

Figure 5 and 6 shows the motor start-up waveforms at no load and 0.1 N-m load respectively. Proper power up sequence follows applying a high-voltage dc input first then the speed input voltage (V_{SP}). Typically, motor will start at 2.1 V V_{SP} voltage.

At motor start-up, the initial position is known according to the Hall sensors outputs. The controller uses 6-step control commutation before entering normal state with sinusoidal commutation as depicted in the following waveform plots.

The maximum start-up torque can be changed by modifying the start-up maximum duty to suit different motor application. The profile can be set from the PTC GUI parameter settings. In this design example, the driver is configured to allow the motor to start up to 0.1 N-m load.

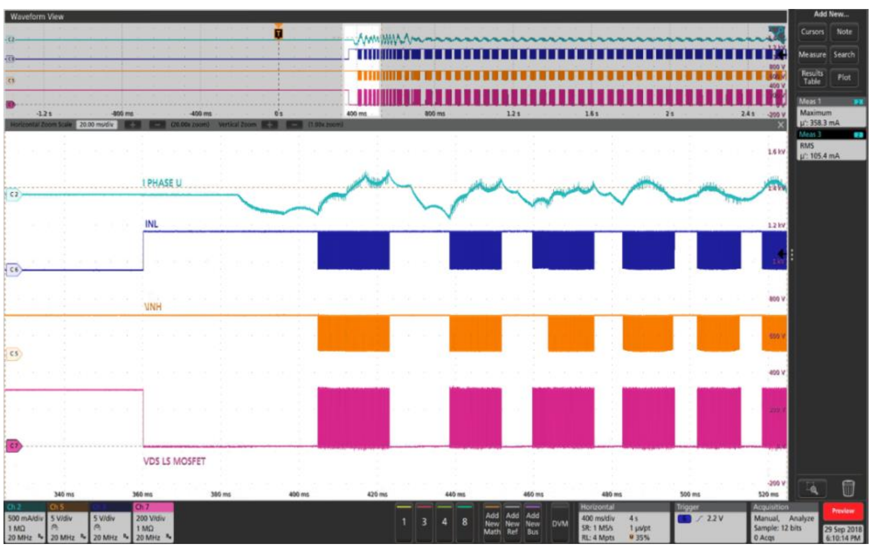

Figure 5 – Start-Up at No Load.
First: $I_{MOTOR\ (PHASE\ U)}$, 500 mA / div.
Second: $V_{INL\ (PHASE\ U)}$, 5 V / div.
Third: $V_{\backslash INH\ (PHASE\ U)}$, 5 V / div.
Fourth: $V_{DS\text{-}LS\ (PHASE\ U)}$, 200 V / div., 20 ms / div.

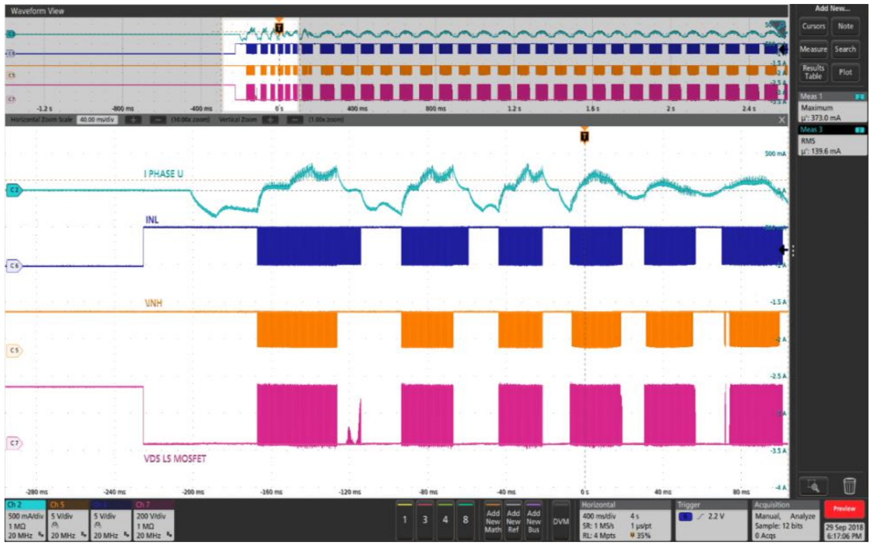

Figure 6 – Start-Up at 0.1 N-m Load.
First: $I_{MOTOR\ (PHASE\ U)}$, 500 mA / div.
Second: $V_{INL\ (PHASE\ U)}$, 5 V / div.
Third: $V_{\backslash INH\ (PHASE\ U)}$, 5 V / div.
Fourth: $V_{DS\text{-}LS\ (PHASE\ U)}$, 200 V / div., 20 ms / div.

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7.2 *Steady-State Operation*

7.2.1 Steady-State Waveforms at 0.1 N-m Load

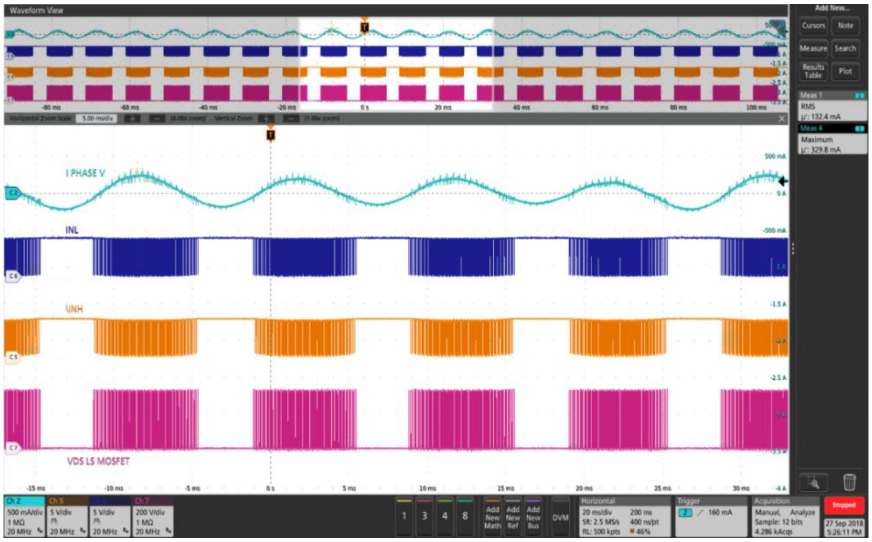

Figure 7 – Steady-State Waveforms at 0.1 N-m Load, 1500 RPM.
First: $I_{MOTOR\ (PHASE\ V)}$, 500 mA / div.
Second: $V_{INL\ (PHASE\ V)}$, 5 V / div.
Third: $V_{\backslash INH\ (PHASE\ V)}$, 5 V / div.
Fourth: $V_{DS-LS\ (PHASE\ V)}$, 200 V / div., 5 ms / div.

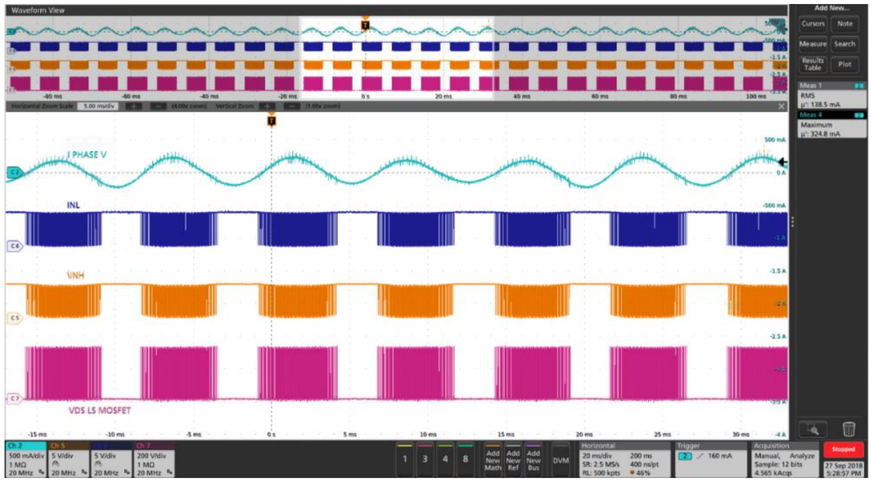

Figure 8 – Steady State Waveforms at 0.1 N-m load, 2000 RPM.
First: $I_{MOTOR\ (PHASE\ V)}$, 500 mA / div.
Second: $V_{INL\ (PHASE\ V)}$, 5 V / div.
Third: $V_{\backslash INH\ (PHASE\ V)}$, 5 V / div.
Fourth: $V_{DS\text{-}LS\ (PHASE\ V)}$, 200 V / div., 5 ms / div.

7.2.2 Steady-State Waveforms at 0.2 N-m Load

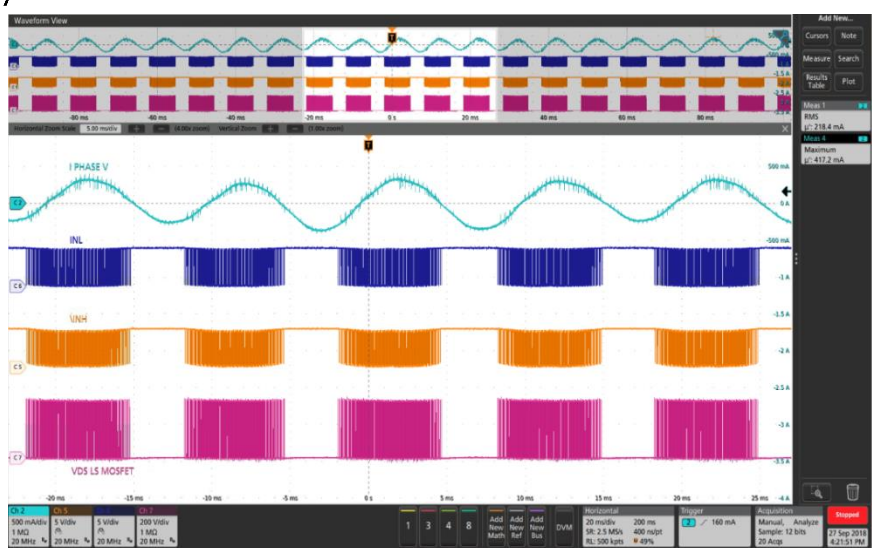

Figure 9 – Steady-State Waveforms at 0.2 N-m Load, 1500 RPM.
First: $I_{MOTOR\ (PHASE\ V)}$, 500 mA / div.
Second: $V_{INL\ (PHASE\ V)}$, 5 V / div.
Third: $V_{\backslash INH\ (PHASE\ V)}$, 5 V / div.
Fourth: $V_{DS\text{-}LS\ (PHASE\ V)}$, 200 V / div., 5 ms / div.

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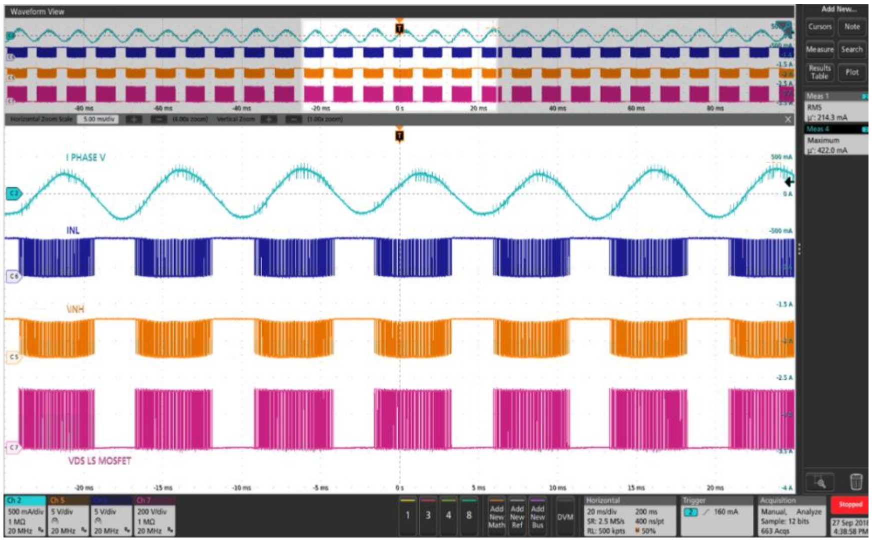

Figure 10 – Steady-State Waveforms at 0.1 N-m Load, 2000 RPM.
First: $I_{MOTOR\ (PHASE\ V)}$, 500 mA / div.
Second: $V_{INL\ (PHASE\ V)}$, 5 V / div.
Third: $V_{\backslash INH\ (PHASE\ V)}$, 5 V / div.
Fourth: $V_{DS\text{-}LS\ (PHASE\ V)}$, 200 V / div., 5 ms / div.

7.2.3 Speed Pulse Output

The motor speed monitor is provided from the FG output terminal (J4) as a logic level pulse frequency. FG should connect to an external pull-up supply with range from 5 V to 15 V. In this design example, FG output frequency is set from the register to be 3 times the electrical speed/frequency (FG = 3* F $_{Hz}$). Motor actual speed can be calculated given FG output frequency as speed (RPM) = FG $_{Hz}$ *5.

Figure 11 to 13 depicts the FG output at 1500 RPM and 2000 RPM for 0.1 N-m and 0.2 N-load torque respectively. FG terminal is connected to +5 V external pull-up with 10 kΩ resistor.

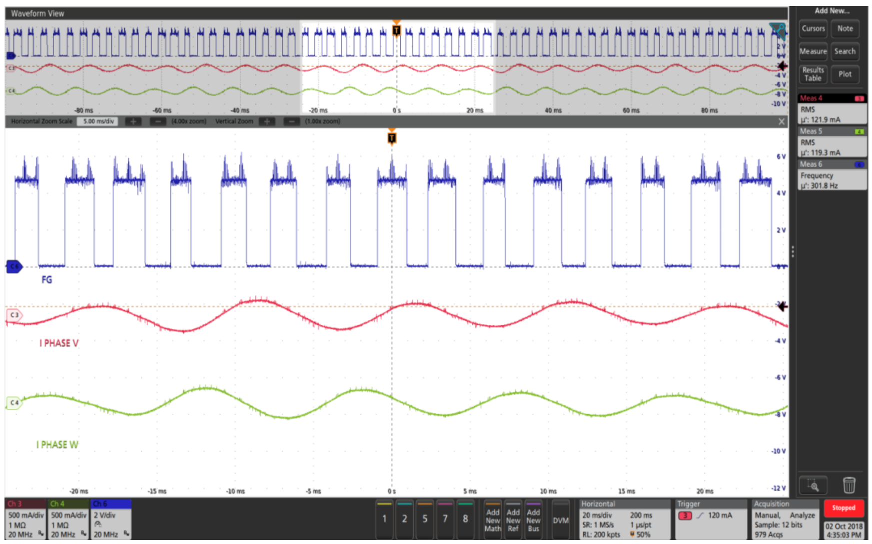

Figure 11 – Speed Pulse Output at 0.1 N-m Load, 1500 RPM.
First:. V_{FG} , 2 V / div.
Second: $I_{MOTOR\ (PHASE\ V)}$, 500 mA / div.
Third: $I_{MOTOR\ (PHASE\ W)}$, 500 mA / div., 5 ms / div.
FG Output Frequency: 301.8 Hz.

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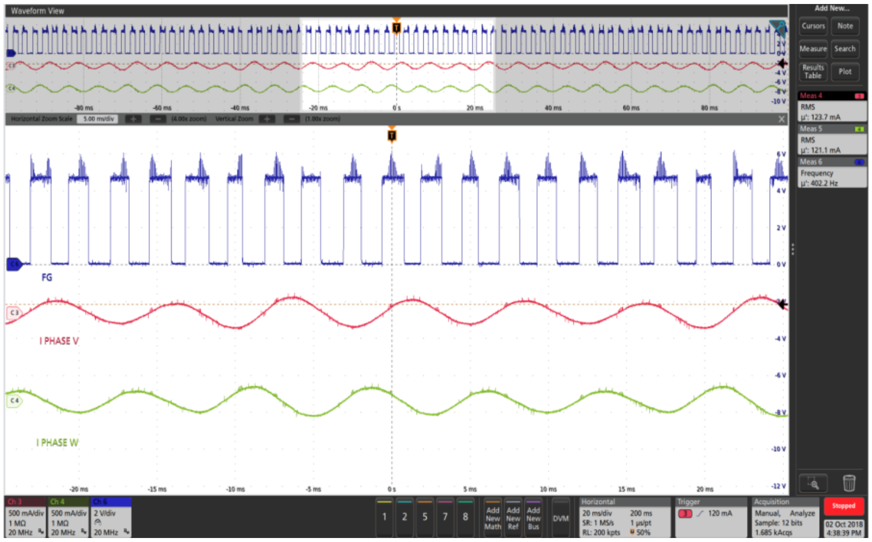

Figure 12 – Speed Pulse Output at 0.1 N-m Load, 2000 RPM.
First:. V_{FG} , 2V / div.
Second: $I_{MOTOR\ (PHASE\ V)}$, 500 mA / div.
Third: $I_{MOTOR\ (PHASE\ W)}$, 500 mA / div., 5 ms / div.
FG Output Frequency: 402.2 Hz.

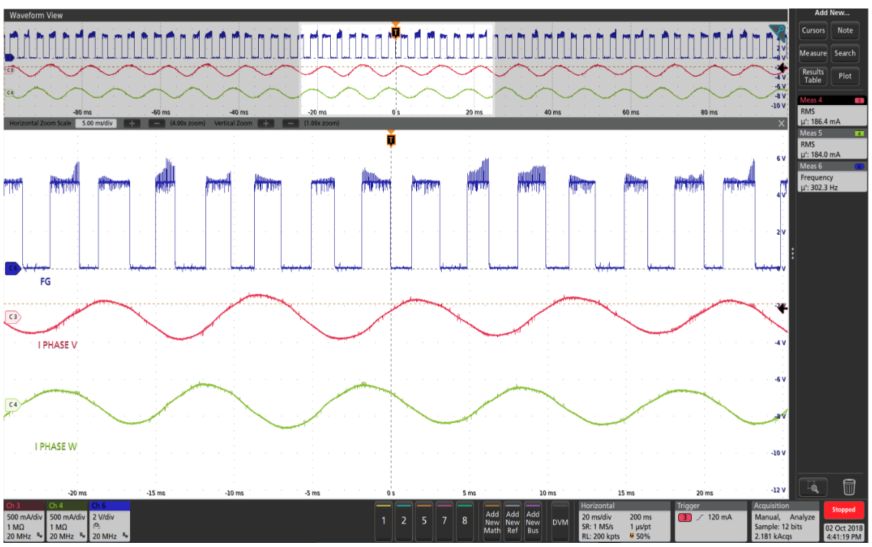

Figure 13 – Speed Pulse Output at 0.2 N-m Load, 1500 RPM.
First:. V_{FG} , 2V / div.
Second: $I_{MOTOR\ (PHASE\ V)}$, 500 mA / div.
Third: $I_{MOTOR\ (PHASE\ W)}$, 500 mA / div., 5 ms / div.
FG Output Frequency: 302.3 Hz.

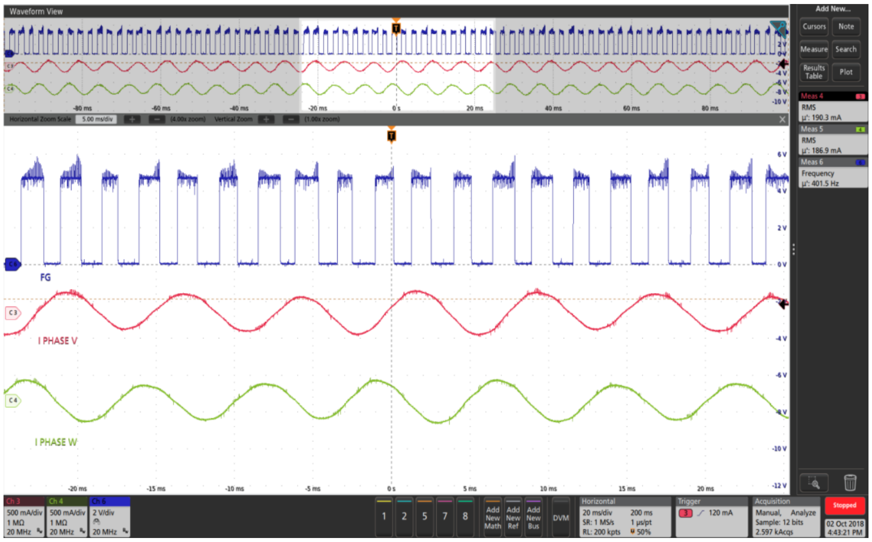

Figure 14 – Speed Pulse Output at 0.1 N-m Load, 2000 RPM.
First:. V_{FG} , 2V / div.
Second: $I_{MOTOR\ (PHASE\ V)}$, 500 mA / div.
Third: $I_{MOTOR\ (PHASE\ W)}$, 500 mA / div., 5 ms / div.
FG Output Frequency: 401.5 Hz.

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7.2.4 Motor Speed Profile

PT2505 offers I^2C, external DC and PWM input control to change the motor speed. In this design example, the motor speed is controlled through external DC input on the VSP terminal input (J3). For external DC input speed control, VSP range can be set through register settings as well as the maximum speed setting. In this design example, the motor speed is limited to ~2400 RPM.

Figure 15 depicts the motor speed profile vs. VSP voltage (V_{SP}) at 0.1 N-m and 0.2 N-m load respectively.

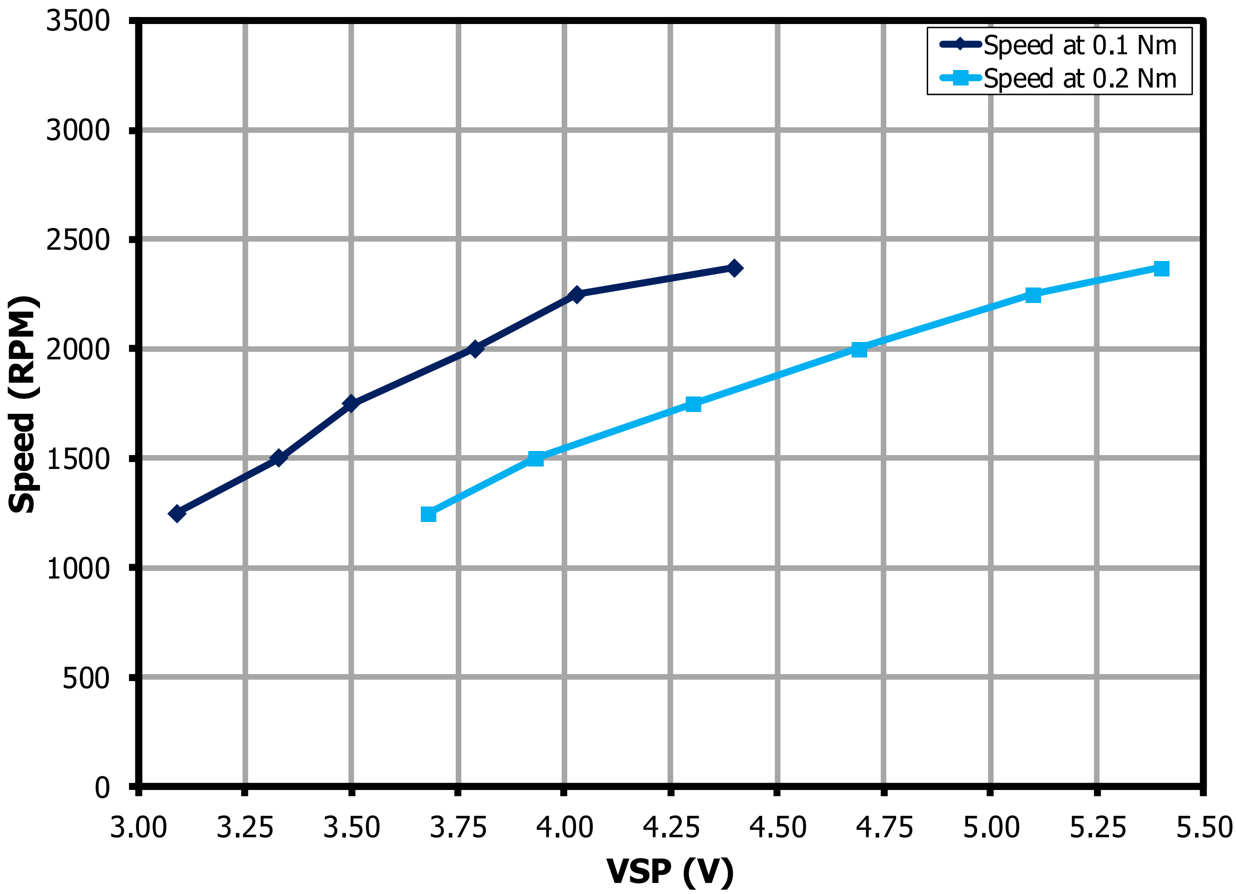

Figure 15 – Motor Speed Profile.

7.3 *Thermal Performance*

Figure 16 and Figure 17 depicts the open case on-board thermal scan of BridgeSwitch devices (U1, U3, U8) and the motor control chip (U1) after 30 minutes of operation running at 1500 RPM at 0.1 N-m and 0.2 N-m load respectively at ~26 ºC ambient temperature.

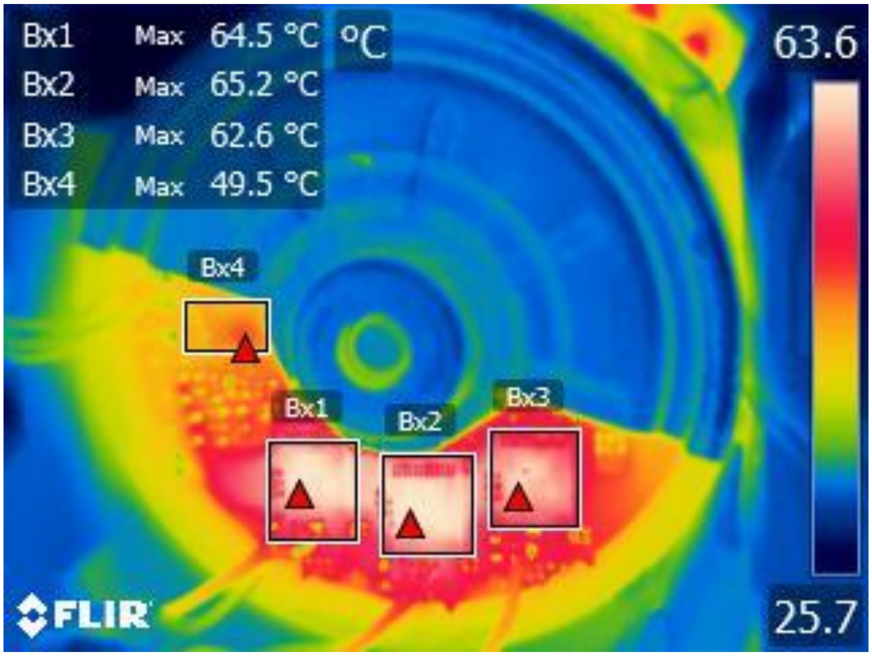

Figure 16 – Thermal Scan at 0.1 N-m Load.

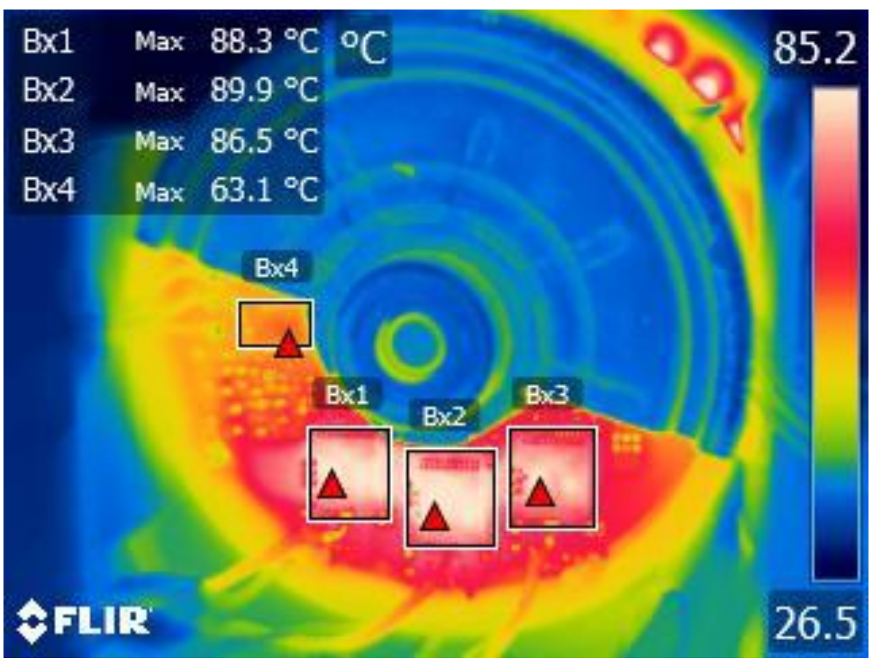

Figure 17 – Thermal Scan at 0.2 N-m Load.

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7.4 *No-Load Power Consumption*

Figure 18 depicts the BridgeSwitch inverter and the system (inverter including the LinkSwitch-TN2 auxiliary and PT2505 controller circuit) no-load input power consumption measured across the input line voltage.

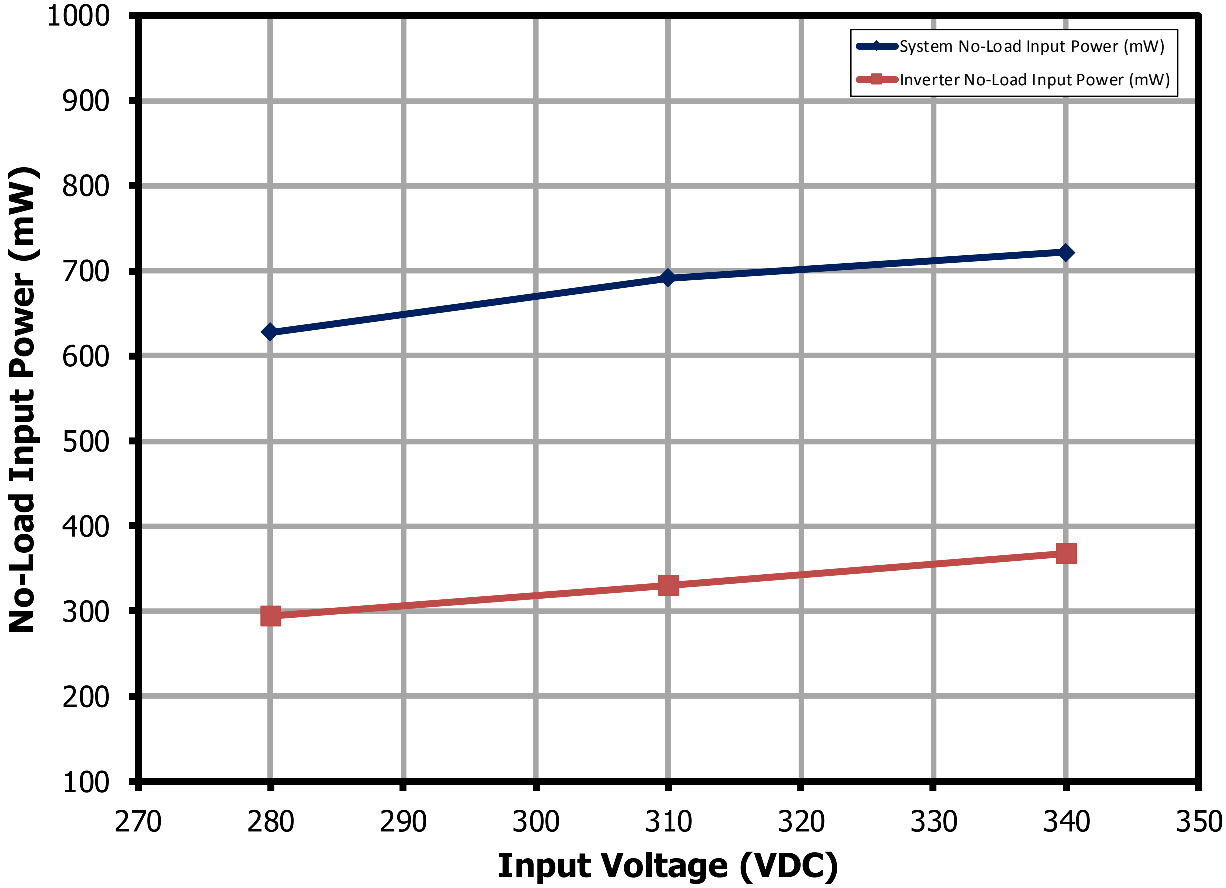

Figure 18 – No-Load Input Power.

7.5 *Efficiency*

Figure 19 and Figure 20 depicts the inverter efficiency at 310 V input voltage at torque loads of 0.1 N-m and 0.2 N-m versus motor speed and output power respectively.

The inverter efficiency denotes inverter stage efficiency only. It does not include the power consumption from the LinkSwitch-TN2 auxiliary supply circuit.

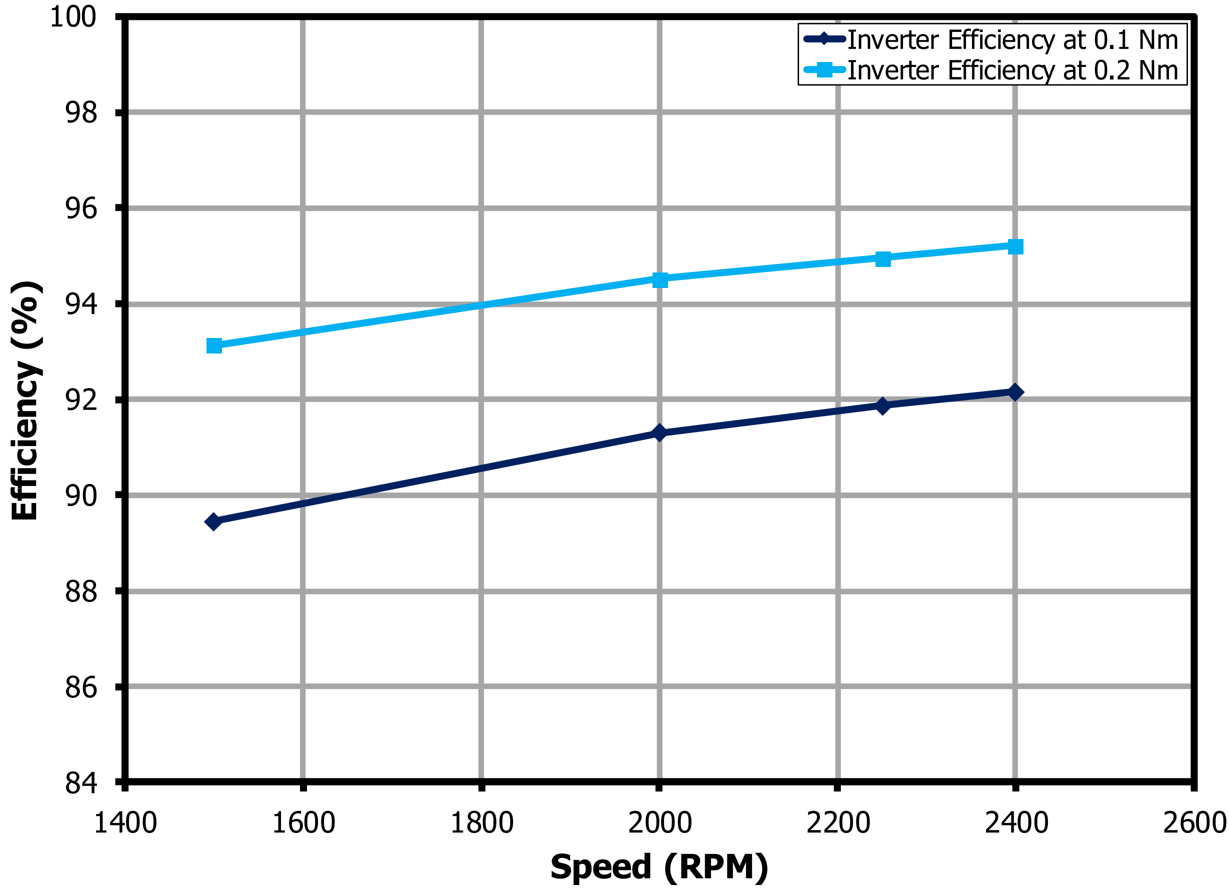

Figure 19 – Inverter Efficiency vs. Speed.

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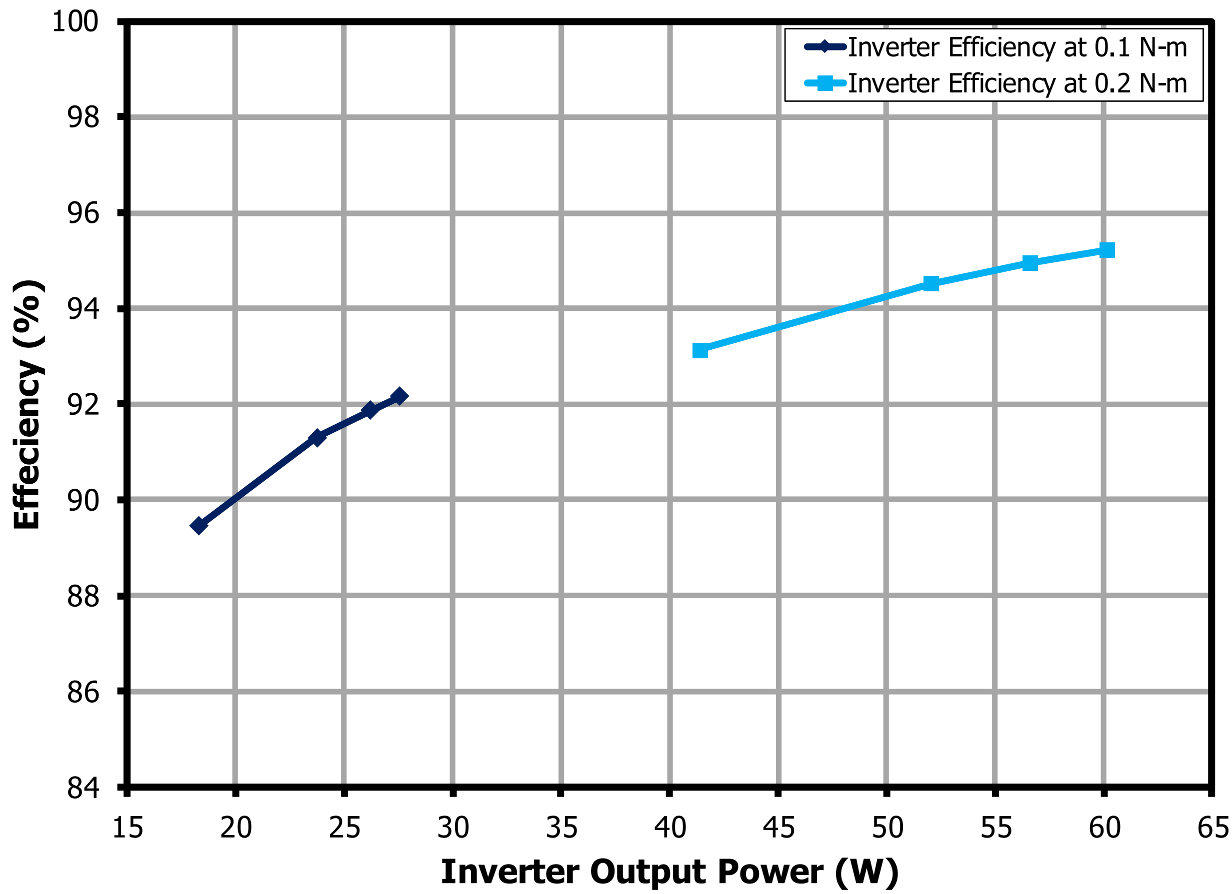

Figure 20 – Inverter Efficiency vs Output Power

Table 3 and 4 shows the data from the efficiency graph described.

Input DC Voltage (V)	Speed (RPM)	DC Input Power (W)	Motor RMS Current Phase U (A)	Motor RMS Current Phase V (A)	Motor RMS Current Phase W (A)	Inverter Output Power (W)	Inverter Efficiency (%)
311	1500	0.1457	0.1470	0.1451	0.1457	18.28	89.5
311	2000	0.1556	0.1571	0.1551	0.1556	23.75	91.3
311	2250	0.1599	0.1619	0.1595	0.1599	26.23	91.9
311	2400	0.1624	0.1644	0.1619	0.1624	27.56	92.2

Table 3 – Efficiency Table at 0.1 N-m load.

Input DC Voltage (V)	Speed (RPM)	DC Input Power (W)	Motor RMS Current Phase U (A)	Motor RMS Current Phase V (A)	Motor RMS Current Phase W (A)	Inverter Output Power (W)	Inverter Efficiency (%)
311	1500	44.4390	0.2110	0.2120	0.2100	41.39	93.1
311	2000	55.0640	0.2064	0.2080	0.2054	52.05	94.5
311	2250	59.6040	0.2044	0.2059	0.2034	56.60	95.0
311	2400	63.1350	0.2049	0.2069	0.2039	60.11	95.2

Table 4 – Efficiency Table at 0.2 N-m load.

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7.6 ***System Level Protection***

This section demonstrates the system-level protection features on the inverter driver. Protection related parameters described can be configured using the PTC GUI software.

7.6.1 Over-current Protection

The system-level over-current protection is achieved using PT2505 two-stage over-current protection (OCPL and OCPH). The motor current information is sensed from the composite IPH signal provided by the three BridgeSwitch devices via R19. When the voltage (V_{RF}) on the sense resistor reaches V_{OCPL}, OCPL condition will be triggered. At this time, the controller will reduce the PWM duty cycle until V_{RF} is less than $V_{OCPL.}$ The driver is configured by reducing PWM duty cycle by 25% when the current reaches ~0.47 A. Figure 21 depicts the OCPL condition.

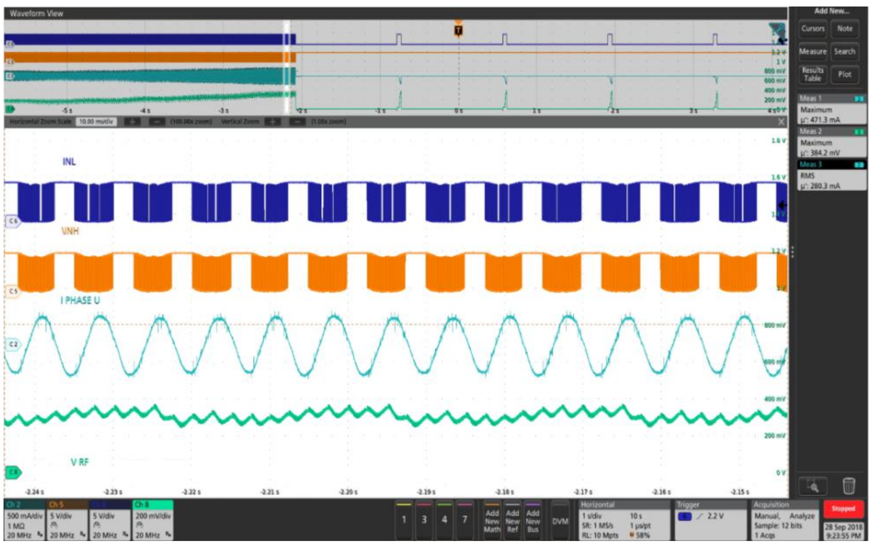

Figure 21 – OCPL Condition PWM Duty Reduced to 25%.
First:. V_{INL} , 5 V / div.
Second: V\$_{INH}$, 5 V / div.
Third: $I_{MOTOR\ (PHASE\ V)}$, 500 mA / div.
Fourth: V_{RF}, 200 mV / div., 10 ms / div.

When V_{RF} exceeds the V_{OCPH}, OCPH condition will be triggered and the PWM will turn off immediately and will go into lock mode. Lock mode protection means the controller will wait a certain period and re-start again (period and re-start times are set through register internal parameters) and the exception number counter will plus one. If the motor remained to be locked and the counter exceeds the max exception setting, it would cause system to go into deadlock status. The system will no longer start at this state and a power cycle is required to restart the system. Figure 22 and Figure 23 shows the PWM turn off and restart condition during OCPH condition ~0.5 A motor current.

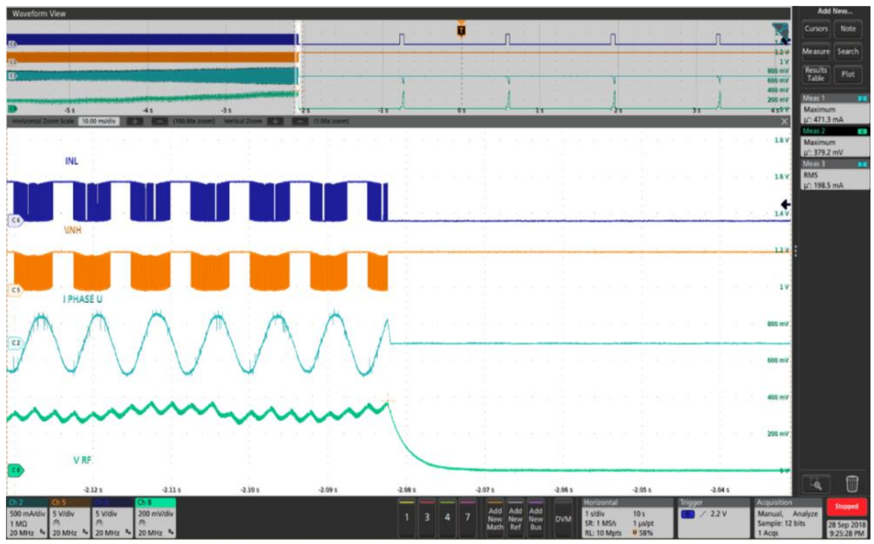

Figure 22 – OCPH Condition PWM Turn Off
First:. V_{INL} , 5 V / div.
Second: $V_{\backslash INH}$, 5 V / div.
Third: $I_{MOTOR\ (PHASE\ V)}$, 500 mA / div.
Fourth: V_{RF}, 200 mV / div., 10 ms / div.

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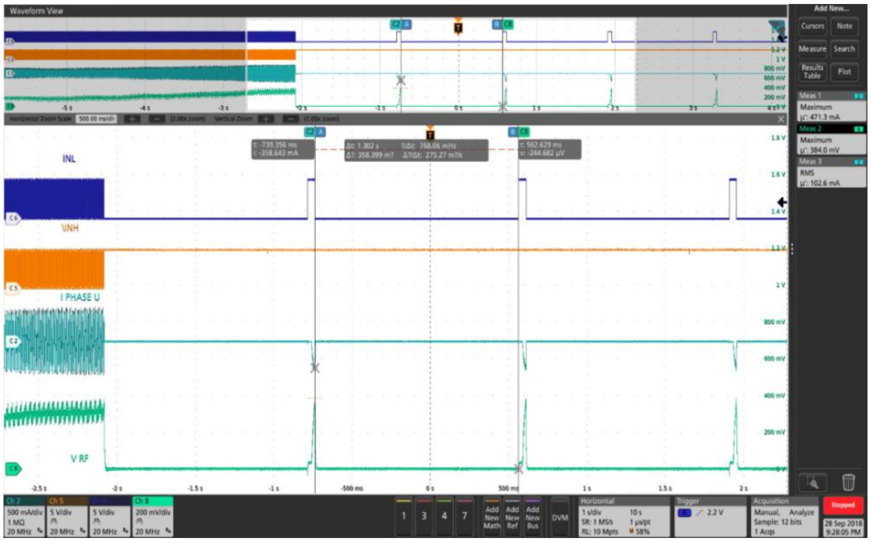

Figure 23 – Retry during OCPH Condition.
First:. V_{INL} , 5 V / div.
Second: $V_{\backslash INH}$, 5 V / div.
Third: $I_{MOTOR\ (PHASE\ V)}$, 500 mA / div.
Fourth: V_{RF}, 200 mV / div., 10 ms / div.

7.6.2 Over/Undervoltage Protection

The system overvoltage and undervoltage protection is achieved using external voltage divider (R8, R9, R11) connected to the chip ROVP pin of PT2505. When ROVP voltage is greater than V_{PRTH} (3.5 V - overvoltage threshold) or less than V_{PRTL} (undervoltage threshold – set through register internal settings) it will enter over/undervoltage protection and the PWM will turn off until the fault is removed.

Figure 24 depicts the overvoltage condition at ~390 V.

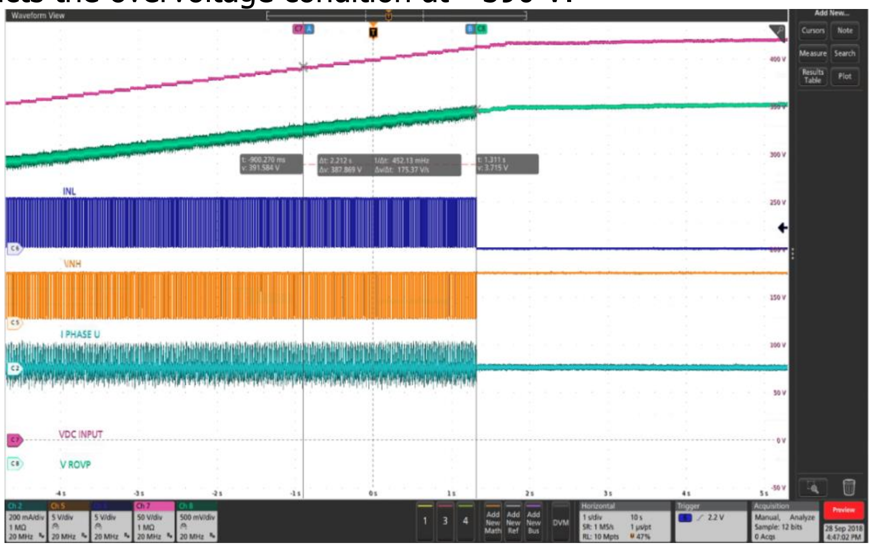

Figure 24 – Overvoltage Condition PWM Turn Off.
First: $V_{HV\ BUS}$, 50 V / div.
Second: V_{ROVP} , 500 mV / div.
Third: V_{INL}, 5 V / div.
Fourth: $V_{\backslash INL}$, 5 V / div.
Fifth: $I_{MOTOR\ (PHASE\ U)}$, 500 mA / div., 1 s / div.

Figure 25 depicts the restart after the overvoltage condition is removed. Figure 26 and 27 depicts the undervoltage protection and restart respectively. Undervoltage protection is set at ~240 V.

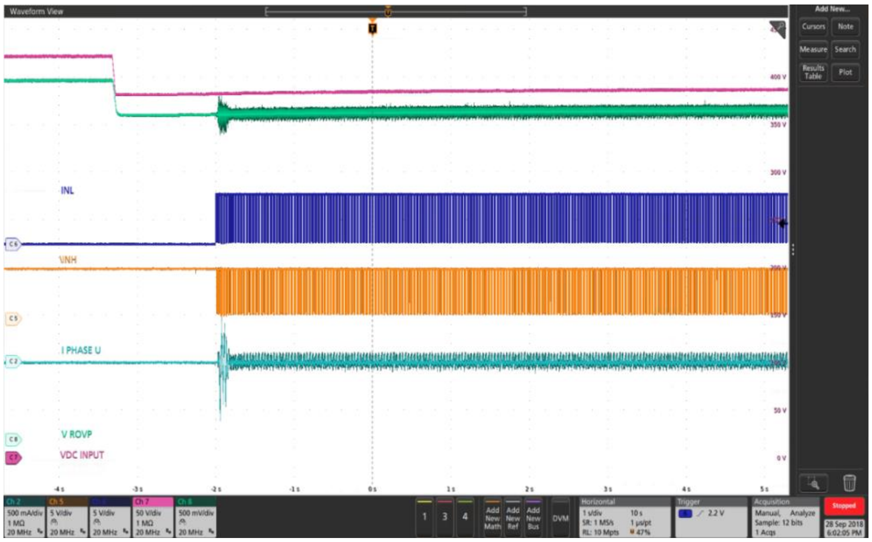

Figure 25 – Restart after Overvoltage Condition is Removed.
First: $V_{HV\ BUS}$, 50 V / div.
Second: V_{ROVP} , 500 mV / div.
Third: V_{INL} , 5 V / div.
Fourth: $V_{\backslash INL}$, 5 V / div.
Fifth: $I_{MOTOR\ (PHASE\ U)}$, 500 mA / div., 1 s / div.

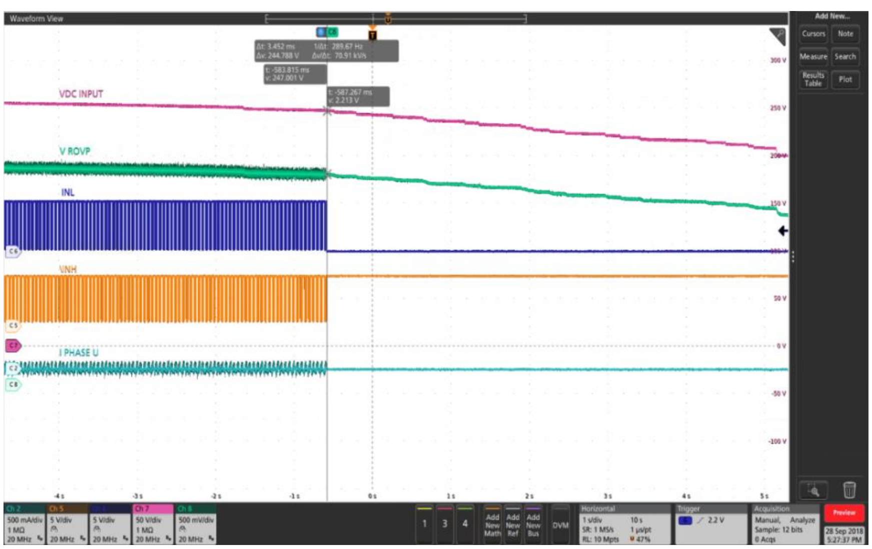

Figure 26 – Undervoltage Condition PWM Turn Off.
First:. $V_{HV\ BUS}$, 50 V / div.
Second: V_{ROVP} , 500 mV / div.
Third: V_{INL} , 5 V / div.
Fourth: $V_{\backslash INL}$, 5 V / div.
Fifth: $I_{MOTOR\ (PHASE\ U)}$, 500 mA / div., 1 s / div.

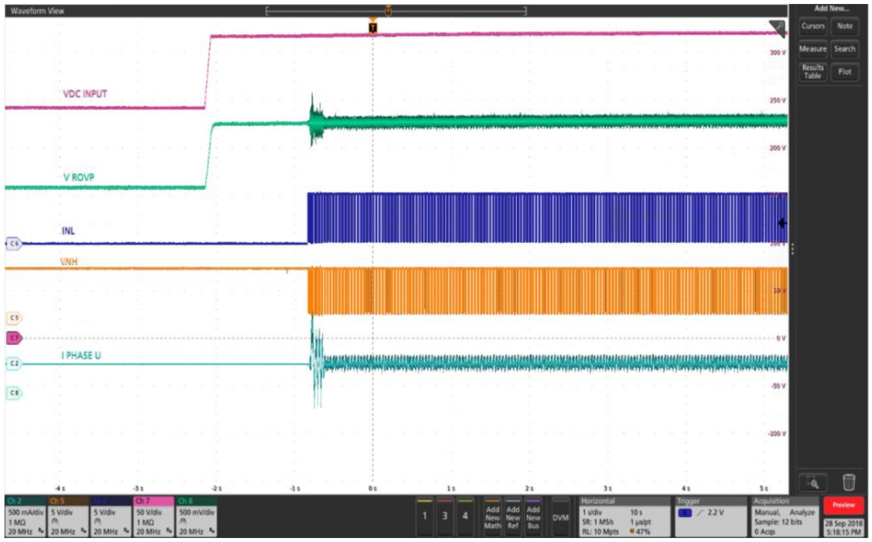

Figure 27 – Restart after Undervoltage Condition is Removed.
First:. $V_{HV\ BUS}$, 50 V / div.
Second: V_{ROVP}, 500 mV / div.
Third: V_{INL}, 5 V / div.
Fourth: $V_{\backslash INL}$, 5 V / div.
Fifth: $I_{MOTOR\ (PHASE\ U)}$, 500 mA / div., 1 s / div.

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7.6.3 System Over-temperature Protection

The system over-temperature is achieved by using an external NTC temperature-sensing resistor (RT1) connected to RTSD pin of PT2505 in series with R14. Over-temperature protection will be triggered when the V_{RTSD} drops to the lower reference (V_{REFL}) voltage 1.2 V then it will be released once V_{RTSD} is greater than the higher reference (V_{REFH}) 2.6 V.
In this design example, the inverter board will trigger over-temperature protection around 95 ºC and will restart around 45 ºC ambient temperature.

Figure 28 and 29 depicts the over-temperature condition and restart after the over-temperature condition respectively.

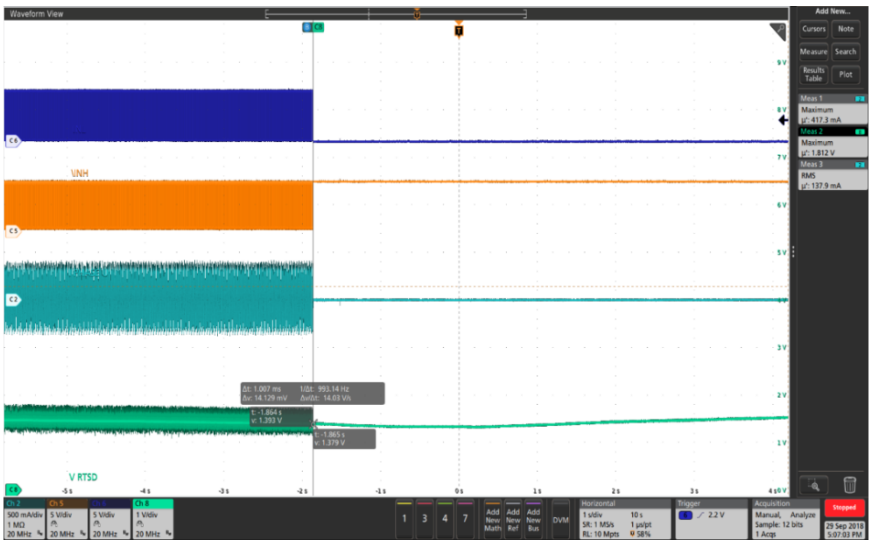

Figure 28 – Over-temperature Condition PWM Turn Off.
Fist: V_{INL} , 5 V / div
Second: $V_{\backslash INL}$, 5 V / div.
Third: $I_{MOTOR\ (PHASE\ U)}$, 500 mA / div.
Fourth: V_{RTSD}, 1 V / div., 1 s / div.

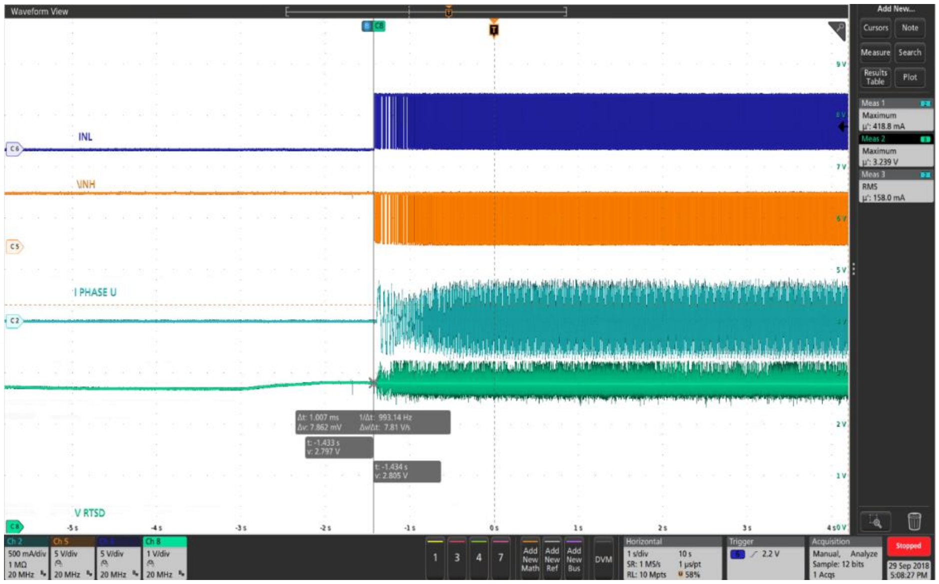

Figure 29 – Restart after Over-temperature Condition
Fist: V_{INL} , 5 V / div
Second: $V_{\backslash INL}$, 5 V / div.
Third: $I_{MOTOR\ (PHASE\ U)}$, 500 mA / div.
Fourth: V_{RTSD}, 1 V / div., 1 s / div.

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8 Appendix

8.1 *Inverter Circuit Board Manual*

Figure 30 shows locations and functions of all connectors to and from the inverter board.

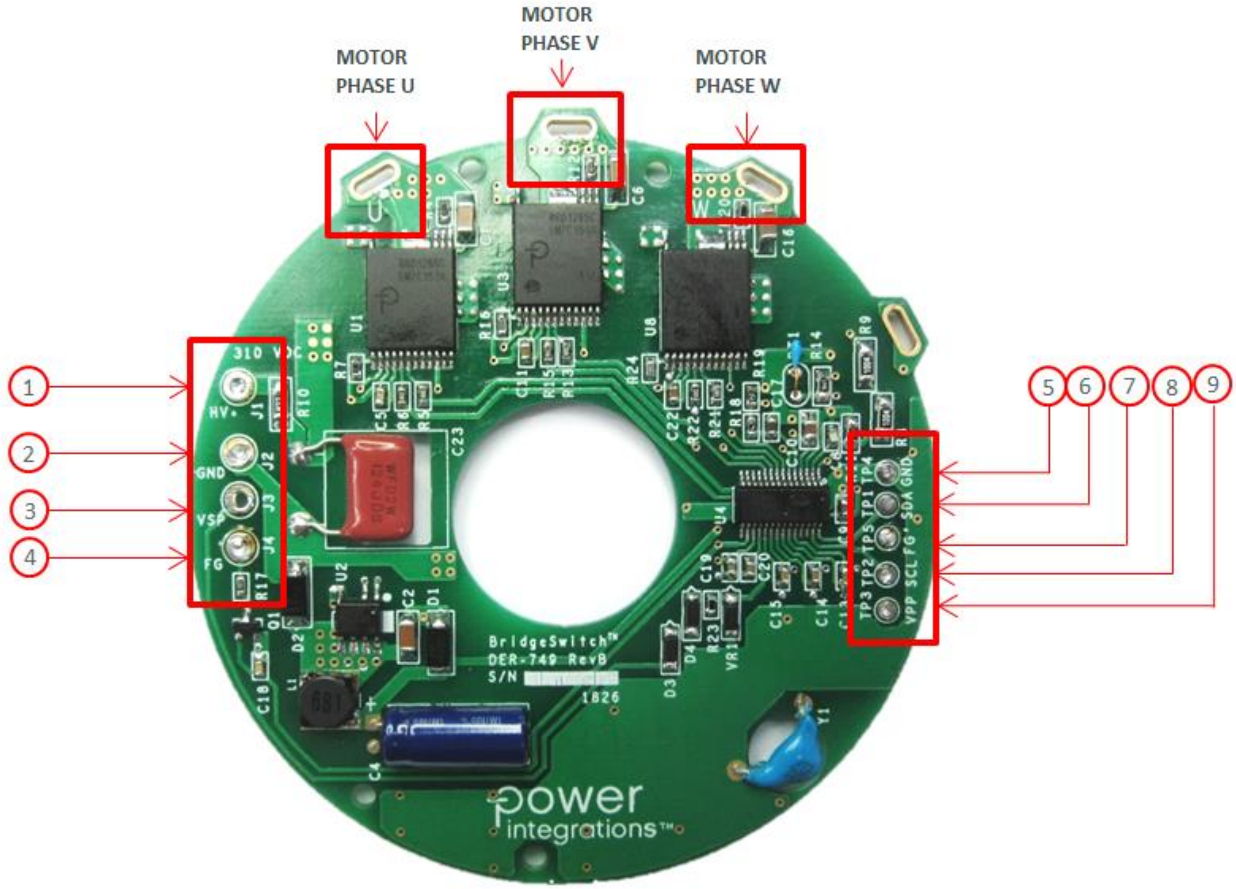

Figure 30 – DER-749 Connections (Top View).

The high-voltage DC bus connects to the inverter through two through-hole mount terminal points, J1 and J2. The positive input terminal should connect to J1, and the negative input terminal should connect to J2.

Speed control input signal (VSP) connects to terminal J3 and speed output monitor (FG) connect to the terminal J4. Programming interface to the PTC BLDC UI Kit connects to TP1, TP2, TP3, TP4 and TP5 respectively. Motor phase winding connects to Phase U, Phase V and Phase W terminals. See Table 5 for each pin connection description.

Table 5 lists the input and output signals and programming interface connections on the inverter board.

Pin No.	Signal	Type	Comments
1	HV^+	Input	High-voltage bus input supply (310Vdc typical)
2	GND	n/a	Power ground connection
3	VSP	Input	DC input speed control voltage (2.1 V – 5.4 V)
4	FG	Output	Pulse output monitor for rotation speed information. Should pull-up to external supply (5 V – 15 V)
5	GND	n/a	Signal ground connection
6	SDA	Input/Output	Serial data I^2C control interface
7	FG'	Input	Input for system clock trimming
8	SCL	Input	Serial clock input I^2C interface
9	VPP	Input	+7.5 V for OTP programming, provided internally from PTC BLDC UI Kit

Table 5 – Input/Output, and Programming Interface Connector Pinout.

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8.2 ***Test Bench Set-up***

Figure 31 depicts the test bench used to gather the performance data presented in this report. It consists of:

- 3-phase inverter using BRD1260C with PT2505 in sinusoidal commutation logic
- 310VDC, 8 poles BLDC motor (Foshan Lepuda PLD-39-8-1)
    - Alternate motor: WZDK-38G-2 30W 310VDC 8P BLDC motor
- Electro-mechanics hysteresis brake (HB-103)
- Programmable DC input source
- Bench power supply
- Motor brake controller (ICS-2000)

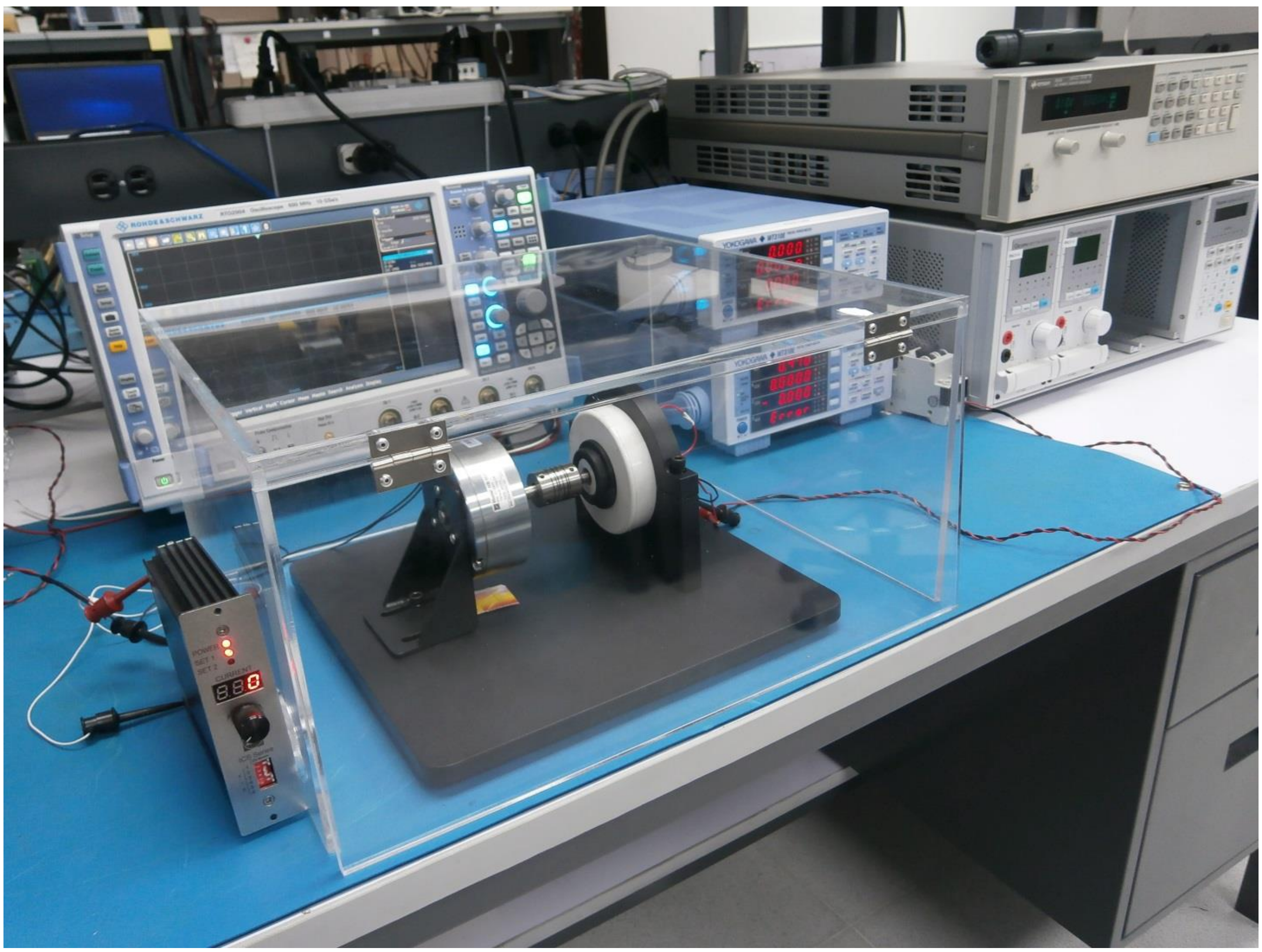


Figure *31* **–** Test Bench Set-up.

8.3 ***PTC BLDC UI Kit***

The PT2505 provides a BLDC User Interface (UI) Kit to work with their Graphical User Interface (GUI) software for OTP parameter settings. For complete instruction of how to use the UI Kit and parameter settings using GUI, PTC provides a detailed instruction documented in the application note. To obtain the PTC BLDC UI Kit and software, please contact PTC sales or their customer contact window.

8.3.1 BLDC UI (I2C-to-USB) Kit

The PTC BLDC UI Kit needs to be connected to the PC/NB via the USB interface. With the GUI software, the following actions can be performed on the PT2501/PT2502/PT2505/PT2511 and other ICs:

- Temporary parameter modification
- Register parameter reading
- OTP parameter burning
- OTP parameter reading
- Motor instant control
- Motor status display

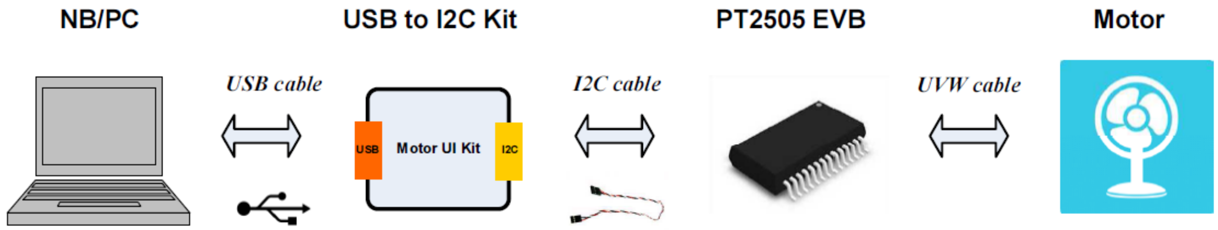


Figure 32 – PTC BLDC UI Kit Connection Diagram.

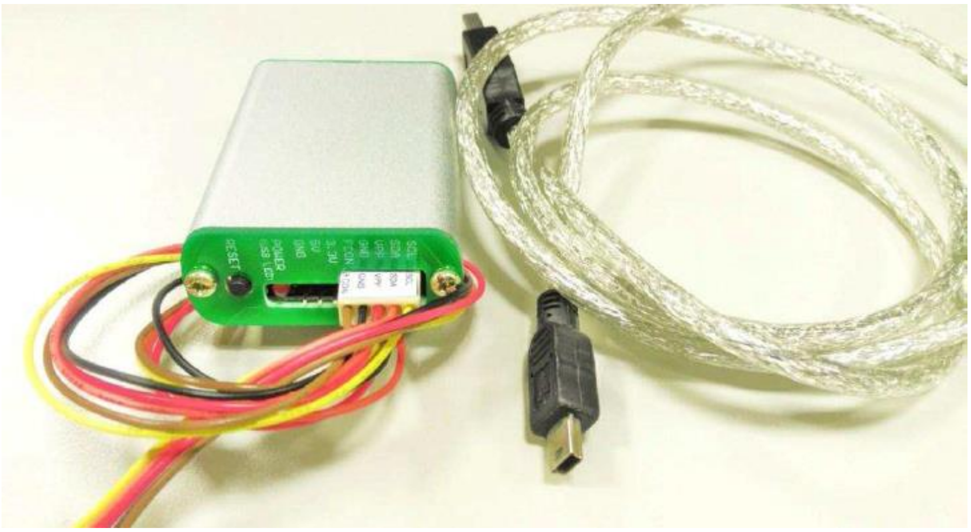
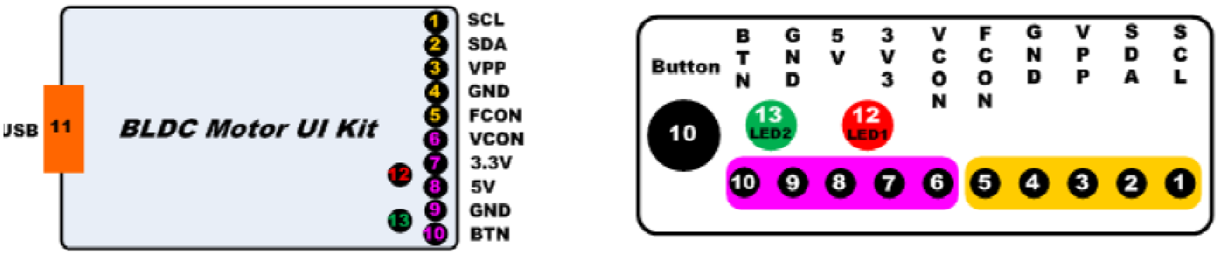


Figure 33 – PTC BLDC (USB-to-I2C) UI Kit.



Pin Name	Description	Pin No.
SCL	I2C serial frequency (internal pull-up resistor 4.7KΩ)	1
SDA	I2C serial data (internal pull-up resistor 4.7KΩ)	2
VPP	OTP recording voltage is 7.5V, Normal is 5V	3
GND	Ground	4
FCON	Connect to the “FG” pin on the motor control board	5
VCON	Calibrate VREG voltage output to +5V	6
3.3V	3.3V power supply	7
5V	5V power supply	8
GND	Ground	9
Button	Offline burn button (production use)	10
BTN	Offline burn button extension contact, external button	10
USB	USB port	11
LED1	Offline burning "Failed" The light is on red, the buzzer is one second long sound.	12
LED2	Offline burning " success" The light is on green, the buzzer sounds short.	13

Figure 34 – PTC BLDC UI Kit Pin Description.

The programming interface on the inverter connects to pin 1-to-5 respectively (SCL, SDA, VPP, GND and FCON) to achieve clock trimming, parameter write/read, motor instant control and display and one-time programming. Detailed instruction is provided in the application note.

8.3.2 PTC Graphical User Inteface (GUI)

Figure 35 depicts the overview of PTC GUI used together with the PTC BLDC (I2C to USB) kit for control parameter settings to suit different motor applications and performance optimization. PTC provides a detailed instruction how to use the GUI documented in the application note.

The parameter settings used in this design example is available and can be obtained from the applications engineering group.

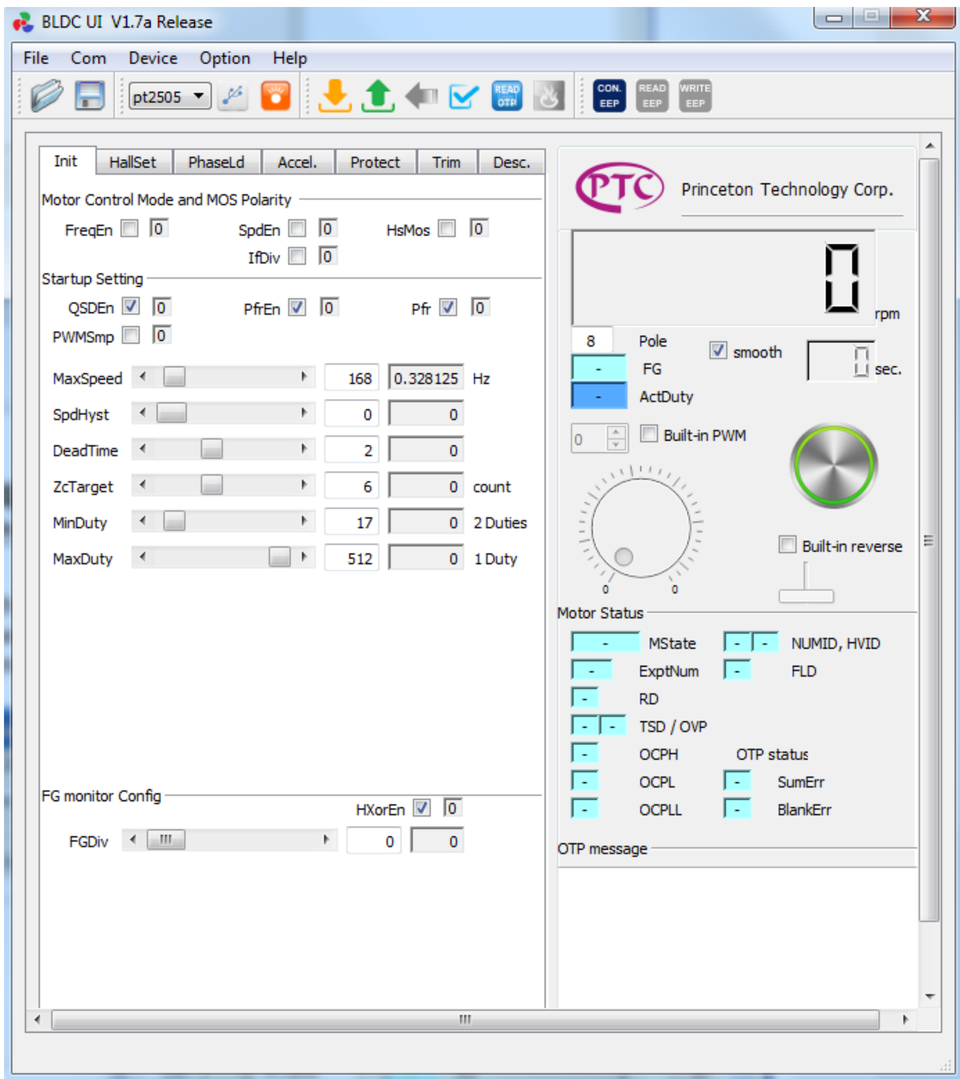


Figure 35 – PTC BLDC Graphical User Interface.

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8.4 *Inverter Output Power Measurement*

3-phase inverter output power P_{OUT} and efficiency measurements apply the “two wattmeter” method illustrated in Figure 36 below.

$$P_{OUT} = P_{CH1} + P_{CH2}$$

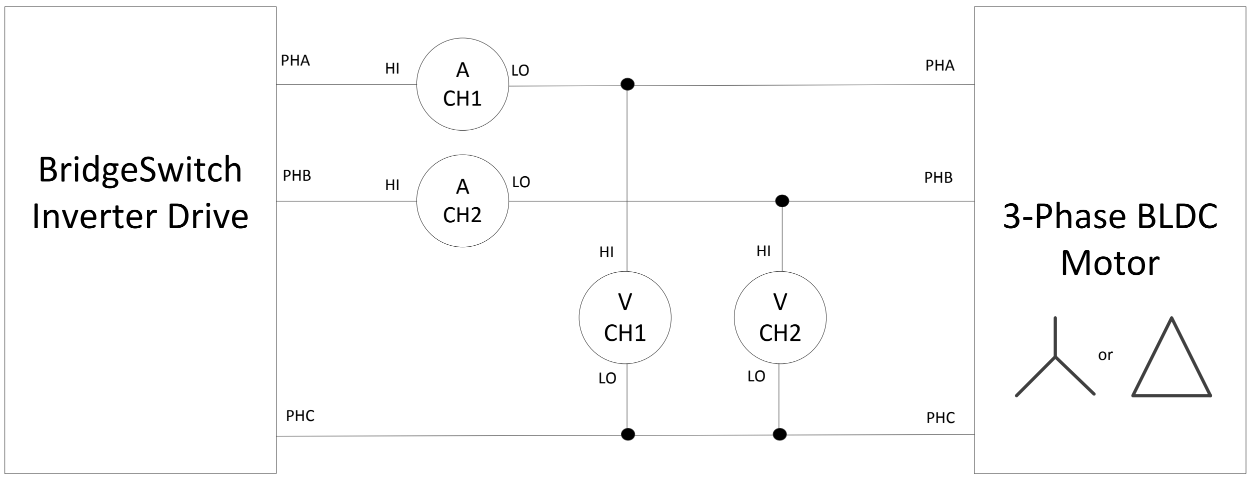

Figure 36 – Inverter Output Power Measurement.

9 Notes

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10 Revision History

Date	Author	Revision	Description & Changes	Reviewed
13-Nov-18	JHP	1.0	Initial Release.	Apps & Mktg
20-Dec-18	JHP	1.1	Updated Schematic Figure 2 and Text.	
09-Jan-19	JHP	1.2	Updated PCB Images.	

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