Application Note AN-109
LinkSwitch-XT2SR Family

Design Guide

Introduction

The LinkSwitch™-XT2SR family of devices are highly integrated off-line switcher ICs with a synchronous-rectifier driver and integrated 3.3 V LDO (uVCC) supply designed for non-isolated flyback converters capable to deliver power up to 12 W for universal input voltage or 15 W for high-line only input voltage. Using a synchronous rectification instead of diode rectification on the output winding greatly increases the conversion efficiency by up to 7 percentage points. The 3.3 V (uVCC) is intended for supplying power to an external microprocessor unit (MCU) without the need for external LDO, which simplifies the design. The LinkSwitch-XT2SR family comes with 725 V internal power MOSFET switch for universal input voltage range (i.e., 90 – 265 VAC) and 900 V rating for increased industrial input voltage ranges up to 440 VAC or extra safety margin. Both have excellent surge-withstand.

LinkSwitch-XT2SR controlled power supplies can easily achieve zero no-load power (<5 mW), worldwide standby power consumption requirements and global energy efficiency regulations.

Target applications are for appliance, home/business automation and industrials systems market not requiring (safety) isolation. Typically used as auxiliary supply with single output voltage of 5 V or 12 V output but also used for dual output voltage of 5 V and 12 V with an option of utilizing the integrated 3.3 V LDO (uVCC) to power peripheral circuits such as Wi-Fi or Bluetooth modules and MCUs with almost no impact on efficiency. Another unique feature of LinkSwitch-XT2SR is the need of no bias winding to supply the IC itself to achieve zero no-load requirement. The no-bias supply feature will allow simple two-winding transformer, which can be automatically built, a significant system cost saving. LinkSwitch-XT2SR ICs have options for internal FB, which enable to operate without feedback divider circuit for either single 5 V or 12 V output, and external FB for dual-output design, which requires shared output sensing for tighter regulation, and for output voltages other than 5 V or 12 V. (See Figures 1 and 2)

LinkSwitch-XT2SR ICs offer the internal protections and features without the need for designer intervention, which as follows 1) auto-restart, which limits device and circuit power dissipation during overload or output short-circuit, 2) hysteretic over-temperature protection (OTP), which disables switching during thermal faults, 3) output overvoltage protection (OVP) set at 120% of output voltage, and 4) frequency-jitter, which reduces EMI by modulating switching frequency.

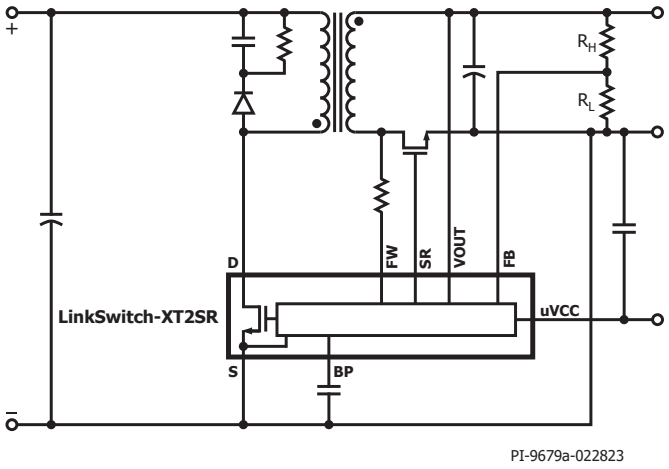

Figure 1. Example Schematic Showing LinkSwitch-XT2SR Single VOUT with Optional External FB.

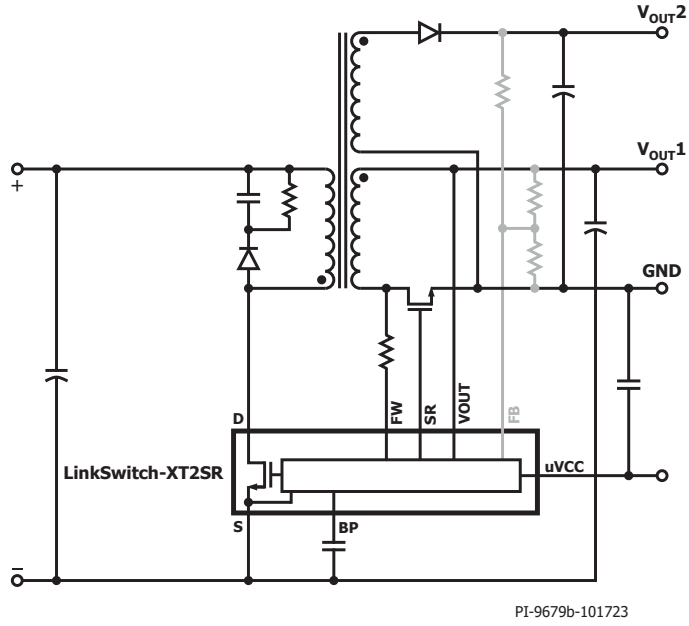

Figure 2. Example Schematic Showing LinkSwitch-XT2SR Dual VOUT with Optional External FB.
Note: For dual output design use diode rectifier for the higher voltage output.

Scope

This application note is intended to guide engineers through a step-by-step design process of designing non-isolated AC-DC flyback power supply using the LinkSwitch-XT2SR family of devices. The objective is to provide power supply engineers with guidelines to quickly select key components and complete a suitable transformer design and to enable them to quickly build an efficient flyback converter. This application note uses the Power Integrations PIXIs Designer tool for LinkSwitch-XT2SR devices. The PIXIs Designer is part of the PI Expert Suite™ of software tools developed to simplify the process of designing with Power Integrations' products. PIXIs is a spreadsheet-based tool that takes a user's specifications and calculates critical design parameters needed to complete a power supply design. (PIXIs is available at https://piexpertonline.power.com)

In addition to this application note, the reader may also find the LinkSwitch-XT2SR Reference Design Kit (RDK-962) containing an engineering prototype board, useful as an example of a complete and fully functional power supply. Further details can be found at www.power.com.

Typical Application Schematic

Figure 3 shows the typical application schematic for a non-isolated flyback converter using the LinkSwitch-XT2SR controller. Unless otherwise specified, references to components in this document shall refer to the designators shown in Figure 3. The schematic shown will apply to most applications.

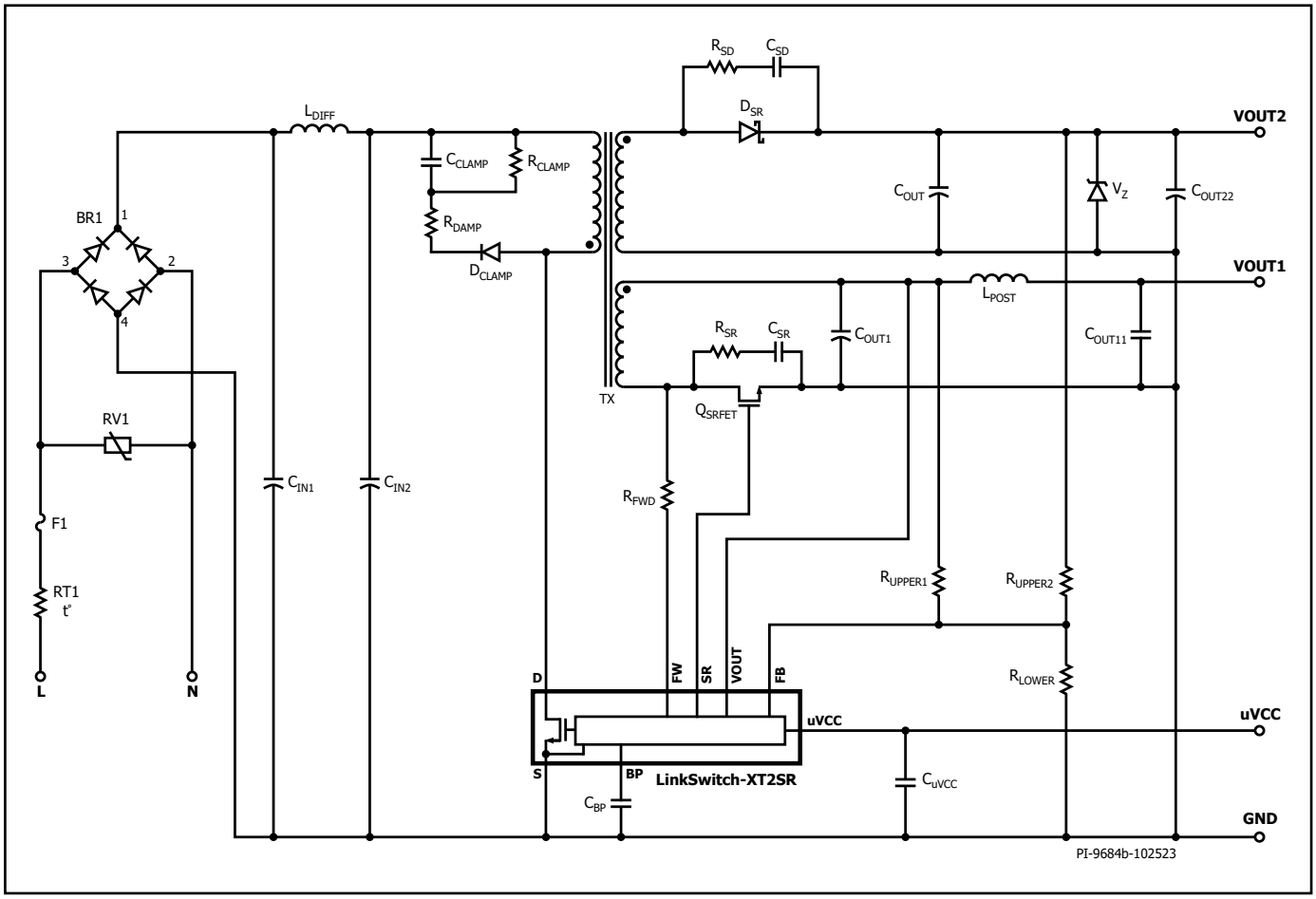

Figure 3. Typical Non-Isolated Dual Output Voltage Flyback Converter Using LinkSwitch-XT2SR IC.

PIXIs Design Details

When using the PIXIs tool, it is important to iterate the design until no more warnings are present. Warnings can be addressed by following the guidance given in the right most column of the spreadsheet. Once all warnings are cleared, use the magnetics designer tool to optimize the transformer and then generate the design documents that can be used to create a prototype transformer.

Open the appropriate PIXIs Designer spreadsheet for LinkSwitch-XT2SR from link https://www.power.com/piexpert/login

Step 1 – ENTER APPLICATION VARIABLES

VACMIN, VACMAX, fL, LINE RECTIFICATION TYPE, VOUT, IOUT, EFFICIENCY, CIN, VMIN, FEEDBACK, INPUT STAGE RESISTANCE

ACDC_LinkSwitchXT2SR_Flyback_081623; Rev.1.1; Copyright Power Integrations 2023	INPUT	INFO	OUTPUT	UNIT	ACDC LinkSwitch-XT2SR Flyback Design Spreadsheet
ENTER APPLICATION VARIABLES					
LINE VOLTAGE RANGE			UNIVERSAL		AC line voltage range
VACMIN			90.00	V	Minimum AC line voltage
VACMAX			265.00	V	Maximum AC line voltage
fL			60.00	Hz	AC mains frequency
LINE RECTIFICATION TYPE	F		F		Line rectification type: select "F" if full wave rectification or "H" if half wave rectification
VOUT			5.00	V	Output voltage
IOUT	2.400		2.400	A	Average output current
EFFICIENCY (User Estimate)			0.80		Overall efficiency estimate
LOSS ALLOCATION FACTOR			0.50		The ratio of power losses during the primary switch off-state to the total system losses
POUT			12.00	W	Continuous output power
CIN	30.00		30.00	uF	Input capacitor
VMIN			99.77	V	Valley voltage of the rectified minimum AC line voltage
VMAX			374.77	V	Peak voltage of the maximum AC line voltage
FEEDBACK	EXTERNAL		EXTERNAL		Feedback type: select either "INTERNAL" or "EXTERNAL"
INPUT STAGE RESISTANCE			10.0	Ohms	Input stage resistance (includes thermistor, filtering components, etc)
PLOSS_INPUTSTAGE			0.226	W	Maximum input stage power loss

Table 1. Application Variable Section of LinkSwitch-XT2SR Design Spreadsheet.

AC Line Voltage, VACMIN and VACMAX

Determine the input voltage range from Table 2. For Universal input voltage range use 90 VAC and 265 VAC for VACMIN and VACMAX, respectively.

Region	Nominal Input Voltage (VAC)	Minimum Input Voltage (VAC)	Maximum Input Voltage (VAC)	Nominal Line Frequency (Hz)
Japan	100	85	132	50 / 60
United States, Canada	120	90	132	60
Australia, China, European Union Countries, India, Korea, Malaysia, Russia	230	185	265	50
Indonesia, Thailand, Vietnam	115, 120, 127	90	155	50 / 60
	220, 230	185	265	50 / 60
	240	185	265	50

Table 2. Reference for Worldwide Input Line Voltage Ranges and Line Frequencies.

Line Frequency, f_L
Select 50 Hz for universal or single line 100 VAC, 60 Hz for single line 115 VAC input. 50 Hz for single 230 VAC input. These values represent typical line frequencies which most applications this gives adequate overall design margin. For absolute worst-case conditions, assume a line frequency tolerance of ±6%.

LINE RECTIFICATION TYPE
Select "F" if full wave rectification or "H" if half wave rectification.

Output Voltage, V_{OUT} (V)
Enter the nominal output voltage of the main output during the continuous load condition. Generally, the main output is the output from which feedback is derived.

Output Current, I_{OUT} (A)
Enter the output current from the power supply.

This should be the maximum output current. In multiple output designs the output power of the main output (typically the output from which feedback is taken) should be increased such that the maximum continuous output power from the main output matches the combined output power from all the outputs. The individual output voltages and currents should then be entered at the bottom of the spreadsheet.

Power Supply Efficiency, η
This is the complete power supply efficiency measured at the point of load, use a value of 0.8 for a 5.0 V output if no better data is available, or until measurements can be made on a prototype.

Power Supply Loss Allocation Factor
This factor represents the proportion of losses between the primary and the secondary of the power supply. If no better data is available, then the following values are recommended:

$$Z = \frac{\text{Secondary Losses}}{\text{Total Losses}}$$

- Typical Z value: 0.5

Total Input Capacitance, C_{IN} (μF)
Enter total input capacitance using Table 3 for guidance. The capacitance is used to calculate the minimum and maximum DC voltage across the bulk capacitor and should be selected to keep the minimum DC input voltage, V_{MIN} > 50 V, and ideally V_{MIN} > 70 V.

	Total Input Capacitance per Watt Output Power μF/W	
AC Input Voltage (VAC)	Full-Wave Rectification	Half-Wave Rectification
100/115	2-3	4-5
230	1-2	2-3
90 - 265	2-3	4-5

Table 3. Suggested Total Input Capacitance for Different Input Voltage Ranges.

VMIN
Valley voltage of the rectified minimum AC line voltage. The value of VMIN entered by the user will be used for all calculations, neglecting any effect from CIN.

FEEDBACK
Select INTERNAL if VOUT is either 5 V or 12 V, or select EXTERNAL if VOUT is other than 5 V or 12 V, or dual output that requires shared feedback for regulation.

INPUT STAGE RESISTANCE
Includes thermistor, filtering components, etc.

Step 2 – Enter LinkSwitch-XT2SR Variables

To select the correct LinkSwitch-XT2SR device, refer to the LinkSwitch-XT2SR data sheet power table and select based on the input voltage, enclosure type and output power of the design.

Maximum Output Power Table		
Product	**Open Frame[1,2]**	
725 V MOSFET	230 VAC	85 - 265 VAC
LNK3771D	7 W	6 W
LNK3772D	12 W	10 W
LNK3773D	15 W	12 W
900 V Switch	230 VAC	85 - 484 VAC
LNK3792D	12 W	10 W

Notes:
1. Minimum peak power capability.
2. Max output power is dependent on the design. Limit package temperature to <125 ºC.

Table 4. Output Power Table.

LINKSWITCH-XT2 VARIABLES					
DEVICE SERIES	LNK3773D		LNK3773D		Generic LinkSwitch-XT2SR device code
POUT_MAX			12	W	Power capability of the device based on thermal performance
ILIMITMIN			0.478	A	Minimum current limit of the device
ILIMITTYP			0.514	A	Typical current limit of the device
ILIMITMAX			0.550	A	Maximum current limit of the device
RDSON			6.85	Ohms	Switch on-state drain-to-source resistance at 100 degC
FSMIN			62000	Hz	Minimum switching frequency
FSTYP			66000	Hz	Typical switching frequency
FSMAX			70000	Hz	Maximum switching frequency
BVDSS			725	V	Device breakdown voltage

Table 5. LinkSwitch-XT2SR Variables Section of LinkSwitch-XT2SR Design Spreadsheet.

Reflected Output Voltage, VOR (V)
This parameter is the secondary winding voltage reflected back to the primary through the turns ratio of the transformer (during the conduction time of the output rectifier). The default value is 90 V, however this can be increased up to 150 V to achieve the maximum power capability from the selected LinkSwitch-XT2SR device. In general, start with the default value of 90 V, change the value when necessary to maintain K_P above its lower limit of 0.6.

LinkSwitch-XT2SR On-State DRAIN to SOURCE Voltage, V_{DSON} (V)
This parameter is the average on-state voltage developed across the DRAIN and SOURCE pins of LinkSwitch-XT2SR IC. By default, if the gray override cell is left empty, a value of 2 V is assumed. Use the default value if no better data is available

Calculated Ripple to Peak Current Ratio, K_P
Below a value of 1, indicating continuous conduction mode,

K_P is the ratio of ripple to peak primary current (K_{RP}). Above a value of 1, indicating discontinuous conduction mode, and K_P is the ratio of primary power MOSFET off-time to the secondary diode conduction time (K_{DP}). The value of K_P should be in the range of $0.6 < K_P < 6$, and guidance is given in the comments cell if the value is outside this range. A value above 1 will typically result in lower noise, discontinuous conduction mode at 115 VAC, where EMI measurements are made.

PRIMARY WAVEFORM PARAMETERS					
OPERATION MODE			CCM		Continuous mode of operation
VOR	92.0		92.0	V	Voltage reflected across the primary winding when the primary switch is off
VDSON			2.00	V	Primary switch on-time drain-to-source voltage
VDSOFF			536.8	V	Primary switch off-time drain-to-source voltage stress
KRP/KDP			0.676		Degree on how much the operation tend to be continuous or discontinuous
KP_TRANSIENT			0.312		KP value under transient conditions
DUTY			0.485		Maximum duty cycle
TIME_ON_MIN			2.731	us	Primary switch minimum on-time
IPEAK_PRIMARY			0.550	A	Maximum primary peak current
IPED_PRIMARY			0.155	A	Maximum primary pedestal current
IAVG_PRIMARY			0.153	A	Maximum primary average current
IRMS_PRIMARY			0.240	A	Maximum root-mean-squared value of the primary current
PLOSS_SWITCH			0.512	W	Maximum primary switch power loss
THERMAL RESISTANCE OF SWITCH			95	degC/W	Net thermal resistance of primary switch
T_RISE_SWITCH			48.6	degC	Maximum temperature rise of the switch in degrees Celsius
LPRIMARY_MIN			2130	uH	Minimum primary inductance
LPRIMARY_TYP			2366	uH	Typical primary inductance
LPRIMARY_MAX			2603	uH	Maximum primary inductance
LPRIMARY_TOL			10	%	Primary inductance tolerance
SECONDARY WAVEFORM PARAMETERS					
IPEAK_SECONDARY			10.010	A	Peak secondary current
IRMS_SECONDARY			4.494	A	Maximum root-mean-squared value of the secondary current
IRIPPLE_SECONDARY			10.010	A	Maximum ripple value of the secondary current
PIV_SECONDARY			25.5	V	Peak inverse voltage of the secondary rectifier
VF_SECONDARY	0.10		0.10	V	Forward voltage drop of the secondary rectifier

Table 6. Primary Waveform Parameter Section of LinkSwitch-XT2SR Design Spreadsheet.

SR FET On-State DRAIN to SOURCE Voltage, V_{DSON} (V)
Enter the average on-state voltage developed across the DRAIN and SOURCE pins of SR FET. Use 0.1 V for SR FET V_{DSON} (V.)

SECONDARY WAVEFORM PARAMETERS					
IPEAK_SECONDARY			10.010	A	Peak secondary current
IRMS_SECONDARY			4.494	A	Maximum root-mean-squared value of the secondary current
IRIPPLE_SECONDARY			10.010	A	Maximum ripple value of the secondary current
PIV_SECONDARY			25.5	V	Peak inverse voltage of the secondary rectifier
VF_SECONDARY	0.10		0.10	V	Forward voltage drop of the secondary rectifier

Table 7. Secondary Waveform Parameter section of LinkSwitch-XT2SR Design Spreadsheet.

Step 3 – Transformer Construction Parameters

Core Effective Cross-Sectional Area, Ae (mm^2)
Core Effective Path Length, Le (mm),
Core Ungapped Effective Inductance, AL ($nH/turns^2$)
Volume of the Core, Ve (mm^3)
Window area of the Bobbin, AW (mm)
Width of the Bobbin, BW (mm)
Mean Length per turn of the Bobbin, MLT (mm).

By default, if the Core Type cell is left empty, the spreadsheet will select the EE13 core. The user can change this selection and choose an alternate core from a list of commonly available cores suitable for the output power (see Table 8). Changes to these values will change the power capability of a given core size, therefore Table x should be used for guidance only. The gray override cells can be used to enter the core and bobbin parameters directly. This is useful if a core is selected that is not on the list or the specific core or bobbin information differs from that recalled by the spreadsheet.

Core Size	Suggested Power Range
EE8, EE10,EF10, EFD12, EP10, EPC13	<5 W
EE13, EE16, EFD15, EE19, EF12.6, EI16, EP13	<10 W
EE22, EFD20, RM5, EE25	<20 W
EFD25, RM6	<30 W

Table 8. Commonly Available Cores and Power Levels at Which Cores Can be used for Typical Designs

TRANSFORMER CONSTRUCTION PARAMETERS					
Core Selection					
CORE	CUSTOM		CUSTOM		Select the transformer core
CODE CODE	EFD25		EFD25		Core code
BOBBIN	EFD25-H		EFD25-H		Core code
AE	58.00		58.00	mm^2	Cross-sectional area of the core
LE	57.00		57.00	mm	Effective magnetic path length of the core
AL	2000.0		2000.0	nH/(T^2)	Ungapped effective inductance of the core
VE	3300.0		3300.0	mm^3	Effective volume of the core
AW	40.70		40.70	mm^2	Window area of the bobbin
BW	16.10		16.10	mm	Width of the bobbin
MLT	50.00		50.00	mm	Mean length per turn of the bobbin
MARGIN			0.00	mm	Safety margin

Table 9. Transformer Construction Parameter Section of LinkSwitch-XT2SR Design Spreadsheet.

The maximum operating flux density is a calculated parameter. A limit of 3000 Gauss is recommended for normal operation. This will also control the maximum flux density during start-up and output short-circuit, when the output voltage is low, and with little energy is available to reset the core. The lack of full reset will cause the transformer flux density to rise and staircase above normal levels. The value of 3000 Gauss at the peak current-limit of the selected device, together with the built-in protection features of LinkSwitch-XT2SR, provides sufficient margin to prevent core saturation under start-up or output short-circuit conditions. The cycle skipping operating mode used in LinkSwitch-XT2SR IC can generate audible frequency components in the transformer. Following the peak flux density guideline above and using the standard transformer production technique of dip varnishing, practically eliminates audible noise. A careful evaluation of the audible noise performance should be made using production transformer samples before approving the design. Ceramic capacitors that use dielectrics, such as Z5U, may also generate audible noise when used in clamp circuits. If this is the case, replace with capacitors that have a different dielectric material, (e.g., polyester film) to help reduce noise.

Primary Turns_NPrimary
in general, it should be the lowest number that meets the primary current density limit (CMA) of 200 Cmils/Amp.

ALG (nH/T^2) - Gapped Core Effective Inductance
BAC (Gauss) - AC Flux Density for Core Loss Curves (0.5 x Peak to Peak)
AWG - Primary Wire Gauge (Rounded to next smaller standard AWG value)
OD PRIMARY INSULATED (mm) - Primary winding wire outer diameter with insulation
CMA PRIMARY (mils^2/Amp) - Primary Winding Current Capacity.

Primary Winding					
NPRIMARY			91	turns	Primary winding number of turns
BMAX			2712	Gauss	Actual value of magnetic flux density (BMAX_TARGET = 3000 Gauss)
BAC			1356	Gauss	AC flux density
ALG			286	nH/(T^2)	Gapped core effective inductance
LG			0.219	mm	Core gap length

Table 10. Primary Winding Section of LinkSwitch-XT2SR Design Spreadsheet.

Winding Construction
- Primary
  - AWG = 30
  - OD = 0.3 mm
  - CMA = 417.52 Cmils/A

Secondary Turns, N
AWG – Secondary wire gauge (rounded to next smaller standard AWG value)
OD Secondary INSULATED (mm) - Secondary winding wire outer diameter with insulation
CMA Secondary (mils^2/Amp) - Secondary winding current capacity.

Secondary Winding					
NSECONDARY	5		5	turns	Secondary winding number of turns

Table 11. Secondary Winding Section of LinkSwitch-XT2SR Design Spreadsheet.

Winding Construction
- Secondary
  - AWG = 24
  - OD = 0.57 mm
  - CMA = 308.8 Cmils/A

Step 4 – Iterate Transformer Design and Generate Transformer Design Output

Iterate the design making sure that no warnings are displayed. Any parameters outside the recommended range of values can be corrected by following the guidance given in the right-hand column.

Once all warnings have been cleared, the output transformer design parameters can be used to either wind a prototype transformer or send to a vendor for samples. This is the target nominal primary inductance of the transformer.

Primary Inductance Tolerance, $L_{PRIMARY\_TOL}$ (%)
This is the assumed primary inductance tolerance. A value of ±10% is used by default, however if specific information is known from the transformer vendor, then this may be overridden by entering a new value in the gray override cell.

Step 5 – Selection of Primary Clamp resistors, Diode, and capacitor

R2CD Clamp Configurations
R2CD is for applications where the lowest cost and EMI are most important. This is the most commonly used clamp circuit in low power supply applications. Figure 4 shows the circuit using R2CD clamp. In R2CD clamp circuit of Figure 4, the clamp diode, D_{CLAMP} must be a standard recovery glass-passivated type or a fast recovery diode with a reverse recovery time of ≤2 µs. The use of standard recovery glass passivated diodes allows recovery of some of the clamp energy in each switching cycle and helps improve average efficiency. The diode conducts momentarily each time the power MOSFET inside LinkSwitch-XT2SR turns off and energy from the leakage inductance is transferred to the clamp capacitor C_{CLAMP}. Resistor R_{DAMP}, which is in the series path, offers damping preventing excessive ringing due to resonance between the leakage inductance and the MOSFET switch output capacitance C_{OSS}. Damping the ringing reduces the EMI, and R_{DAMP} typical value is in the range of 22 Ω to 500 Ω. Resistor R_{CLAMP} bleeds-off energy stored inside the capacitor C_{CLAMP}. Power supplies using different LinkSwitch-XT2SR devices in the family will have different peak primary current, leakage inductances and therefore leakage energy. Capacitor C_{CLAMP}, and resistors R_{CLAMP} and R_{DAMP} must therefore be optimized for each design. As a general rule it is advisable to minimize the value of capacitor C_{CLAMP} and maximize the value of resistors R_{CLAMP} and R_{DAMP}, while still meeting BV_{DSS} limit at highest input voltage and full load. The value of R_{DAMP} should be high enough to damp the ringing in the required time but must not be so large as to cause the drain voltage to exceed 80% to 90% of BV_{DSS} (depending on derating requirements). Note that The BV_{DSS} of LinkSwitch-XT2SR devices is at 725 V. A ceramic capacitor that uses a dielectric such as Z5U when used in clamp circuit for C_{CLAMP} may generate audible noise, so a polyester film type or a ceramic capacitor with X7R as a dielectric, 1 kV rating, 1206 size are commonly used. Recommended for clamp diode D_{CLAMP} is a S1M, and the reverse recovery time of the diode is around 2 µs.

Key Design Points Primary Clamp Circuit Optimization

- Minimize leakage inductance, completely fill each winding layer of the transformer.
- Following the assumption of leakage inductance or LLK to be less than 3% of primary inductance (LP) is a good starting point for the calculation of primary clamp parameters, but the best practice is to measure the leakage inductance of the transformer sample.
- Optimize the value of snubber resistor in the R2CD clamp to further reduce power losses meeting the following conditions:

1. The EMI performance is not compromised.
2. Enough drain voltage margin for the internal MOSFET (BV_{DSS}), typically set in the range of 80% to 90% of B_{VDSS} under worst-case conditions (maximum input voltage, maximum overload power or output short-circuit).

- Minimize clamp losses by optimizing the reflected voltage (V_{OR}) value.
- Minimizing inter-winding capacitance by following proper layout and transformer construction such as maintaining a tightly coupled loop between the primary snubber and windings and putting layers of tape between each primary winding.

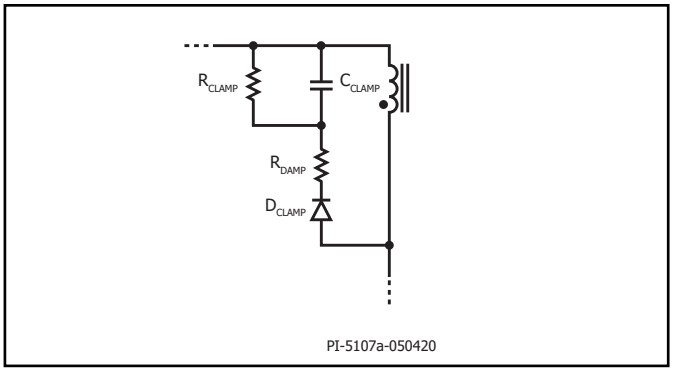

Figure 4. R2CD Clamp Circuit.

- Resistor R_{DAMP} must be large enough to prevent excessive ringing due to inductance between the leakage inductance and the MOSFET switch output capacitance C_{OSS}. If there is excessive ringing occurred in the FWD pin waveform due to insufficient R_{DAMP}, there will be short SR gate drive pulse occurred as shown in Figure 5.

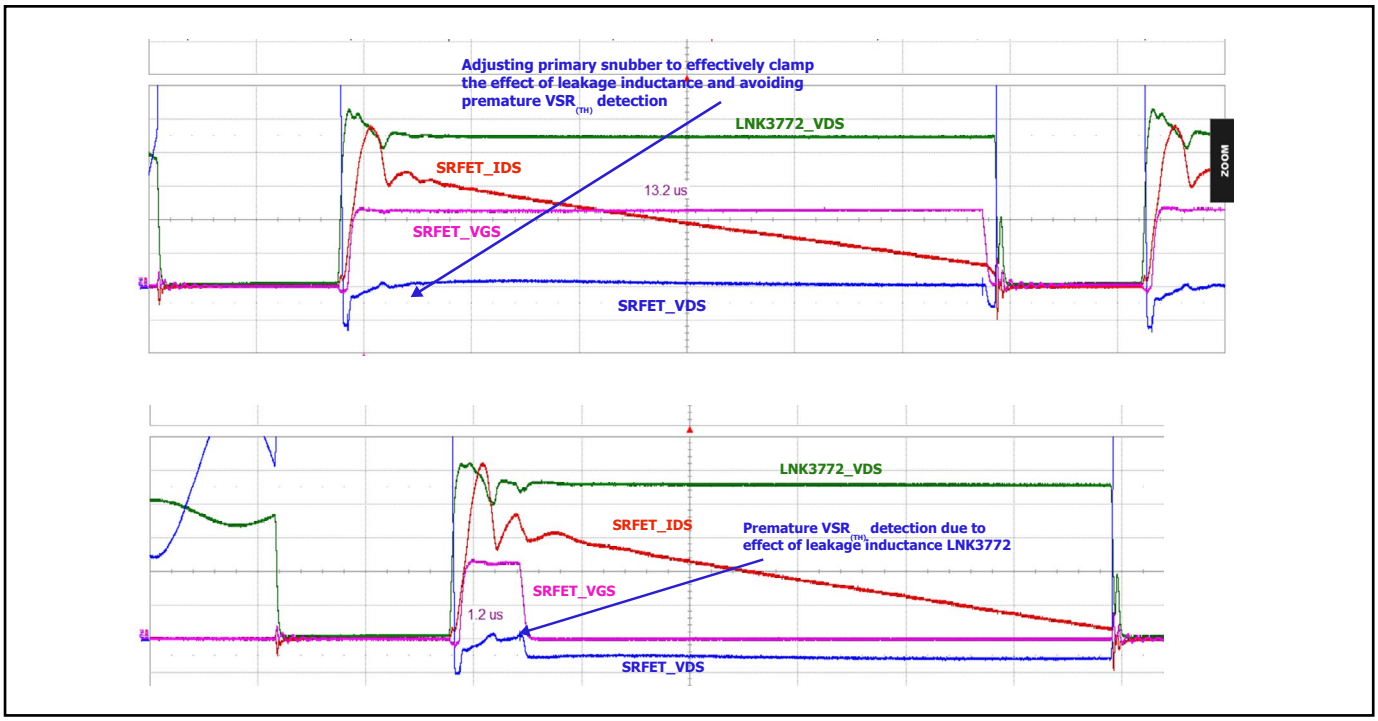

Figure 5. SR Gate Waveforms Depending on R_{DAMP} Values (Sufficient R_{DAMP} – Top Graph, Insufficient R_{DAMP} – Bottom Graph).

Step 6 – Multiple Output Parameters

This section allows the user to select up to two secondary outputs and will help in the selection of secondary rectifier, MOSFET or diode, for each output. The spreadsheet will also provide a warning if the combined output power exceeds the value in the POUT. For single output design, VOUT1, IOUT1 and POUT1 will be the main output parameters entered in Step 1. Table 12 displays the multiple output parameters shown in the spreadsheet.

The Spreadsheet also calculates the critical electrical parameters for each secondary output: Number of turns for output, NS

- It is necessary to use power MOSFET as a main output rectifier type and use a diode as a 2nd output rectifier type. The main output should provide higher output power than the other output. The SR pin should not be shorted to SOURCE pin in any case.
- Secondary turns are calculated for each output. NS1 is for the main output which is equivalent to calculated or desired secondary number turns.
- RMS current of the secondary output, ISRMS (A)
- Used to determine the size of the winding wire for each secondary and determine the ripple current at the output capacitor.
- Current Ripple on the Secondary, ISRIPPLE (A)
- This parameter will help the designer select the appropriate output filter capacitor for each output.

Secondary Rectifier Maximum Peak Inverse Voltage, PIVS (V)

- This parameter, provided for each output will help the user select the appropriate voltage rating for each rectifier. Additional information for the magnetic wire are also given:
  Secondary Winding Conductor Bare Diameter CMS (Cmils)
  Secondary Wire Gauge AWGS (AWG)
  Minimum Secondary Bare Conductor Diameter DIAS (mm)
  Maximum Secondary Outside diameter ODS (mm)

For each output, use the values of peak inverse voltage (PIVS) and output current (IOUT) provided in the design spreadsheet to select the output rectifier voltage rating (VR's).

VR ≥ 1.25 × PIVS: where PIVS is taken from the Voltage Stress Parameters section of the spreadsheet and Transformer Secondary Design Parameters (Multiple Outputs).

ID ≥ 3 × IOUT: where ID is the output rectifier rated DC current, and IOUT is the average output current.

Depending on the temperature rise and the duration of the peak load condition, it may be necessary to increase the current rating once a prototype has been built. This also applies to the amount of heat sinking necessary. Additionally, Table 13 lists some of the suitable MOSFETs for SR FET may be used with LinkSwitch-XT2SR circuits. The LinkSwitch-XT2SR spreadsheet also recommends a MOSFET and a diode based on the above guidelines.

MULTIPLE OUTPUT PARAMETERS					
Output 1 (SRFET)					
VOUT1			5.00	V	Output voltage 1
IOUT1	1.400		1.400	A	Output current 1
POUT1			7.00	W	Output power 1
VD1	0.10		0.10	V	Forward voltage drop of SRFET for output 1
NS1			5	turns	Number of turns for output 1
ISPEAK1			10.01	A	Instantaneous peak value of the secondary current for output 1
ISRMS1			2.621	A	Root-mean-squared value of the secondary current for output 1
ISRIPPLE1			10.010	A	Current ripple on the secondary current waveform for output 1
PIV1			31.9	V	Computed peak inverse voltage stress on the secondary SRFET for output 1
OUTPUT_RECTIFIER1	AO4264		AO4264		Selected SRFET for output 1
VRRM1			60	V	Maximum repetitive peak reverse voltage of the SRFET for output 1
TRR1			15	ns	Reverse recovery time of the SRFET for output 1
IFM1			12.00	A	Maximum forward continuous current of the SRFET of output 1
PLOSS_SRFET1			0.512	W	Maximum SRFET power loss for output 1
VOUT1_RIPPLE			50	mV	Output voltage ripple for output 1
ESR_COUT1			5	mOhms	Equivalent series resistance of the output capacitor for output 1
IRMS_COUT1			2.216	A	Root-mean-squared value of the output capacitor current for output 1
PLOSS_COUT1			0.025	W	Maximum output capacitor power loss for output 1
Output 2 (Diode)					
VOUT2	12.00		12.00	V	Output voltage 2
IOUT2	0.420		0.420	A	Output current 2
POUT2			5.04	W	Output power 2
VD2	0.20		0.20	V	Forward voltage drop of diode for output 2
NS2			12	turns	Number of turns for output 2
ISPEAK2			4.171	A	Instantaneous peak value of the secondary current for output 2
ISRMS2			0.786	A	Root-mean-squared value of the secondary current for output 2
ISRIPPLE2			4.171	A	Current ripple on the secondary current waveform for output 2
PIV2_CALCULATED			83.8	V	Computed peak inverse voltage stress on the diode for output 2
OUTPUT_RECTIFIER2	STPS2H100AY		STPS2H100AY		Selected diode for output 2
PIV2_RATING			100	V	Peak inverse voltage rating on the diode for output 2
TRR2			0	ns	Reverse recovery time of the diode for output 2
IFM2			2.00	A	Maximum forward continuous current of the diode for output 2
PLOSS_DIODE2			0.064	W	Maximum diode power loss for output 2
VOUT2_RIPPLE			120	mV	Output voltage ripple for output 2
ESR_COUT2			29	mOhms	Equivalent series resistance of the output capacitor for output 2
IRMS_COUT2			0.665	A	Root-mean-squared value of the output capacitor current for output 2
PLOSS_COUT2			0.013	W	Maximum output capacitor power loss for output 2
POUT_TOTAL		Warning	12.04	W	The total power of all outputs exceeds the design power. Increase the design power in the first section of the spreadsheet
NEGATIVE OUTPUT					If a negative output exists, select the output number (e.g. if VO2 is a negative output, select 2)

Table 12. Multiple Output Parameter Section of LinkSwitch-XT2SR Design Spreadsheet.

PART	PIV	I_{DRAIN}	$V_{GS(TH)}$	$V_{GS(TH)}$	C_{ISS}	C_{RSS}	C_{RSS}/C_{ISS}	R_G	$R_{DS(ON)}$	T_{RR}	Package	Manufacturer
			MAX	MIN								
	(Volts)	(Amperes)	(Volts)	(Volts)	(pF)	(pF)		(Ω)	(mΩ)	(ns)		
AO4260	60	18.0	2.4	1.3	4940	32.0	0.65%	0.9	6.3	22	8-SOIC (0.154", 3.90 mm Width)	Alpha and Omega
AO4264	60	12.0	2.5	1.4	2007	12.5	0.62%	1.2	13.5	15	8-SOIC (0.154", 3.90 mm Width)	Alpha and Omega
AON6244	60	85.0	2.5	1.5	3838	14.5	0.38%	1.0	6.2	17	8-PowerSMD, Flat Leads	Alpha and Omega
AON6266	60	30.0	2.5	1.5	1340	10.0	0.75%	1.5	19.0	17	8-PowerSMD, Flat Leads	Alpha and Omega
AON7246	60	34.5	2.5	1.5	1340	10.0	0.75%	1.5	19.0	16	8-PowerVDFN	Alpha and Omega
AO4294	100	11.5	2.4	1.4	2420	11.0	0.45%	0.6	15.5	25	8-SOIC (0.154", 3.90 mm Width)	Alpha and Omega
AON7292	100	23.0	2.6	1.6	1170	8.0	0.68%	0.7	32.0	24	8-WDFN Exposed Pad	Alpha and Omega
AO4292	100	8	2.7	1.6	1190	7	0.59%	3	33	20	SOIC-8	Alpha and Omega
AO4294	100	11.5	2.4	1.4	2420	11	0.45%	3	15.5	25	SOIC-8	Alpha and Omega
AO4296	100	13.5	2.3	1.3	3130	12.5	0.40%	3	10.6	28	SOIC-8	Alpha and Omega
AOD294A	100	55	2.5	1.5	2305	11.5	0.50%	3	15.5	30	TO-252	Alpha and Omega
AOD296A	100	70	2.3	1.3	3130	12.5	0.40%	3	10.6	30	TO-252	Alpha and Omega
AOD2910	100	31	2.7	1.6	1190	7	0.59%	3	33	30	TO-252	Alpha and Omega
AOD2916	100	25	2.7	1.6	870	3.5	0.40%	3	43.5	20	TO-252	Alpha and Omega
AOD2544	150	23.0	2.7	1.7	675	4.0	0.59%	2.9	66.0	37	TO-252 DPAK	Alpha and Omega
AON7254	150	17.0	2.7	1.7	675	4.0	0.59%	2.9	66.0	37	8-WDFN Exposed Pad	Alpha and Omega

Table 13. List of Logic Level MOSFETs Suitable for SR FETs with LinkSwitch-XT2SR Circuits.

Step 7 – Selection of Output Capacitors

Ripple Current Rating
Select the output capacitor(s) such that the ripple rating is greater than the calculated value, ISRIPPLE from the spreadsheet.

Many capacitor manufacturers provide factors that increased the allowable ripple current as the capacitor temperature is reduced or the frequency of the ripple is increased from the data sheet specified values. This should be considered to ensure the capacitor is not oversized, increasing the cost. Two or more capacitors may be used in parallel to give a combined ripple current rating equal to the sum of the individual capacitor ratings.

ESR Specification
Select a low ESR type, which gives acceptable output switching ripple. The switching ripple voltage is equal to the peak secondary current multiplied by the ESR of the output capacitor. Generally the selection the capacitor for ripple current rating will also result in an acceptable ESR.

Voltage Rating
Select a voltage rating such that VRATED ≥ 1.25 × V_O.

Step 8 – Choose Feedback Scheme and Select Feedback Components

FEEDBACK PARAMETERS

FEEDBACK PARAMETERS					
VFBRATIO			0.80		Output voltage feedback priority ratio. Eg. Ratio of 0.8 implies that VOUT1 has an 80% feedback priority.
RUPPER1			46400	Ohms	FB pin upper resistor connected to VOUT1
RUPPER2			619000	Ohms	FB pin upper resistor connected to VOUT2
RLOWER	24900		24900	Ohms	FB pin (Lower) Resistor

Table 14. Feedback Parameter section of LinkSwitch-XT2SR Design Spreadsheet.

Built in Output Voltage Feedback Circuit
The FB pin voltage is 2.0 V, and FB pin should be shorted to ground when using internal built-in divider used for single output voltage.

For external feedback, resistors R_H and R_L, can be selected as follows;

$$V_{OUT} = \frac{V_{FB} \times (R_H + R_L)}{R_L}, \text{ where } V_{FB} = 2.0 \text{ V}$$

Let R_H = 130 kΩ, R_L = 86.6 kΩ, Then V_{OUT} = 5 V.

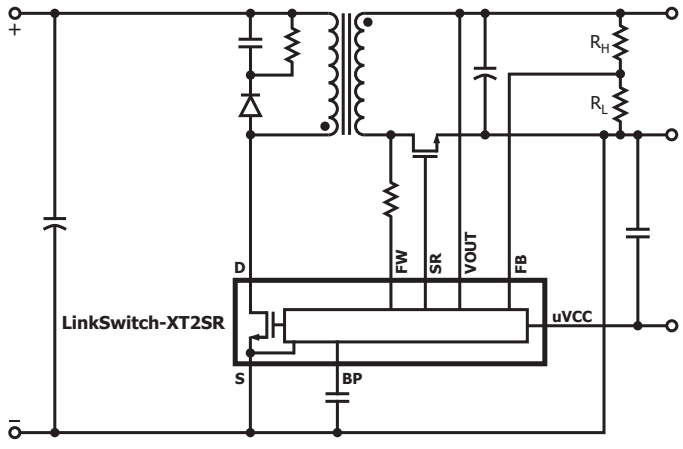

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Figure 6. External Feedback Configuration.

Key Application Considerations

LinkSwitch-XT2SR Design Considerations Output Power Table

The data sheet maximum output power table (Table 4) represents the maximum practical continuous output power level that can be obtained under the following assumed conditions:

1. The minimum DC input voltage is 90 V or higher for 85 VAC input, or 240 V or higher for 230 VAC input or 115 VAC with a voltage doubler. The value of the input capacitance should be large enough to meet these criteria for AC input designs.
2. Assumed efficiency of 80%.
3. Voltage only output
4. A primary clamp (R2CD) is used.
5. The part is board mounted with SOURCE pins soldered to a sufficient area of copper to keep the SOURCE pin temperature at or below 100 °C.
6. Ambient temperature of 50 °C for open frame designs and an internal enclosure temperature of 60 °C for adapter designs.

LinkSwitch-XT2SR Design Considerations for Zero (<5 mW) No-Load Input Power Design

1. Select input capacitor.
   a. Select input capacitor with minimum leakage current for minimize the no load input power.
   b. Do not oversize the input capacitor than necessary. Oversized input capacitor would increase no-load input power.
2. Optimize primary and secondary snubber.
   a. R2CD snubber must be optimized to minimize the dissipation without compromising EMI performance.
   b. The maximum drain voltage voltages of primary FET and SR FET need to be within 80% to 90% of the rated breakdown voltage.
3. Optimize transformer construction.
   a. Minimize leakage inductance
      - Minimize the number of turns
      - Reduce number of layers
      - Minimize the insulation of windings
      - Keep tight coupling between windings
   b. Minimize winding capacitance
      - Z-winding reduces winding capacitance
      - Sectional winding reduces winding capacitance

ON/OFF Operation with Current Limit State Machine

The internal clock of the LinkSwitch-XT2SR IC runs all the time. At the beginning of each cycle, it determines the appropriate current limit (Figure 7 illustrates the ON/OFF control operation). At high loads, the state machine sets the current limit to its highest value. At lighter loads, the state machine sets the current limit to reduced values. MOSFET current ramps to a fixed limit every enabled switching cycle. The switching cycles are disabled to maintain the regulation. The effective switching frequency is proportional to the load. This makes the efficiency virtually constant over the entire load range, even in standby mode. And the multi-level MOSFET current limit practically eliminates audible noise. The response time of the ON/OFF control scheme is very fast, that it provides tight regulation and excellent transient response, without the needs of loop compensation.

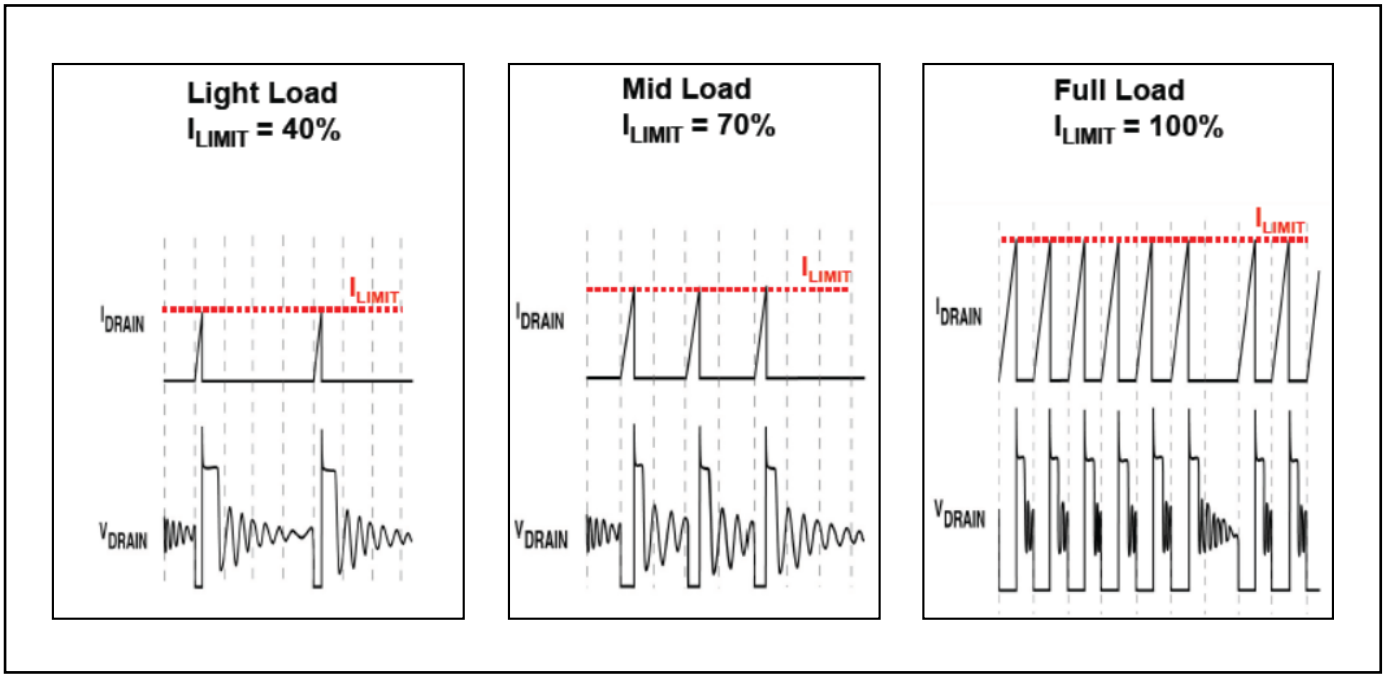


Figure 7. ON/OFF Control Operation.

LinkSwitch-XT2SR Layout Considerations

See Figures 9 and 11 for a recommended circuit board layout, for LinkSwitch-XT2SR devices.

Single Point Grounding
Use a single point ground connection from the input filter capacitor to the area of copper connected to the SOURCE pins.

Bypass Capacitor CBP
The BYPASS pin capacitor should be located as near as possible to the BYPASS and SOURCE pins.

Primary Loop Area
The area of the primary loop that connects the input filter capacitor, transformer primary and LinkSwitch-XT2SR IC together should be kept as small as possible.

Primary Clamp Circuit
A clamp is used to limit peak voltage on the DRAIN pin at turn-off. This can be achieved by using an R2CD clamp. In all cases, to minimize EMI, care should be taken to minimize the circuit path from the clamp components to the transformer and LinkSwitch-XT2SR IC.

Thermal Considerations
The copper area underneath the LinkSwitch-XT2SR IC acts not only as a single point ground, but also as a heat sink. As this area is connected to the quiet source node, it should be maximized for good heat sinking of LinkSwitch-XT2SR IC. The same applies to the source of SR FET.

Feedback Signal
Keep the high current, high-voltage drain and clamp traces away from the feedback signal to prevent noise pick up.

Output Rectifier
For best performance, the area of the loop connecting the secondary winding, SR FET, and the output filter capacitor should be minimized. In addition, sufficient copper area should be provided at the source of the SR FET for heat sinking.

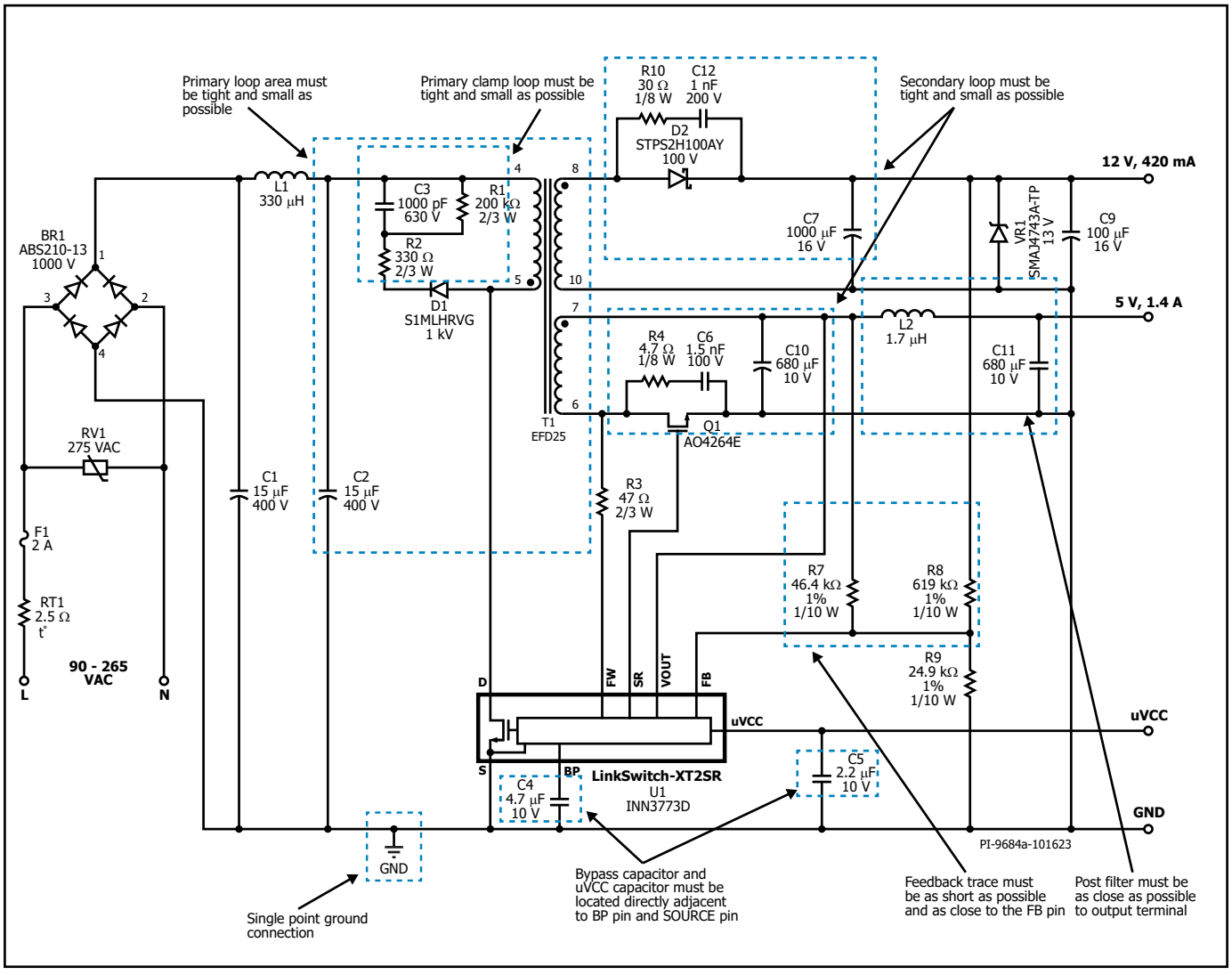
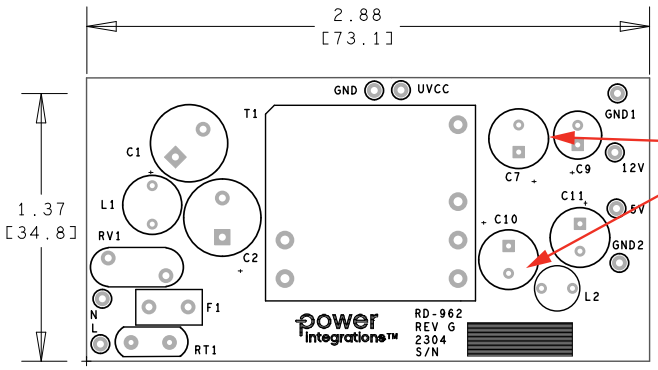


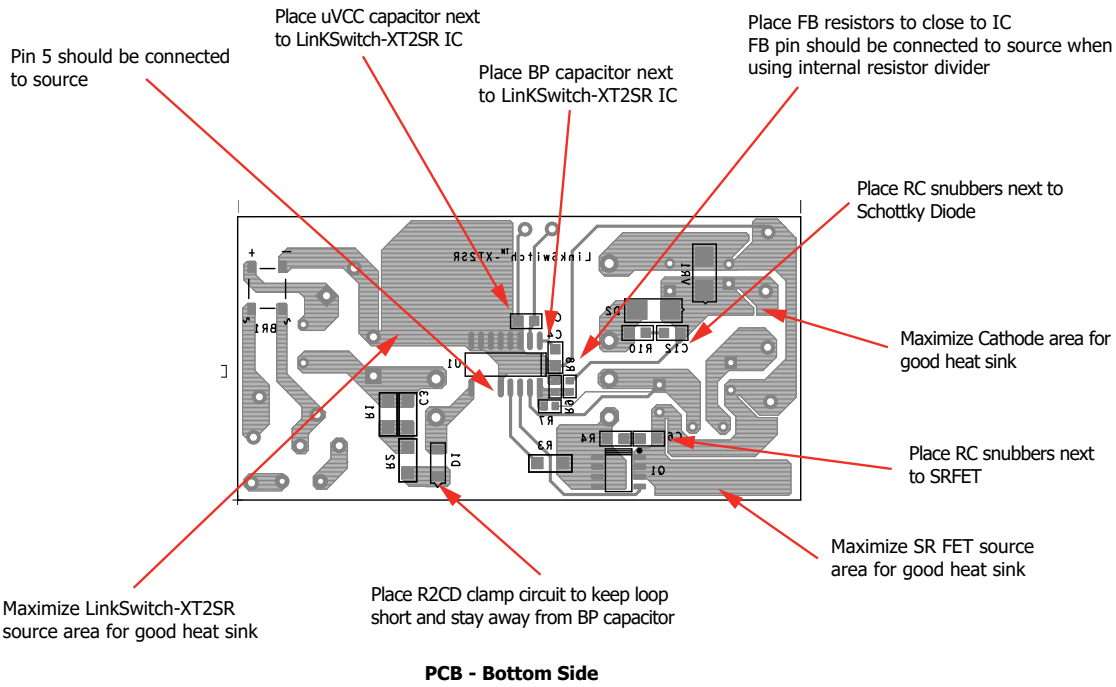
Figure 8. Typical Schematic of LinkSwitch-XT2SR Showing Critical Loops Area and Critical Component Placements.

Layout Example



Place output capacitors close to SR FET source and transformer pin to have small switching loop

PCB - Top Side



PCB - Bottom Side

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Figure 9. Recommended Printed Circuit Layout for LinkSwitch-XT2SR in a Flyback Converter Configuration.

Quick Design Checklist

As with any power supply design, all LinkSwitch-XT2SR designs should be verified on the bench to make sure that component specifications are not exceeded under worst-case conditions. The following minimum set of tests is strongly recommended:

1. Maximum Drain Voltage – Verify that V_{DS} does not exceed 90% of BV_{DSS} at the highest input voltage and peak (overload) output power. The 10% margin versus BV_{DSS} specification gives margin for design variation.

2. Maximum Drain Current – At maximum ambient temperature, maximum input voltage and peak output (overload) power, verify drain current waveforms for any signs of transformer saturation and excessive leading edge current spikes at start-up. Repeat under steady state conditions and verify that the leading-edge current spike event is below $I_{LIMIT(MIN)}$ at the end of the $t_{LEB(MIN)}$. Under all conditions, the maximum drain current should be below the specified absolute maximum ratings.

3. Thermal Check – At specified maximum output power, minimum input voltage and maximum ambient temperature, verify that the temperature specifications are not exceeded for LinkSwitch-XT2SR IC, transformer, output diode and output capacitors. Enough thermal margin should be allowed for part-to-part variation of the $R_{DS(ON)}$ of LinkSwitch-XT2SR IC as specified in the data sheet. Under low-line, maximum power, a maximum LinkSwitch-XT2SR IC SOURCE pin temperature of 100 °C is recommended to allow for these variations.

Design Tools

Up-to-date information on design tools can be found at the Power Integrations website: www.power.com

Appendix A – Application Example, DER-998

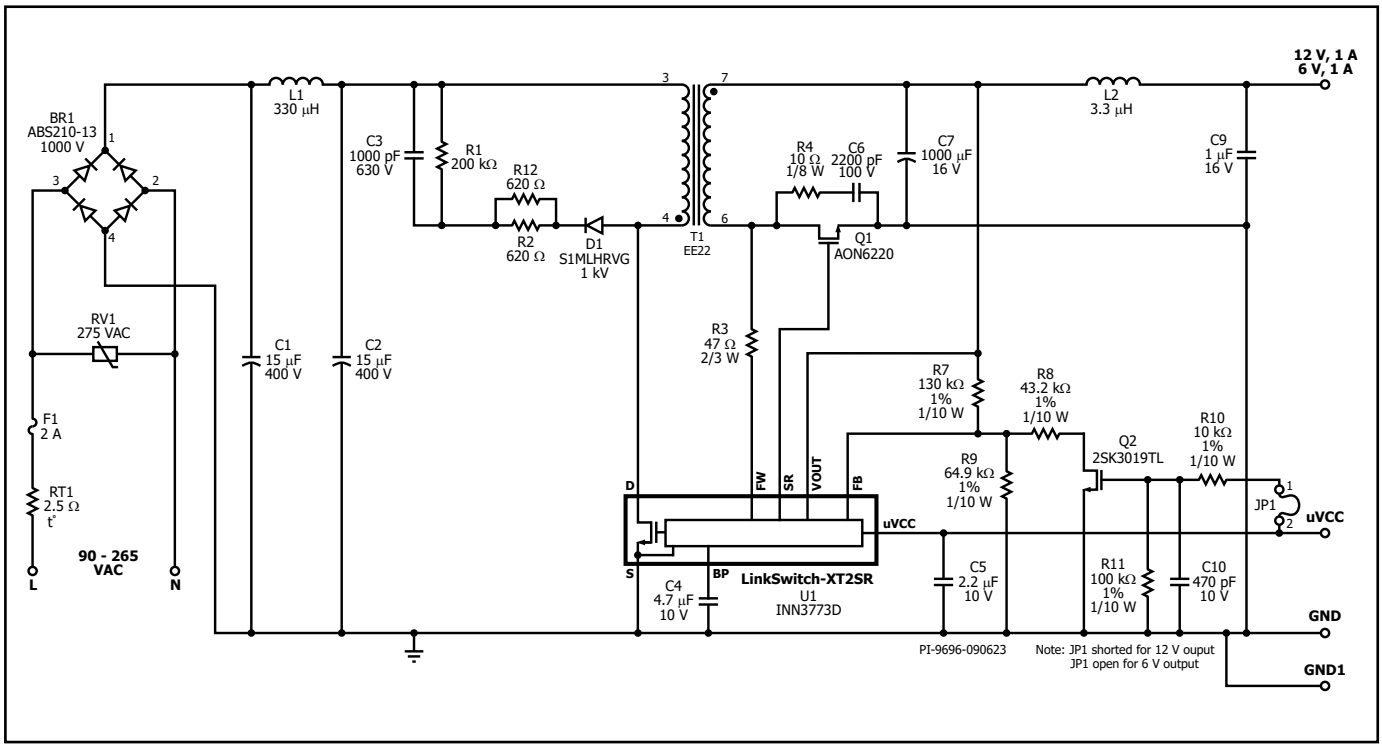

Figure 10. Schematic Diagram of a Selective Single Output Voltage, 6 V or 12 V, 1 A Output.

A Variable Selective Output Voltage 6 V / 12 V, 1 A (12 W) Design

The schematic shown in Figure 10 is a typical implementation of a non-isolated universal input, selective output voltage 6 V or 12 V ±5%, 1 A, power supply using LNK3773D. This circuit makes use of zero no-load input power and external feedback circuit with logic level FET to be able to select the output voltage. By selecting 6 V during standby, it would minimize the power loss during standby period. The EcoSmart features built into the LinkSwitch-XT2SR family allow this design to easily meet all current and proposed energy efficiency standards, including the mandatory California Energy Commission (CEC) requirement for average operating efficiency.

The AC input is rectified by bridge rectifier BR1 and filtered by the bulk storage capacitors C1 and C2. Resistor RF1 is a flameproof, fusible, wire wound type and functions as a fuse, inrush current limiter and, together with the filter formed by C1, C2, and L1, differential mode noise attenuator. This simple input stage, together with the frequency jittering of LinkSwitch-XT2SR ICs, allows the design to meet both conducted EMI limits with ≥10 dBV margin. The rectified and filtered input voltage is applied to the primary winding of T1. The other side of the primary is driven by the integrated power MOSFET in U1. R2CD clamp circuit with R1, R2, R12,C3, and D1, is used to provide adequate clamping of the leakage inductance drain voltage spike. The secondary of the flyback transformer T1 is rectified by Q1 SR FET, and filtered by C7, low ESR capacitor. The output voltage is sensed via resistor divider R7, R8, R9 and Q2. Output voltage is regulated so as to achieve a voltage of 2 V on the FEEDBACK pin. When logic low signal on Q2 gate with open JP1 jumper, the voltage divider network of R7 and R9 determines the output voltage to be 6 V. When logic high signal on Q2 gate applied with JP1 jumper, the effective resistance of R8 and R9 in parallel will be a part of voltage divider network with R7, and it will determine the output voltage to be 12 V. The LinkSwitch-XT2SR ICs is completely self-powered from the DRAIN pin, requiring only a small ceramic capacitor C4 connected to the BYPASS pin.

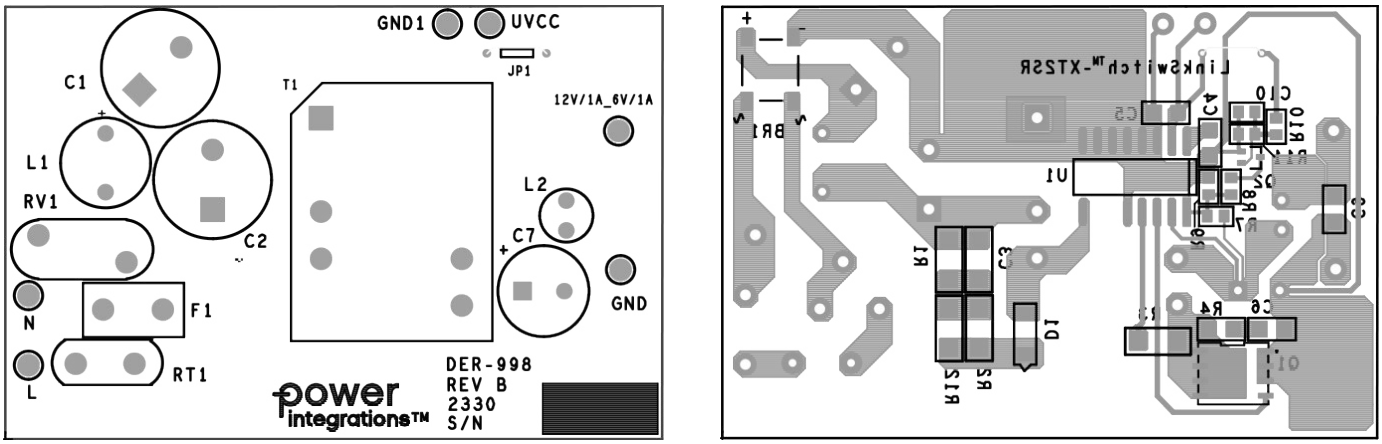

Figure 11. Layout of DER-998. (Left) Top Side and (Right) Bottom Side.

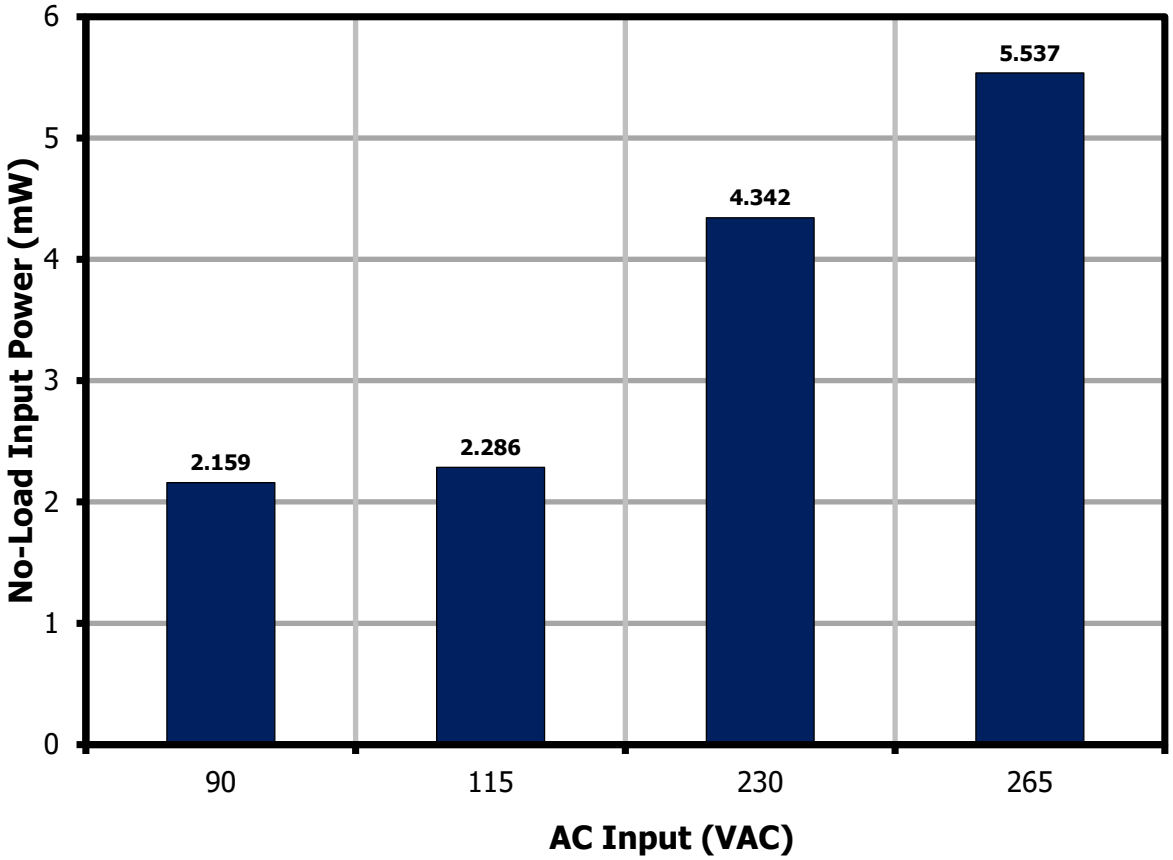

Figure 12. No-Load Input Power at 6 V Output.

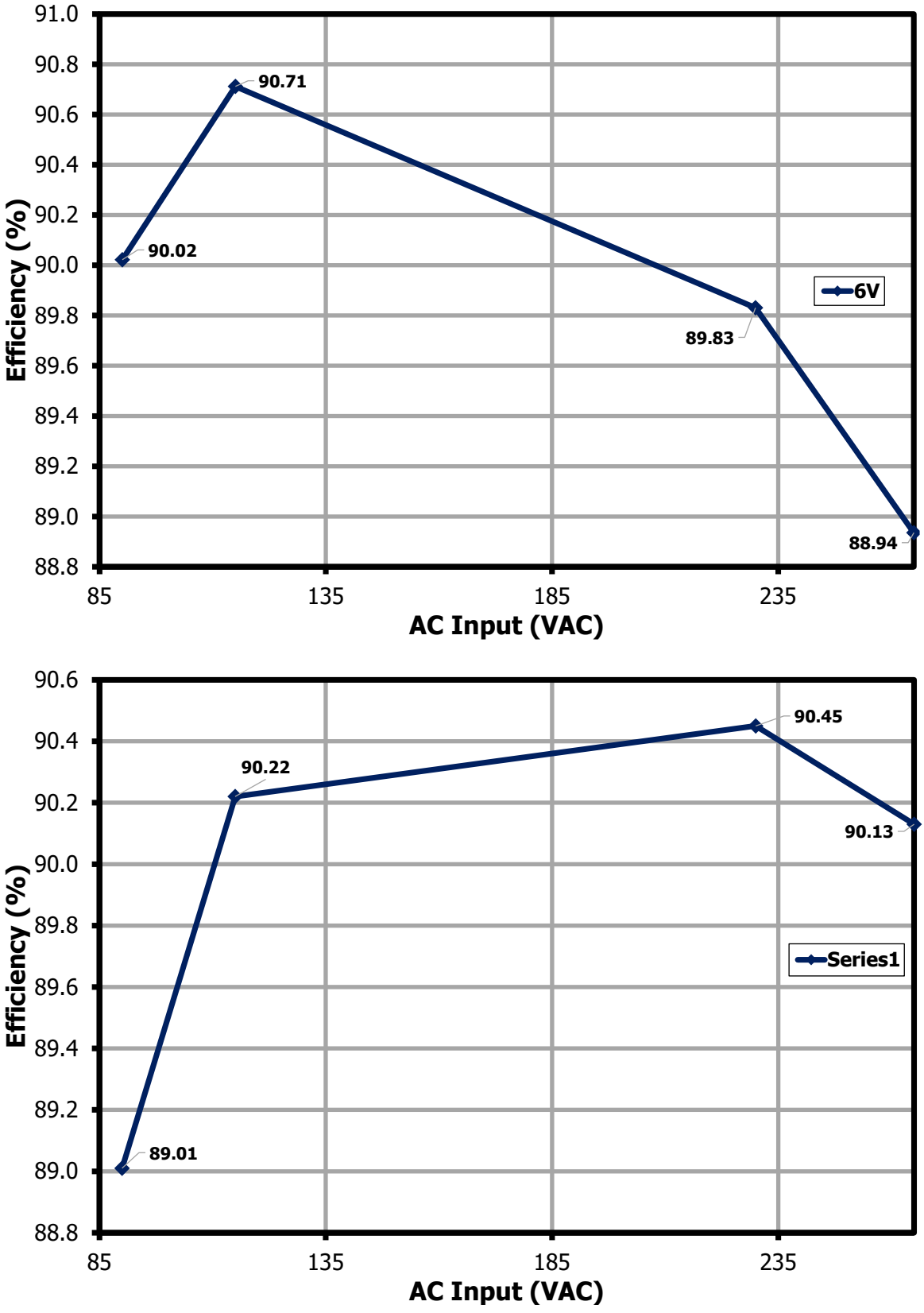

Figure 13. Full Load Efficiency at 6 V (Top) Output and 12 V (Bottom) Output.

Output Voltage Regulation

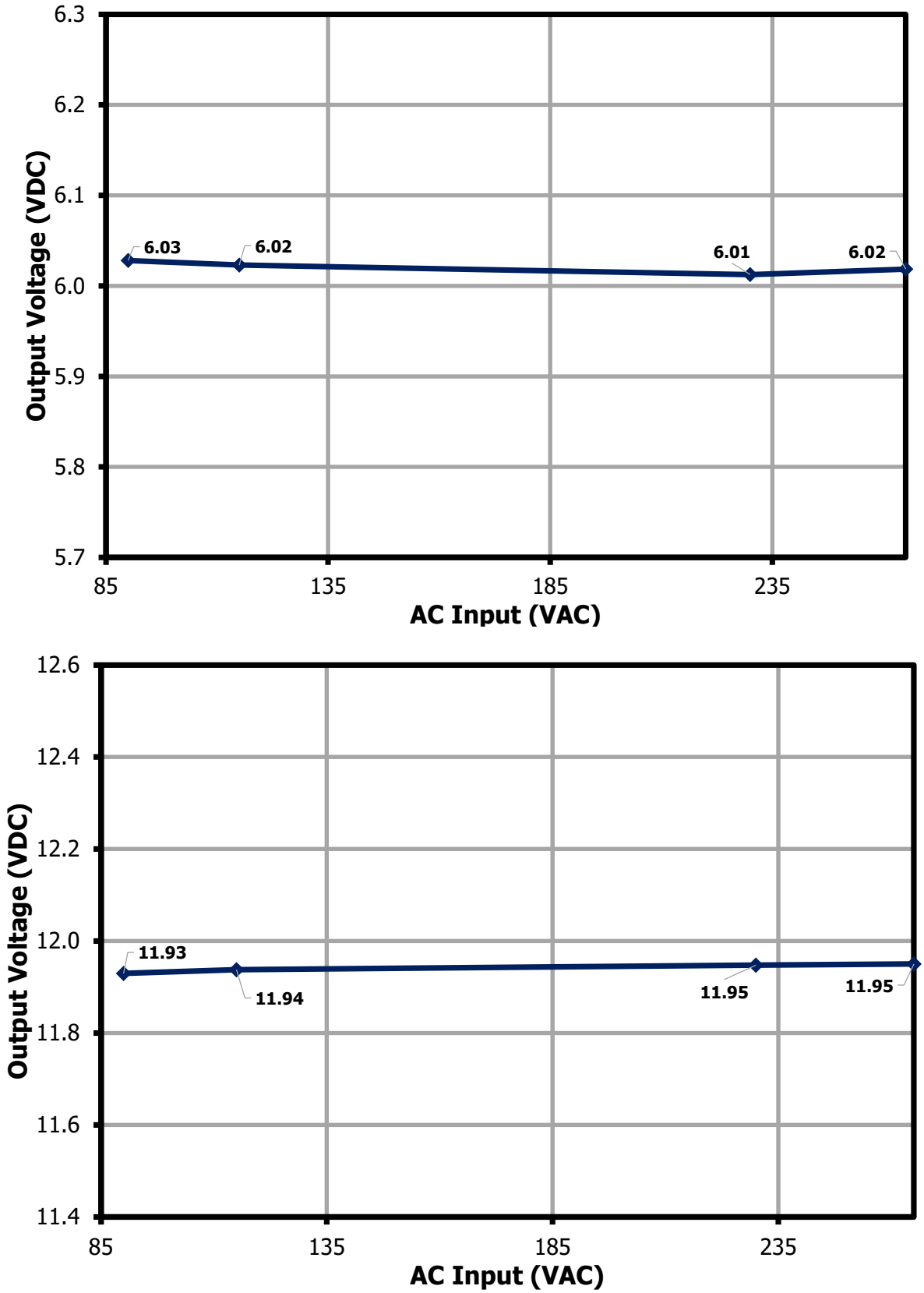

Figure 14. Output Voltage Regulation at 6 V (Top) Output and 12 V (Bottom) Output.

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Revision	Notes	Date
A	Initial release.	11/23

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