

Design Example Report

Title	<i>45 W USB PD 3.0 Power Supply with 3.3 V – 11 V / 5 A (45 W Power-limited) PPS Output Using InnoSwitch™ 3-PD PowiGaN™ INN3879C-H803</i>
Specification	90 VAC – 265 VAC Input; 5 V / 5 A, 9 V / 5 A, 15 V / 3 A, 20 V / 2.25 A, 3.3 V – 11 V / 5 A PPS (45 W Power-limited), 3.3 V – 16 V / 3 A PPS, or 3.3 V – 21 V / 2.25 A PPS Outputs
Application	USB PD / PPS Power Adapter
Author	Applications Engineering Department
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Summary and Features

- InnoSwitch3-PD: Off-Line CV/CC QR Flyback Switcher IC with Integrated USB Type-C and USB-PD Controller, Integrated High-Voltage Switch, Synchronous Rectification and FluxLink Feedback™
 - Integrated USB Type-C and USB-PD Controller reduces footprint, no external controller required
 - Comprehensive protection features with telemetry for power supply status and fault monitoring
- Meets DOE6 and CoC v5 2016 Average Efficiency requirements with high margin (>2.5%)
 - 5 V Output: 91.01% at 115 VAC (6.02% margin); 90.55% at 230 VAC (5.56% margin)
 - 9 V Output: 91.75% at 115 VAC (2.90% margin); 92.05% at 230 VAC (3.20% margin)
 - 15 V Output: 92.03% at 115 VAC (3.18% margin); 92.27% at 230 VAC (3.42% margin)
 - 20 V Output: 91.55% at 115 VAC (2.70% margin); 91.80% at 230 VAC (2.95% margin)
- <20 mW no-load input power at 230 VAC
- Meets CISPR22 / EN55022 Class B Conducted EMI with high margin
 - >7dB margin at worst case condition (20 V / 2.25 A, 230 VAC)
- Low component count, high power density
 - Total part count: 54
 - Power density: 14.0 W / inch³ without enclosure (1.89" x 1.81" x 0.94" form factor)

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PATENT INFORMATION

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Important Note:

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.



1 Introduction

This document is an engineering report describing a 45 W USB PD 3.0 power supply using InnoSwitch3-PD INN3879C-H803, which features an integrated USB PD controller within the IC. The USB PD source capabilities of the power supply are listed below.

- PDO1: 5 V / 5 A (Fixed Supply)
- PDO2: 9 V / 5 A (Fixed Supply)
- PDO3: 15 V / 3 A (Fixed Supply)
- PDO4: 20 V / 2.25 A (Fixed Supply)
- PDO5: 3.3 V – 11 V / 5 A (Programmable Power Supply, 45 W power-limited)
- PDO6: 3.3 V – 16 V / 3 A (Programmable Power Supply)
- PDO7: 3.3 V – 21 V / 2.25 A (Programmable Power Supply)

This design shows the high power density and efficiency that is possible due to the high level of integration of the InnoSwitch3-PD controller providing exceptional performance.

The report contains the power supply specification, schematic diagram, printed circuit board layout, bill of materials, magnetics specifications, and performance data.

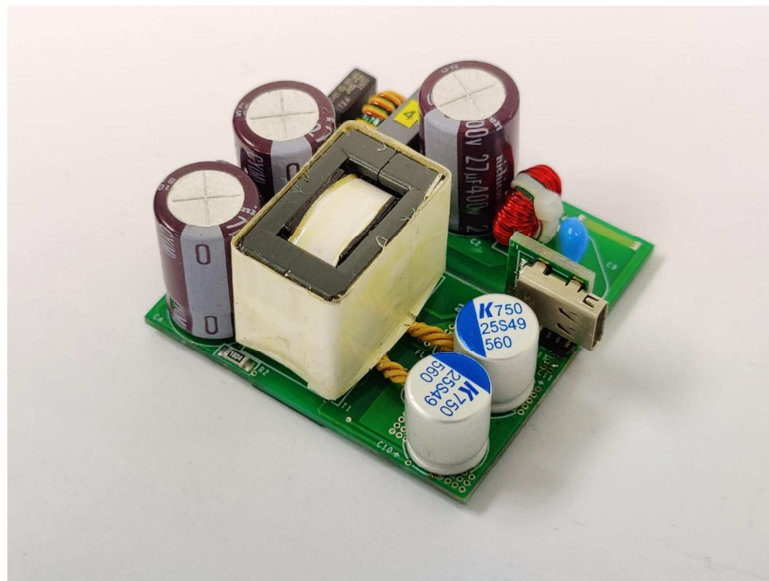


Figure 1 – Populated Circuit Board Photograph, Entire Assembly.

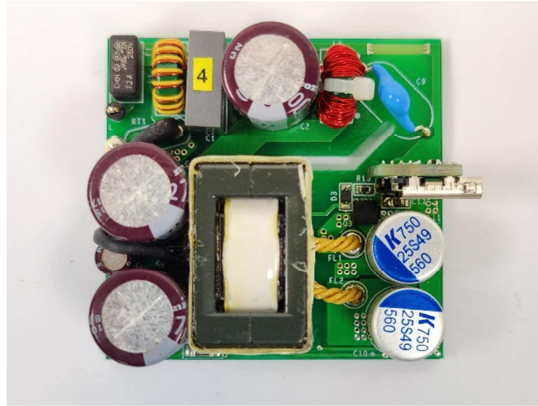
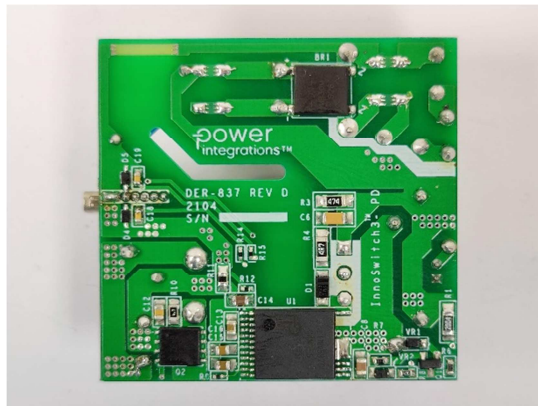


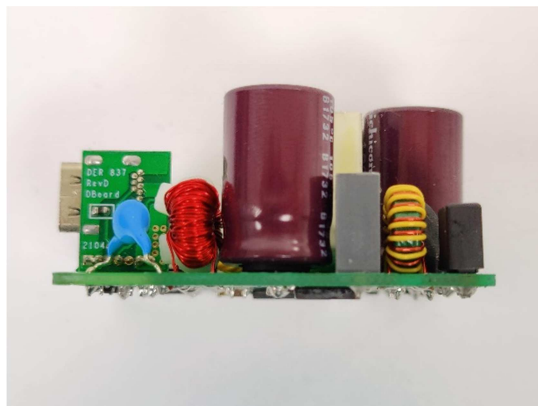
Figure 2 – Populated Circuit Board Photograph - Top.



48.0 mm board length

46.0 mm board width

Figure 3 – Populated Circuit Board Photograph - Bottom.



23.8 mm assembly height

Figure 4 – Populated Circuit Board Photograph - Side.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Input Voltage	V_{IN}	90		265	VAC	2 Wire – no P.E.
Input Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power				20	mW	Measured at 230 VAC
USB PD 3.0 Output: Fixed Supply PDOs						
5 V / 5 A						
Fixed Supply PDO1						
Output Voltage	$V_{OUT(5V)}$		5.0		V	See Note A.
Output Voltage Ripple	$V_{RIPPLE(5V)}$			150	mV	Measured at End of 100 mΩ Cable. See Note B.
Output Current	$I_{OUT(5V)}$			5.0	A	See Note C.
Average Efficiency	$\eta(5V)$	90.5			%	Average Efficiency at 115 VAC with VOUT Measured on the Board.
Continuous Output Power	$P_{OUT(5V)}$			25	W	
9 V / 5 A						
Fixed Supply PDO2						
Output Voltage	$V_{OUT(9V)}$		9.0		V	See Note A.
Output Voltage Ripple	$V_{RIPPLE(9V)}$			150	mV	Measured at End of 100 mΩ Cable. See Note B.
Output Current	$I_{OUT(9V)}$			5.0	A	See Note C.
Average Efficiency	$\eta(9V)$	91.2			%	Average Efficiency at 115 VAC with VOUT Measured on the Board.
Continuous Output Power	$P_{OUT(9V)}$			45	W	
15 V / 3 A						
Fixed Supply PDO3						
Output Voltage	$V_{OUT(15V)}$		15.0		V	See Note A.
Output Voltage Ripple	$V_{RIPPLE(15V)}$			150	mV	Measured at End of 100 mΩ Cable. See Note B.
Output Current	$I_{OUT(15V)}$			3.0	A	See Note C.
Average Efficiency	$\eta(15V)$	91.5			%	Average Efficiency at 115 VAC with VOUT Measured on the Board.
Continuous Output Power	$P_{OUT(15V)}$			45	W	
20 V / 2.25 A						
Fixed Supply PDO4						
Output Voltage	$V_{OUT(20V)}$		20.0		V	See Note A.
Output Voltage Ripple	$V_{RIPPLE(20V)}$			175	mV	Measured at End of 100 mΩ Cable. See Note B.
Output Current	$I_{OUT(20V)}$			2.25	A	See Note C.
Average Efficiency	$\eta(20V)$	91.0			%	Average Efficiency at 115 VAC with VOUT Measured on the Board.
Continuous Output Power	$P_{OUT(20V)}$			45	W	

Description	Symbol	Min	Typ	Max	Units	Comment
USB PD 3.0 Output: Programmable Power Supply APDOs						
3.3 V – 11 V / 5 A PPS APDO5						
Programmable Output Voltage Range	$V_{OUT(PDO5)}$	3.3		11	V	APDO Minimum and Maximum Voltage. See Note A.
Programmable Output Current Limit Range	$I_{OUT(PDO5)}$	1.0		5.0	A	See Note D.
PPS Voltage Step	$V_{STEP(PDO5)}$		20		mV	PPS Voltage Step (USB PD 3.0).
PPS Current Step	$I_{STEP(PDO5)}$		50		mA	PPS Current Step (USB PD 3.0).
Continuous Output Power	$P_{OUT(PDO5)}$			45	W	PPS Power Limited bit = 1 (USB PD 3.0). See Note E.
3.3 V – 16 V / 3 A PPS APDO6						
Programmable Output Voltage Range	$V_{OUT(PDO6)}$	3.3		16	V	APDO Minimum and Maximum Voltage. See Note A.
Programmable Output Current Limit Range	$I_{OUT(PDO6)}$	1.0		3.0	A	See Note D.
PPS Voltage Step	$V_{STEP(PDO6)}$		20		mV	PPS Voltage Step (USB PD 3.0).
PPS Current Step	$I_{STEP(PDO6)}$		50		mA	PPS Current Step (USB PD 3.0).
Continuous Output Power	$P_{OUT(PDO6)}$			48	W	PPS Power Limited bit = 0 (USB PD 3.0).
3.3 V – 21 V / 2.25 A PPS APDO7						
Programmable Output Voltage Range	$V_{OUT(PDO7)}$	3.3		21	V	APDO Minimum and Maximum Voltage. See Note A.
Programmable Output Current Limit Range	$I_{OUT(PDO7)}$	1.0		2.25	A	See Note D.
PPS Voltage Step	$V_{STEP(PDO7)}$		20		mV	PPS Voltage Step (USB PD 3.0).
PPS Current Limit Step	$I_{STEP(PDO7)}$		50		mA	PPS Current Step (USB PD 3.0).
Continuous Output Power	$P_{OUT(PDO7)}$			47.25	W	PPS Power Limited bit = 0 (USB PD 3.0).
Conducted EMI Margin		6			dB	Meets CISPR22B / EN55022B
Ambient Temperature	T_{AMB}	0		45	°C	Open Frame, Sea Level.

Note A: Output Voltage Regulation compliant with USB PD 3.0 Specifications.

B: Output Voltage Ripple measured at the end of 100 mΩ cable with the probe having decoupling capacitors 47 uF electrolytic and 100 nF ceramic in parallel.

C: Maximum Operating Current for the Fixed Supply PDO. Output Over Current Protection Threshold nominally set at 250 mA above the Operating Current requested by the USB PD Sink.

D: Output Current Limit Accuracy is within ±150 mA for Operating Current between 1 A and 3 A, or ±5% for Operating Current > 3 A; compliant with USB PD 3.0 Specifications.

E: For PPS APDOs with Power Limited bit set to 1, whenever the USB PD Sink sends a valid Output Voltage and Current Limit request that exceeds 45 W, the power supply will provide the requested output voltage and an output current limit that matches 45 W maximum output power.

Note: To use this design for a charger/adaptor with a different shape and form factor, the changes in the circuit board layout must be carefully evaluated to meet the target specifications for EMI, ESD, and Line Surge performance.



3 Schematic

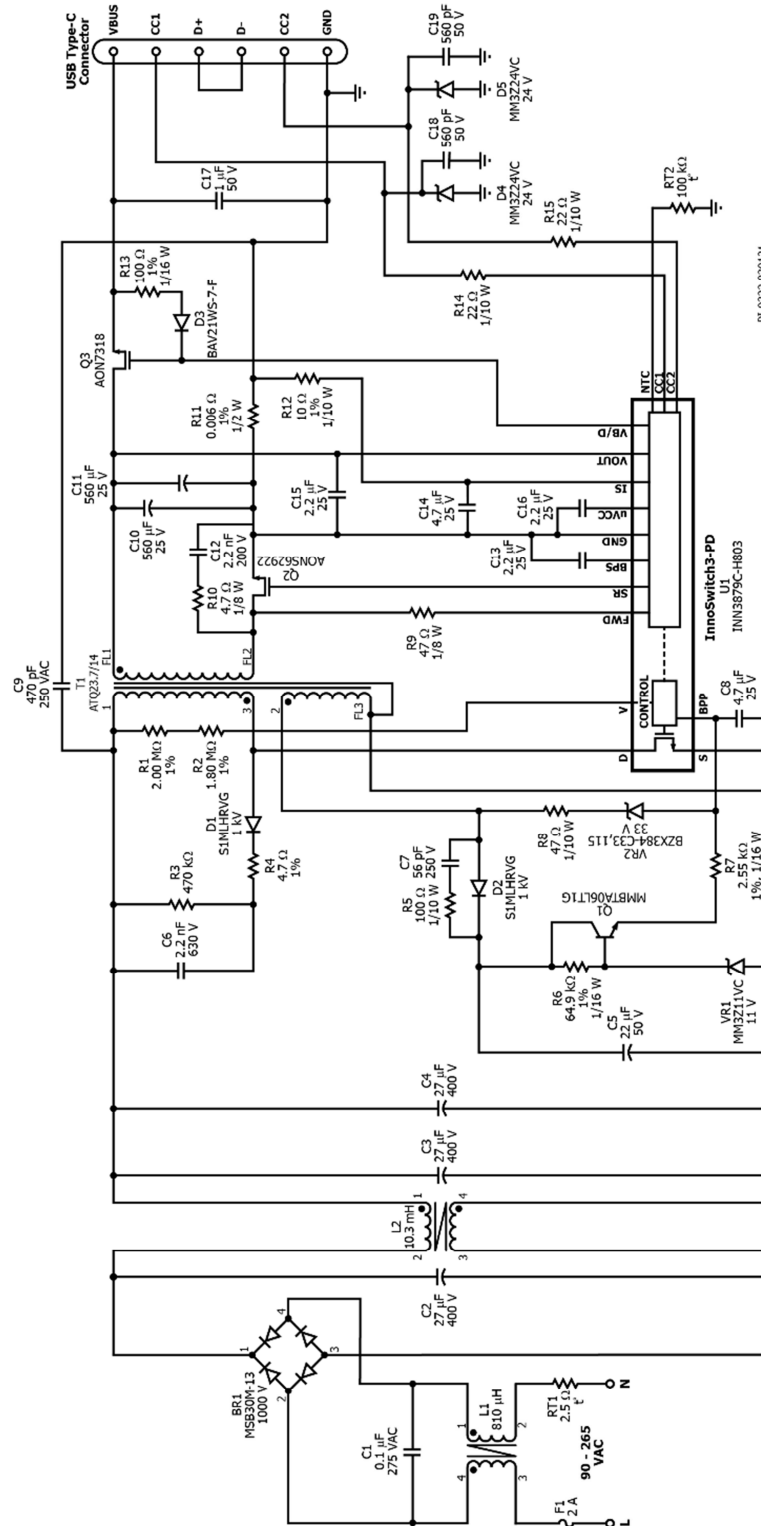


Figure 5 – DER-837 Rev D Schematic.



4 Circuit Description

4.1 *Input Rectifier and EMI Filter*

The input fuse F1 isolates the circuit and provides protection from component failure. NTC thermistor RT1 limits the inrush current when the input AC supply is connected. Common mode chokes L1 and L2, with capacitors C9 and C1 provide common mode and differential mode noise filtering for EMI attenuation. Bridge rectifier BR1 rectifies the AC line voltage to have a full wave rectified DC, which is filtered by the bulk capacitors C2, C3, and C4.

4.2 *InnoSwitch3-PD IC Primary*

One end of the flyback transformer T1 primary winding is connected to the rectified DC bus and the other end is connected to the drain terminal of the switch inside the InnoSwitch3-PD IC U1. Resistors R1 and R2 provide input voltage sensing for protection in case of AC input undervoltage or overvoltage.

A low-cost R2CD clamp formed by diode D1, resistors R3, and R4, and capacitor C6 limits the peak drain-source voltage of U1 at the instant the switch inside U1 turns off. The clamp helps to dissipate the energy stored in the leakage reactance of transformer T1.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor C8 when AC is first applied. During normal operation, the primary side block is powered from an auxiliary winding on the transformer T1. The output of the auxiliary (or bias) winding is rectified using diode D2 and filtered using capacitor C5. A linear regulator comprising resistor R6, R7, BJT Q1 and Zener diode VR1 ensures sufficient current flows through R7 into the BPP pin of the InnoSwitch3-PD IC such that the internal current source of U1 is not required to charge C8 to minimize power consumption during no-load condition and at normal operation. The RC network consisting of resistor R5 and capacitor C7 offers damping of the high frequency ringing in the voltage across diode D2 to reduce radiated EMI.

Zener diode VR2 offers primary sensed output overvoltage protection. In a flyback converter, output of the auxiliary winding tracks the output voltage of the converter. In case of overvoltage at output of the converter, the auxiliary winding voltage increases and causes breakdown of VR2 which then causes excess current to flow into the BPP pin of InnoSwitch3-PD IC. If the current flowing into the BPP pin increases above the I_{SD} threshold, the InnoSwitch3-PD controller will latch off and prevent any further increase in output voltage. Resistor R8 limits the current injected to BPP pin when the output overvoltage protection is triggered.

4.3 *InnoSwitch3-PD IC Secondary and USB Power Delivery Controller*

The secondary-side of the InnoSwitch3-PD IC provides output voltage and current sensing and a gate drive to a FET for synchronous rectification. The voltage across the



transformer secondary winding is rectified by the secondary-side synchronous rectifier FET (SR FET) Q2 and filtered by capacitors C10 and C11. High frequency ringing during switching transients that would otherwise create radiated EMI is reduced via a RC snubber, R10 and C12.

The gate of Q2 is turned on by secondary-side controller inside IC U1, based on the secondary winding voltage sensed via resistor R9 and fed into the FWD pin of the IC.

In continuous conduction mode of operation, the SR FET is turned off just prior to the secondary-side commanding a new switching cycle from the primary. In discontinuous mode of operation, the SR FET is turned off when the magnitude of the voltage drop across the SR FET falls below a threshold of approximately $V_{SR(TH)}$. Secondary-side control of the primary-side power switch avoids any possibility of cross conduction of the two switches and provides extremely reliable synchronous rectifier operation.

The secondary-side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. Capacitor C13 connected to the BPS pin of InnoSwitch3-PD IC provides decoupling for the internal circuitry.

The output current is sensed by monitoring the voltage drop across resistor R11. The current measurement is filtered with resistor R12 and capacitor C14, and then monitored across the IS and SECONDARY GROUND pins. An internal current sense threshold which is configured via the integrated secondary and USB PD controllers of InnoSwitch3-PD IC up to approximately 32 mV is used to reduce losses. Once the threshold is exceeded, the InnoSwitch3-PD IC uses variable frequency and variable primary switch peak current limit control schemes to maintain a fixed output current.

For constant current (CC) operation, when the output voltage falls, the secondary side controller inside InnoSwitch3-PD IC will power itself from the secondary winding directly. During the on-time of the primary-side power switch, the forward voltage that appears across the secondary winding is used to charge the SECONDARY BYPASS pin decoupling capacitor C13 via resistor R9 and an internal regulator. This allows output current regulation to be maintained down to the minimum UV threshold. Below this level the unit enters auto-restart until the output load is reduced.

When the output current is below the CC threshold, the converter operates in constant voltage mode. The output voltage is monitored by the VOUT pin of the InnoSwitch3-PD IC. Similar with current regulation, the output voltage is also compared to an internal voltage threshold that is set via the integrated secondary and USB PD controllers of the InnoSwitch3-PD IC and output voltage regulation is achieved by variable frequency and variable primary switch peak current limit control schemes. Capacitor C15 is needed between the VOUT pin and the SECONDARY GROUND pin for ESD protection of the VOUT pin.

N-channel MOSFET Q3 functions as the bus switch which connects or disconnects the output of the flyback converter from the USB Type-C receptacle. MOSFET Q3 is controlled by the VB/D pin on the InnoSwitch3-PD IC. Resistor R13 and diode D3 are connected across the Source and Gate terminals of the Q3 to provide a discharge path for the bus voltage when the Q3 is turned off. Capacitor C17 is used at the output for ESD protection and output voltage ripple reduction.

The USB Power Delivery (USB PD) controller is integrated within the InnoSwitch3-PD IC. Capacitor C16 connected to uVCC pin serves as a decoupling capacitor to the internal regulator which provides power to the USB PD controller. USB PD protocol is communicated over either CC1 or CC2 line depending on the orientation in which the Type-C plug is connected. Capacitors C18 and C19, resistors R14 and R15, and Zener diodes D4, and D5 provide protection from ESD to pins CC1 and CC2.



5 PCB Layout

PCB copper thickness is 0.062 inches.

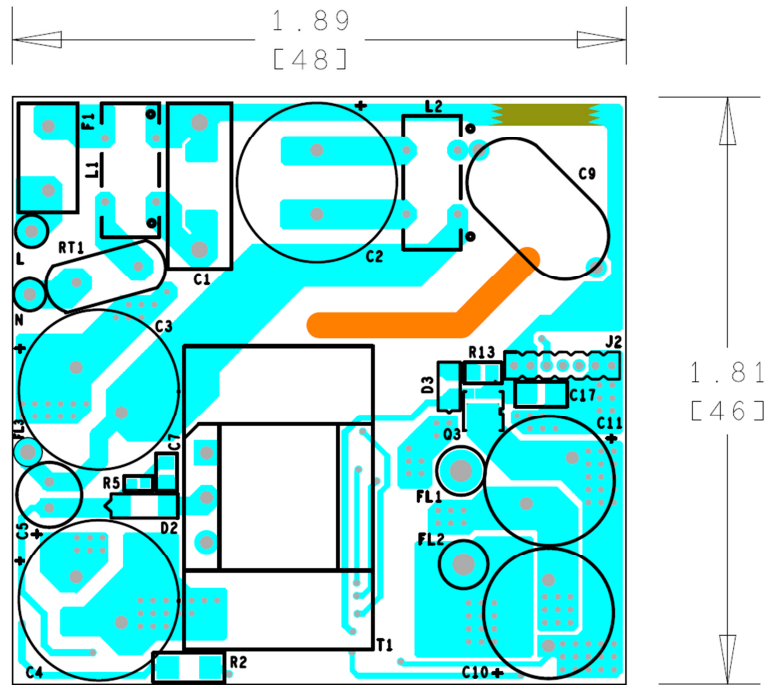


Figure 6 – DER-837 RevD PCB Layout, Top.

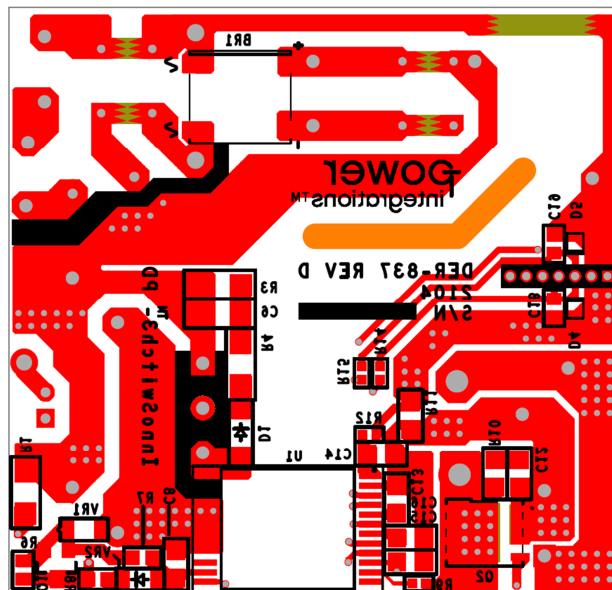


Figure 7 – DER-837 RevD PCB Layout, Bottom.

Note: Component reference J2, although present in the layout, should not be populated. Refer to Assembly Details section of this document for more information.

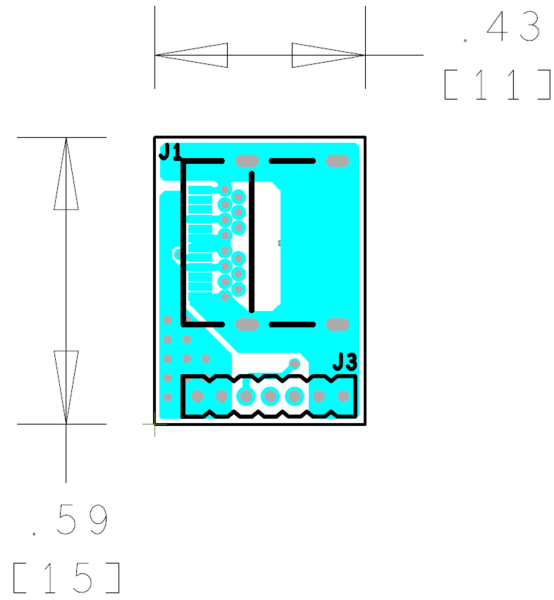


Figure 8 – DER-837 RevD USB Type-C Connector PCB Layout, Top.



Figure 9 – DER-837 RevD USB Type-C Connector PCB Layout, Bottom.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	Bridge Rectifier, Single Phase, Standard, 1 kV, 3 A, SMT, 4-MSBL, 4-SMD, Flat Leads	MSB30M-13	Diodes, Inc.
2	1	C1	0.1 μ F, 20%, 275 VAC, 560 VDC, X2, -40°C ~ 110°C, 5 mm W x 13 mm L x 11.1 mm H	R46KF310000P1M	KEMET
3	1	C2	27 μ F, \pm 20%, 400 V, Electrolytic, -40°C ~ 105°C, 12000 Hrs @ 105°C, (12.5 x 21.5)	UCY2G270MHD1TO	Nichicon
4	1	C3	27 μ F, \pm 20%, 400 V, Electrolytic, -40°C ~ 105°C, 12000 Hrs @ 105°C, (12.5 x 21.5)	UCY2G270MHD1TO	Nichicon
5	1	C4	27 μ F, \pm 20%, 400 V, Electrolytic, -40°C ~ 105°C, 12000 Hrs @ 105°C, (12.5 x 21.5)	UCY2G270MHD1TO	Nichicon
6	1	C5	22 μ F, 50 V, Electrolytic, (5 x 11)	UPW1H220MDD	Nichicon
7	1	C6	2.2 nF, 630 V, Ceramic, X7R, 1206	C3216X7R2J222K	TDK
8	1	C7	56 pF, 250 V, Ceramic, NP0, 0603	GQM1875C2E560JB12D	Murata
9	1	C8	4.7 μ F \pm 10%, 25V, X7R, 0805, -55°C ~ 125°C	TMK212AB7475KG-T	Taiyo Yuden
10	1	C9	470 pF, \pm 10%, 250 VAC, X1, Y1, Ceramic, B, Radial, Disc	DE1B3RA471KA4BN01F	Murata
11	1	C10	560 μ F, 25 V, \pm 20%, Al Organic Polymer, Gen. Purpose, Can, 15 m Ω , 2000 Hrs @ 105°C	A750MS567M1EAAE015	KEMET
12	1	C11	560 μ F, 25 V, \pm 20%, Al Organic Polymer, Gen. Purpose, Can, 15 m Ω , 2000 Hrs @ 105°C	A750MS567M1EAAE015	KEMET
13	1	C12	2.2 nF, 200 V, Ceramic, X7R, 0805	08052C222KAT2A	AVX
14	1	C13	2.2 μ F, \pm 10%, 25V, X7R, r, -55°C ~ 125°C, 0805	CL21B225KAFVPNE	Samsung
15	1	C14	4.7 μ F \pm 10%, 25V, X7R, 0805, -55°C ~ 125°C	TMK212AB7475KG-T	Taiyo Yuden
16	1	C15	2.2 μ F, \pm 10%, 25V, X7R, r, -55°C ~ 125°C, 0805	CL21B225KAFVPNE	Samsung
17	1	C16	2.2 μ F, \pm 10%, 25V, X7R, r, -55°C ~ 125°C, 0805	CL21B225KAFVPNE	Samsung
18	1	C17	1 μ F, \pm 20%, 50 V, Ceramic, X7R, Boardflex Sensitive, 0805	CGA4J3X7R1H105M125AE	TDK
19	1	C18	560 pF, 50 V, Ceramic, X7R, 0603, 0.063" L x 0.031" W (1.60 mm x 0.80 mm)	CC0603KRX7R9BB561	Yageo
20	1	C19	560 pF, 50 V, Ceramic, X7R, 0603, 0.063" L x 0.031" W (1.60 mm x 0.80 mm)	CC0603KRX7R9BB561	Yageo
21	1	D1	Diode, Standard, 1000 V, 1 A, SMT, Sub SMA	S1MLHRVG	TAIWAN SEMI
22	1	D2	Diode, Standard, 1000 V, 1 A, SMT, Sub SMA	S1MLHRVG	TAIWAN SEMI
23	1	D3	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diodes, Inc.
24	1	D4	DIODE, ZENER, 24 V, 200 mW, SC-90, SOD-323F	MM3Z24VC	ON Semi
25	1	D5	DIODE, ZENER, 24 V, 200 mW, SC-90, SOD-323F	MM3Z24VC	ON Semi
26	1	F1	2 A, 250V, Slow, Long Time Lag, RST	RST 2	Belfuse
27	1	J1	Connector, "Certified", USB - C, USB 3.1, For 0.062" PCB Material!, Superspeed+, Receptacle Connector, 24 Position, SMT, RA, Through Hole	632723300011	Würth
28	1	J3	8 Position (1 x 8) header, 0.050" (1.27mm) pitch, Gold, R/A	M50-3930842	Harwin
29	1	L1	Toroidal Common Mode Choke L1, 810 μ H, CUSTOM, DER-837	32-00409-00	Power Integrations
30	1	L2	Toroidal Common Mode Choke L1, 10.3 mH, CUSTOM, DER-837	32-00410-00	Power Integrations
31	1	Q1	NPN, Small Signal BJT, 80 V, 0.5 A, SOT-23	MMBTA06LT1G	On Semi
32	1	Q2	MOSFET, N-CH, 120 V, 85 A (at VGS = 10 V), Trench Power AlphaSGT 120 V TM technology, DFN5X6	AONS62922	Alpha & Omega Semi
33	1	Q3	N-Channel 30V 36.5A (Ta), 50A (Tc) 4.1W (Ta), 39 W (Tc) SMT 8-DFN-EP (3.3x3.3), 8DFN, 8-PowerVDFN	AON7318	Alpha & Omega Semi
34	1	R1	RES, 2.00 M Ω , 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2004V	Panasonic
35	1	R2	RES, 1.80 M Ω , 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1804V	Panasonic
36	1	R3	RES, 470 k Ω , 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ474V	Panasonic

37	1	R4	RES, 4.7 Ω , 1%, 1/4 W, Thick Film, 1206	ERJ-8RQF4R7V	Panasonic
38	1	R5	RES, 100 Ω , 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ101X	Panasonic
39	1	R6	RES, 64.9 k Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF6492V	Panasonic
40	1	R7	RES, 2.55 k Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF2551V	Panasonic
41	1	R8	RES, 47 Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ470V	Panasonic
42	1	R9	RES, 47 Ω , 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ470X	Panasonic
43	1	R10	RES, 4.7 Ω , 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ4R7V	Panasonic
44	1	R11	RES, 0.006 Ω , $\pm 1\%$, 1/2 W, 0805, Current Sense, Thick Film, $\pm 300\text{ppm}/^\circ\text{C}$, $-55^\circ\text{C} \sim 155^\circ\text{C}$	ERJ-6LWFR006V	Panasonic
45	1	R12	RES, 10 Ω , 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF10R0X	Panasonic
46	1	R13	RES, 100 Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1000V	Panasonic
47	1	R14	RES, 22 Ω , 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ220X	Panasonic
48	1	R15	RES, 22 Ω , 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ220X	Panasonic
49	1	RT1	NTC Thermistor, 2.5 Ω , 3 A	SL08 2R503	Ametherm
50	1	RT2	NTC Thermistor, 100 k Ω , 1%, 4250K, 0603	NCU18WF104F60RB	Murata
51	1	T1	Custom, DER-837 Transformer ATQ23.7-14, Lp = 425 μH		Power Integrations
52	1	U1	InnoSwitch3-PD, InSOP24D	INN3879C-H803	Power Integrations
53	1	VR1	11 V, $\pm 5\%$, 200 mW, SOD-323	MM3Z11VC	ON Semi
54	1	VR2	33 V, $\pm 5\%$, 300 mW, SOD-323	BZX384-C33,115	Nexperia

7 Transformer Specification (T1)

7.1 Electrical Diagram

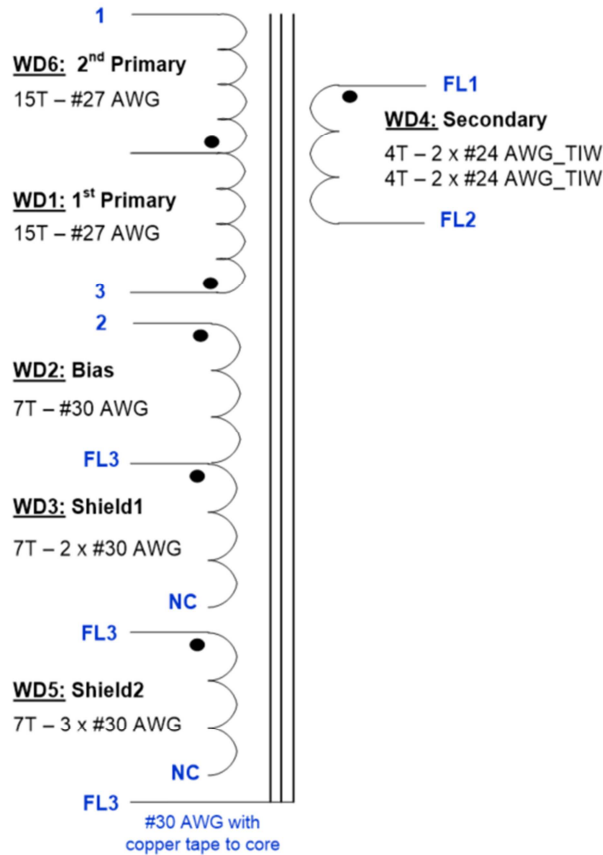


Figure 10 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Parameter	Condition	Spec.
Nominal Primary Inductance	Across pin 1 to pin 3, with all other windings open. LCR meter L_S measurement, 100 kHz, 1.0 V test level.	425 μ H \pm 7%
Primary Leakage Inductance	Across pin 1 to pin 3, with FL1 and FL2 shorted LCR meter L_S measurement, 100 kHz, 1.0 V test level.	5.5 μ H (Max.)
Resonant Frequency	Across Pin 1 to Pin 3, with all other windings open.	1,200 kHz (Min.)
Electrical Strength (Primary to Secondary)	Across shorted primary windings (pins 1, 2, 3, FL3) to shorted secondary winding (FL1, FL2).	3000 VAC, 200 V/s ramp rate, 60 s soak

7.3 Transformer Build Diagram

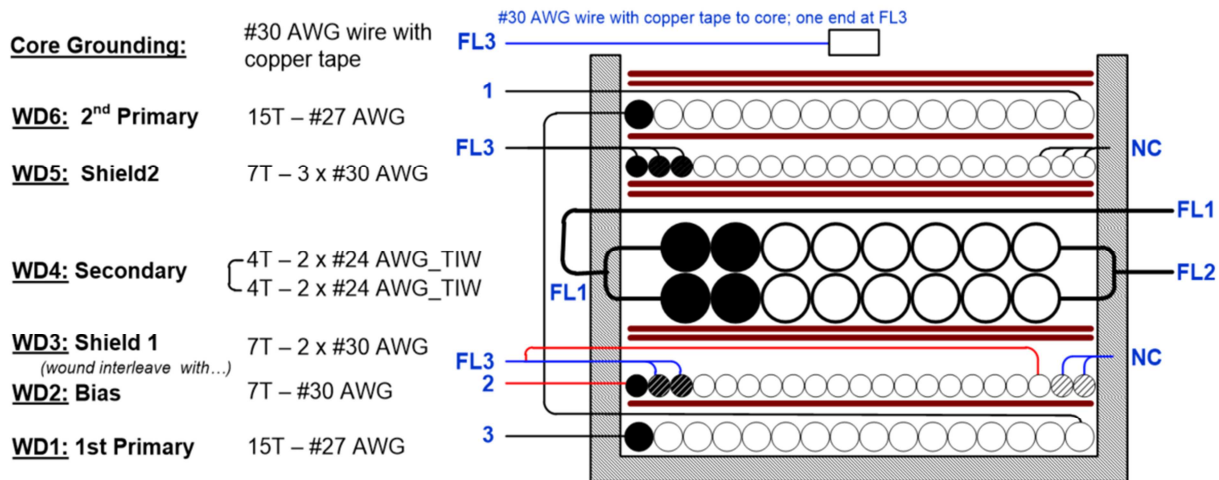


Figure 11 – Transformer Build Diagram.

7.4 Material List

Item	Description
[1]	Core: ATQ23.7-14, Mg/Zn Ferrite material. PI#: 99-00072-00.
[2]	Bobbin: ATQ23.7-14 horizontal. PI#: 25-01171-00.
[3]	Magnet Wire: #27 AWG, Double Coated.
[4]	Magnet Wire: #30 AWG, Double Coated.
[5]	Magnet Wire: #24 AWG, Triple Insulated Wire.
[6]	Copper Foil: Copper Tape, 1 mil Thickness, 8.6 mm Width x 10.0 mm Length.
[7]	Tape: 3M 1350F-1, Polyester Film, 1 mil Thickness, 7.0 mm Width.
[8]	Tape: 3M 1350F-1, Polyester Film, 1 mil Thickness, 20 mm Width.
[9]	Tape: 3M 1350F-1, Polyester Film, 1 mil Thickness, 12.4 mm Width.
[10]	Tape: 3M 1350F-1, Polyester Film, 1 mil Thickness, 18.2 mm Width.
[11]	Tape: 3M 1350F-1, Polyester Film, 1 mil Thickness, 5.6 mm Width.
[12]	Heat shrink: Heat shrink 3/32" inner diameter, Alpha Wire F221B3/32 BK100 or Equivalent, Cut into ~34 mm Length.
[13]	Varnish: Dolph BC-359.

7.5 *Bobbin Preparation*

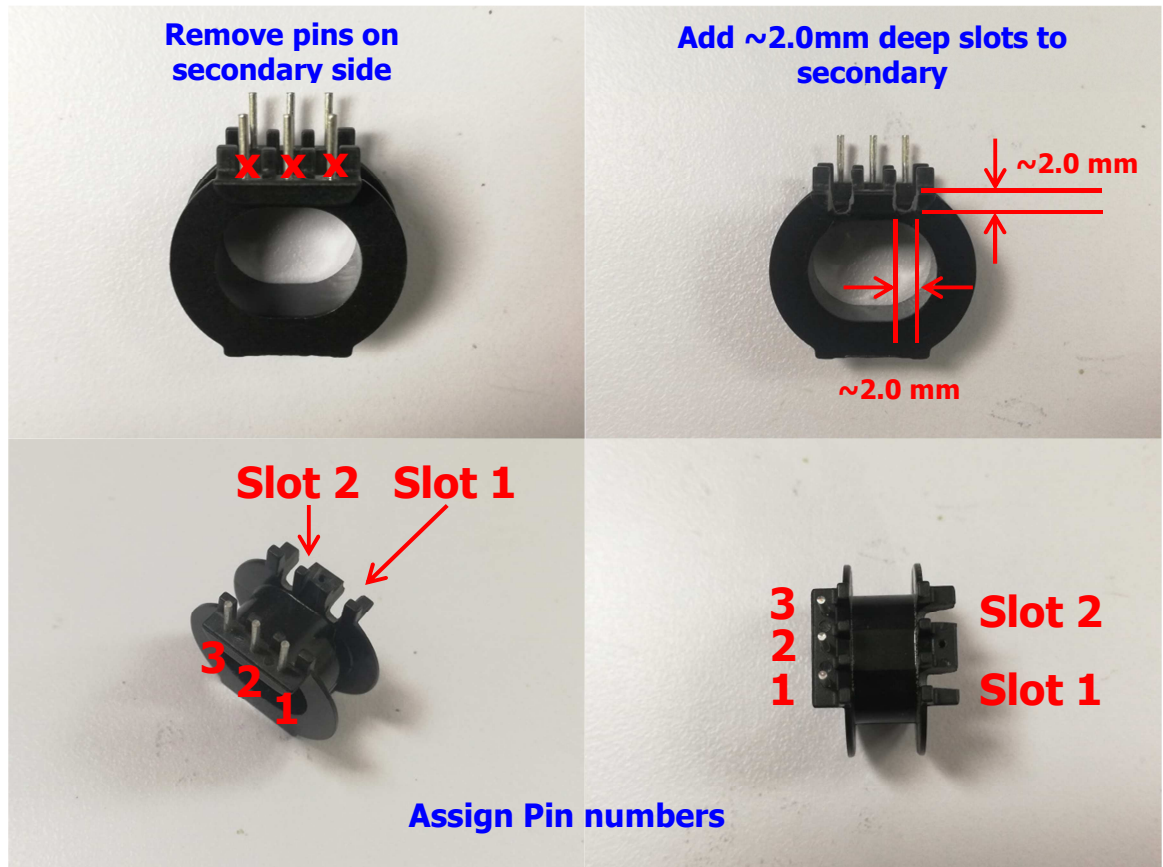
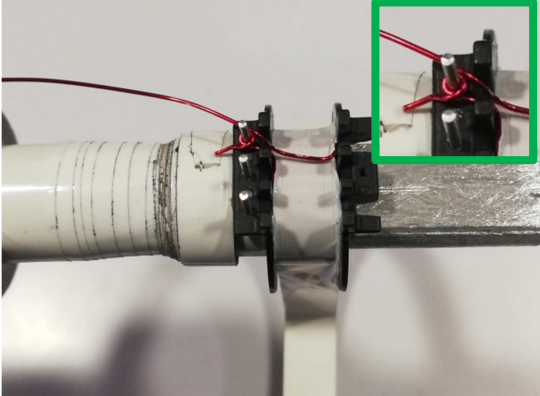
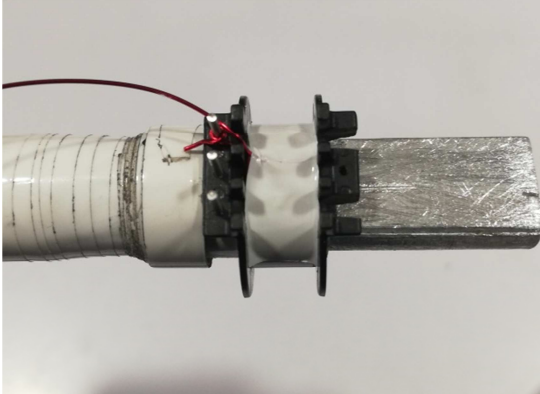
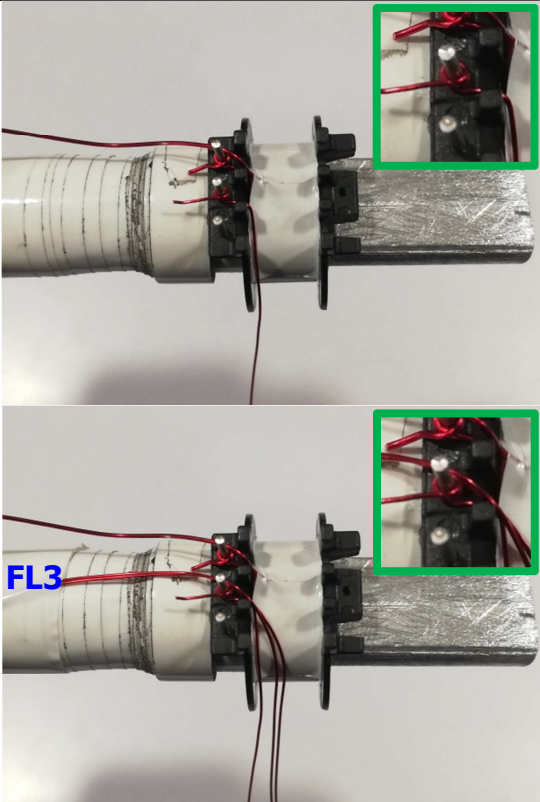
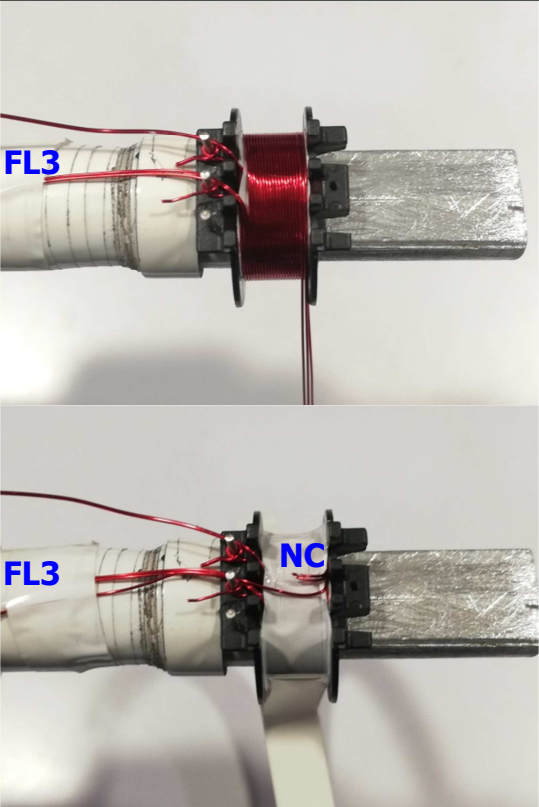
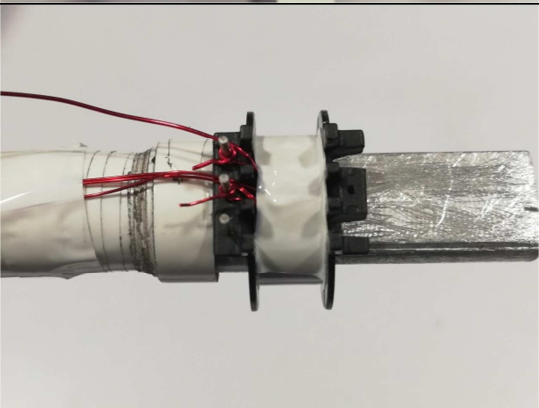
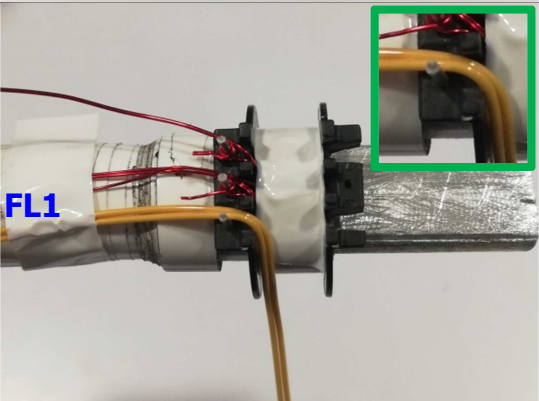


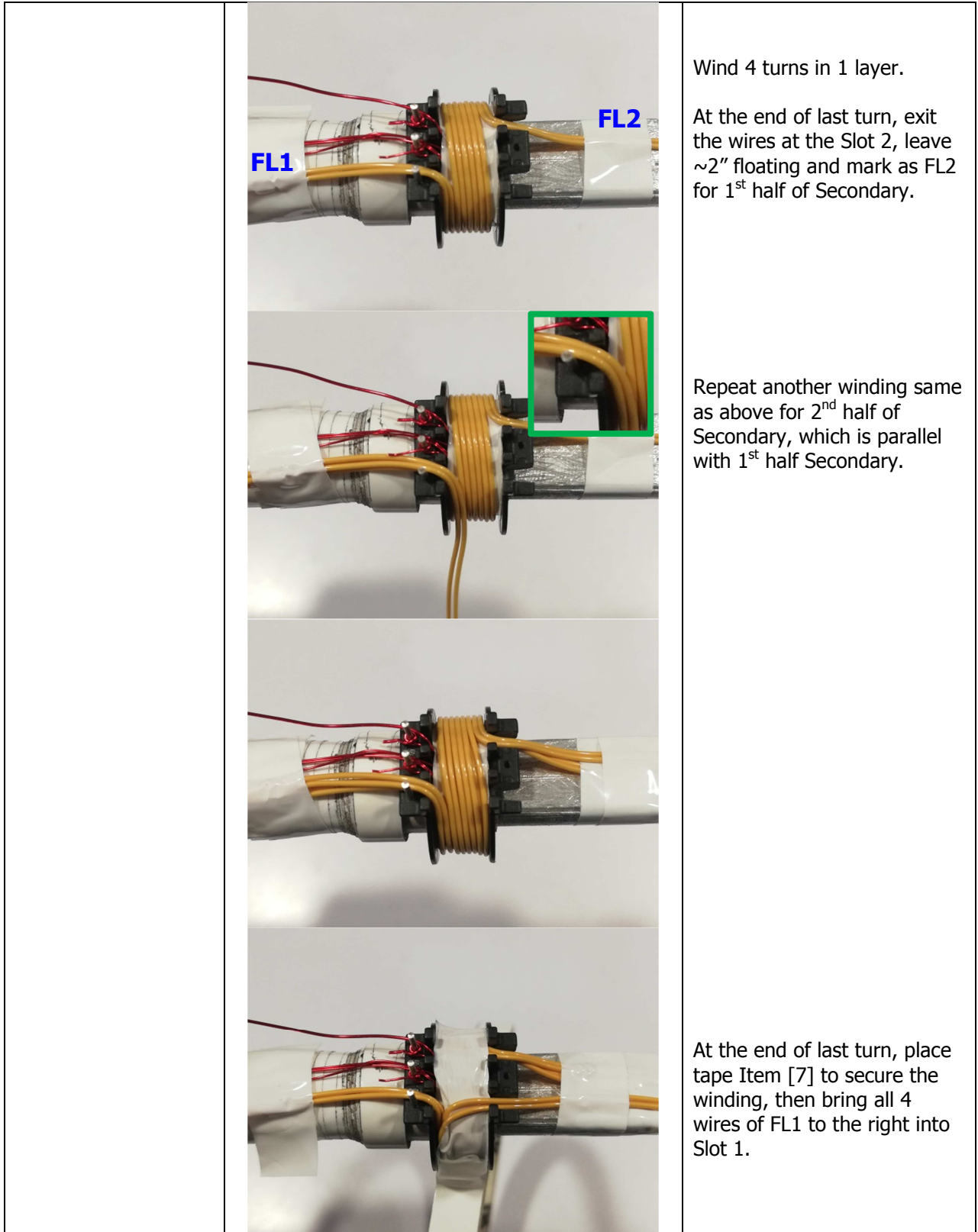
Figure 12 – Transformer Bobbin Modification and Pin Assignment.

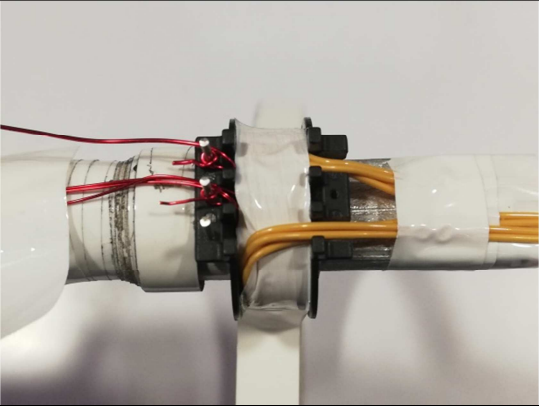
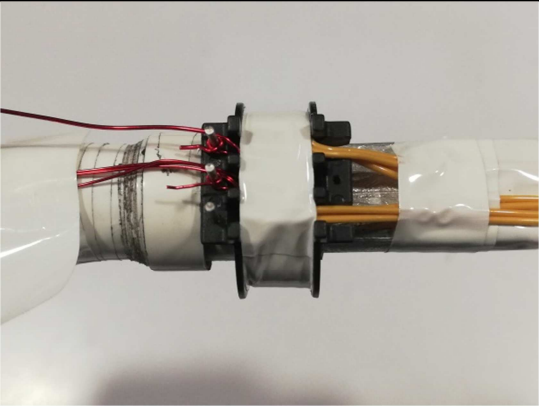
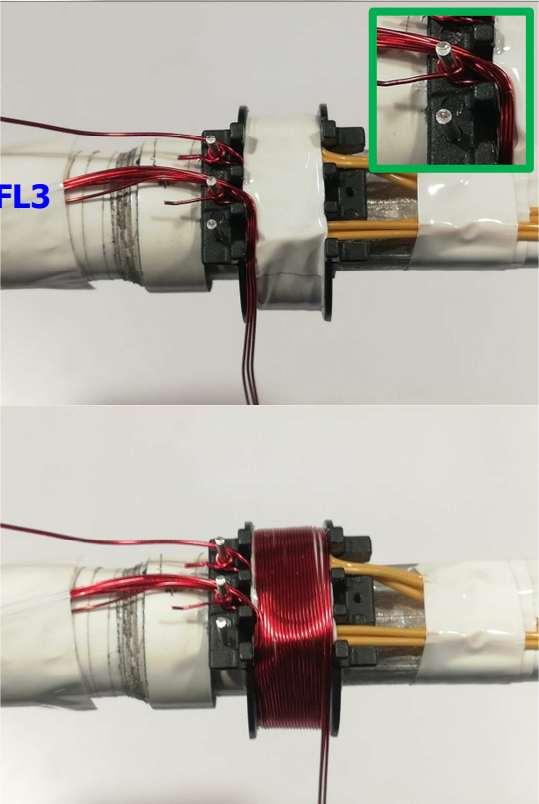
7.6 **Winding Instructions**

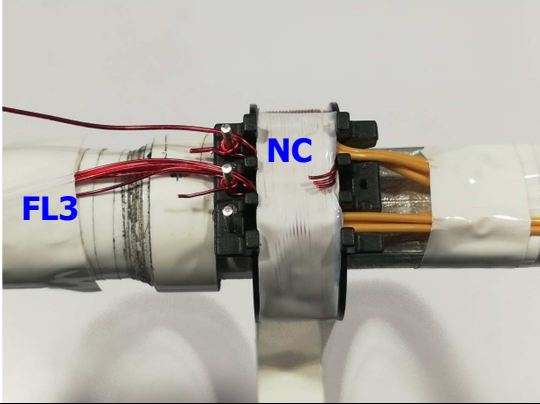

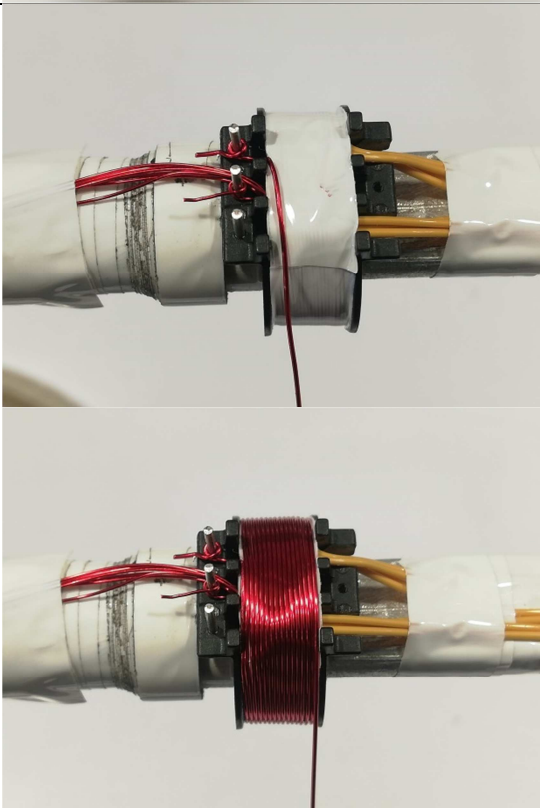
<p>Bobbin and Winding Preparation</p>	<p>Add ~2.0mm deep slots to secondary</p> <p>~2.0 mm</p> <p>~2.0 mm</p> <p>3</p> <p>2</p> <p>1</p>	<p>Remove pins on the secondary side and use a file or any appropriate grinding tool to create two ~2mm deep slots as illustrated in Bobbin Preparation section above.</p> <p>Position the bobbin on the mandrel such that the pin side of the bobbin is on the left side.</p> <p>Rotation of the mandrel is clock-wise as seen from the right side of the setup.</p>
<p>WD1 1st Primary</p>		<p>Start at pin 3, wind 15 turns of wire Item [3] in 1 layer, from left to right.</p>

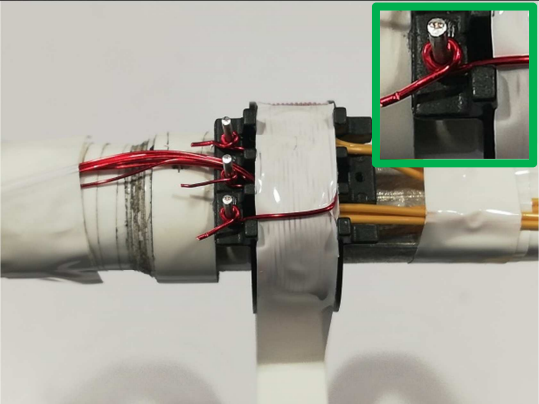
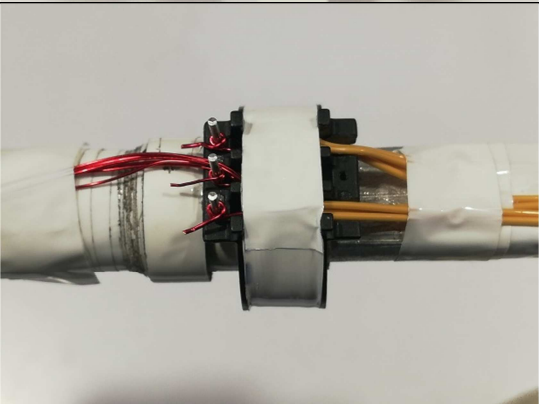
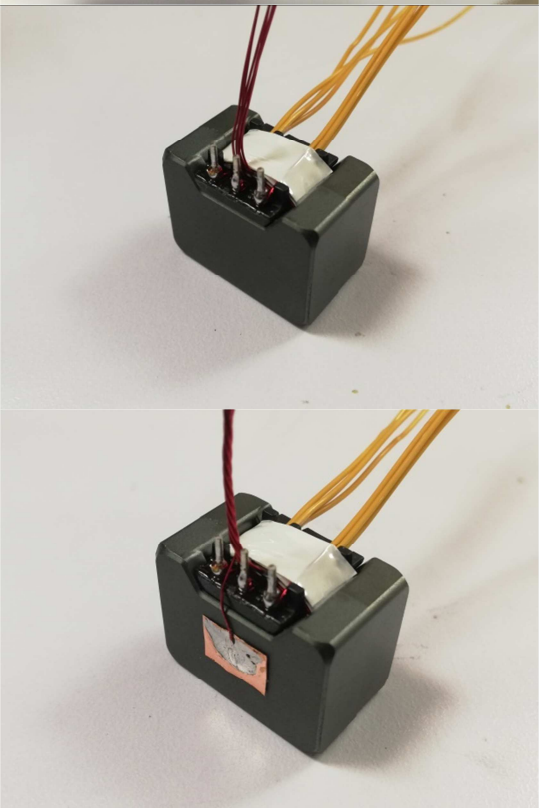
		<p>At the end of last turn, place tape Item [7] to secure the winding, then bring back wire to the left side.</p> <p>Leave enough wire for the 2nd half Primary (15 turns) to be wound later.</p>
<p>Insulation</p>		<p>1 layer of tape Item [7].</p>
<p>WD2: Bias & WD3: Shield 1</p>		<p>Start at pin 2, with 1 wire Item [4] for WD2 (Bias).</p> <p>Start another 2 wires Item [4] for WD3 (Shield), leave ~2" floating and mark as FL3.</p>

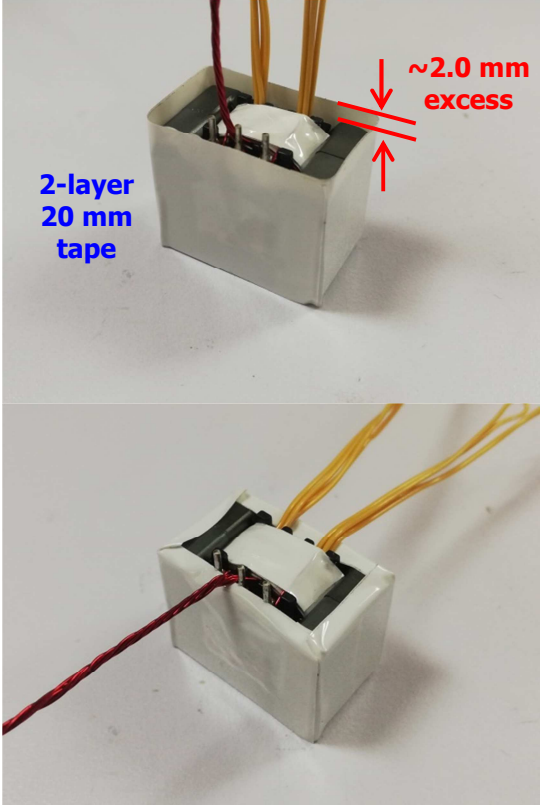
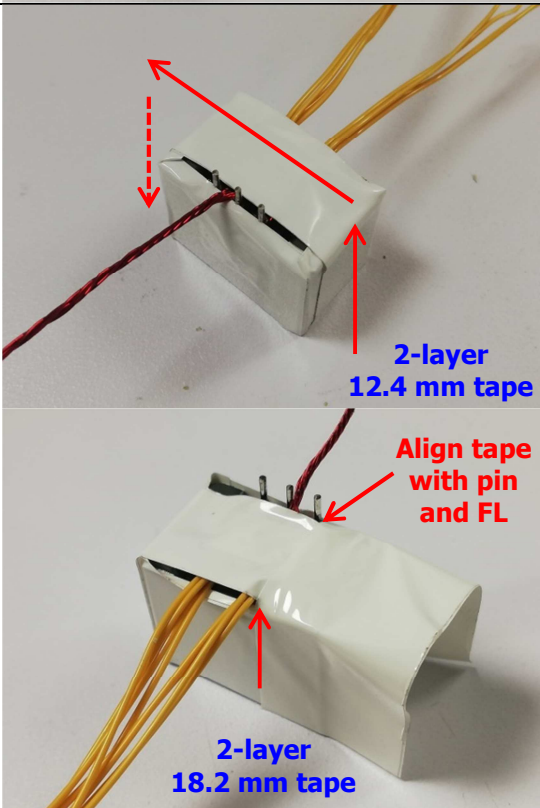
		<p>Wind all 3 wires 7 turns in parallel.</p> <p>At the end of last turn, place tape Item [7] to secure the winding, then bring back 1 wire of WD2 to the left side and combine with FL3, and cut short 2 wires for WD3 as No-Connect.</p>
<p>Insulation</p>		<p>2 layers of tape Item [7].</p>
<p>WD4 Secondary</p>		<p>Temporarily start at the slot of Pin 1. Use 2 wires Item [5], leave ~2" floating, and mark as FL1.</p>

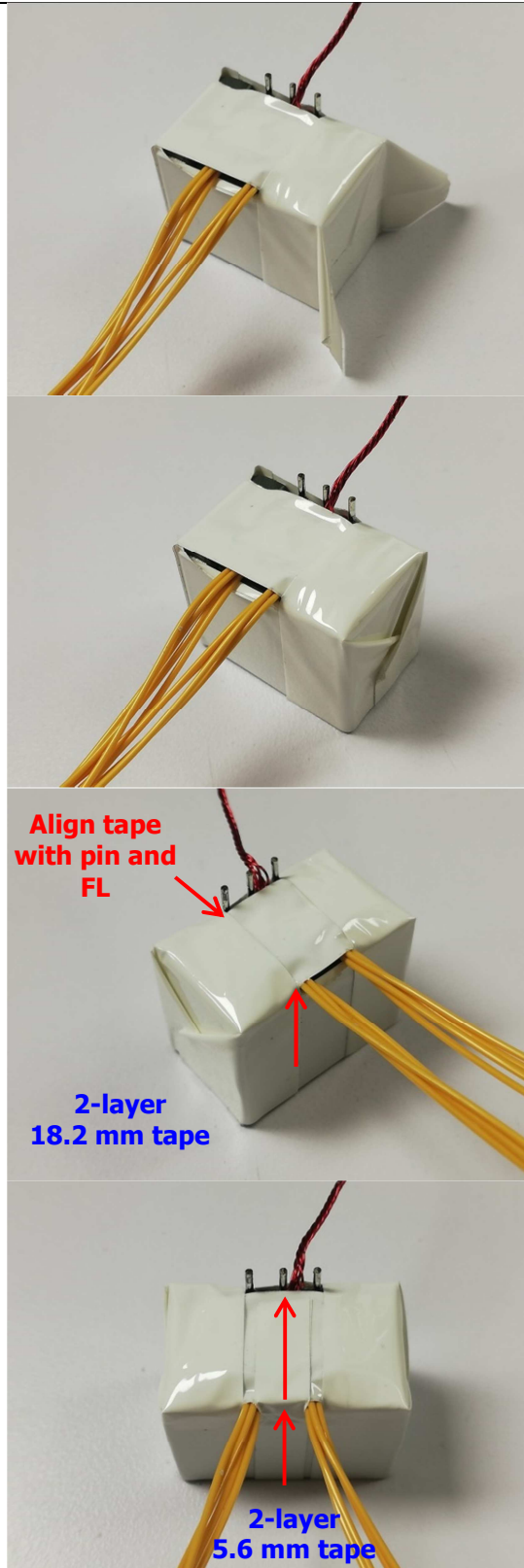


		
<p>Insulation</p>		<p>2 layers of tape Item [7].</p>
<p>WD5 Shield2</p>	 <p>FL3</p>	<p>Start at FL3, use 3 wires Item [4] and wind 7 turns in parallel.</p>

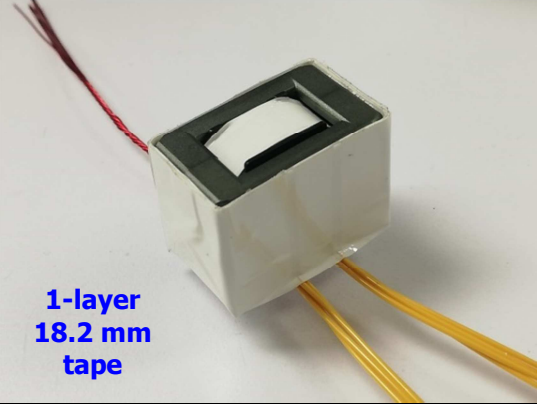
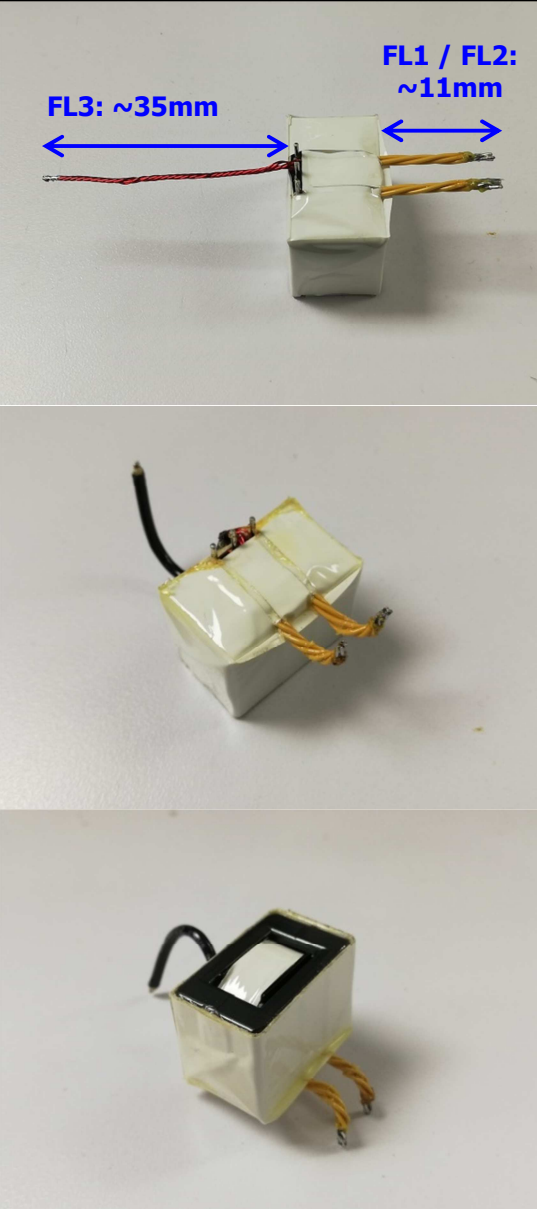
		<p>At the end of last turn, place tape Item [7] to secure the winding, then cut short the wires as No-Connect.</p>
<p>Insulation</p>		<p>1 layer of tape Item [7].</p>
<p>WD6 2nd Primary</p>		<p>Use wire hanging from WD1 and continue winding 15 turns from left to right.</p>

		<p>At the end of last turn, place tape Item [7] to secure the winding, then finish winding at Pin 1.</p>
<p>Insulation</p>		<p>2 layers of tape Item [7].</p>
<p>Gap and Ground Core</p>		<p>Solder the corresponding wires to Pins 1, 2, and 3. Add gap to the middle leg of core Item [1] to get 425 μH \pm7% primary inductance.</p> <p>Solder one end of wire Item [4] to copper tape Item [6].</p> <p>Combine the wire with FL3 and attach the copper tape to the transformer core side.</p>

	 <p>2-layer 20 mm tape</p> <p>~2.0 mm excess</p>	<p>Secure core halves by wrapping 2 layers of tape Item [8] along the transformer sides. Align the tape such that ~2mm tape is extending on transformer bottom.</p> <p>Ensure primary inductance is still 425 μH \pm7%.</p> <p>Fold the excess tape into the transformer bottom.</p>
<p>Tape for Core Insulation</p>	 <p>2-layer 12.4 mm tape</p> <p>Align tape with pin and FL</p> <p>2-layer 18.2 mm tape</p>	<p>Cover the transformer core bottom with 2 layers of tape Item [9] for improved ESD performance.</p> <p>Also secure the corners where the core is exposed with 2 layers of tape Item [10]. Align the edge of the tape to the primary pin and secondary wire.</p>



Also cover the opening between FL1 and FL2 with 2 layers of tape Item [11].

	 <p>1-layer 18.2 mm tape</p>	<p>Wrap around the core sides with 1 layer tape Item [10] to secure the assembly.</p>
<p>Finish Assembly</p>	 <p>FL1 / FL2: ~11mm FL3: ~35mm</p>	<p>Cut FL3 to ~35mm length and FL1 / FL2 to ~11mm length.</p> <p>Wrap FL3 with heat shrink Item [12].</p> <p>Varnish the transformer with Item [13].</p>

8 Common Mode Choke Specifications

8.1 810 μH Common Mode Choke (L1)

8.1.1 Electrical Diagram

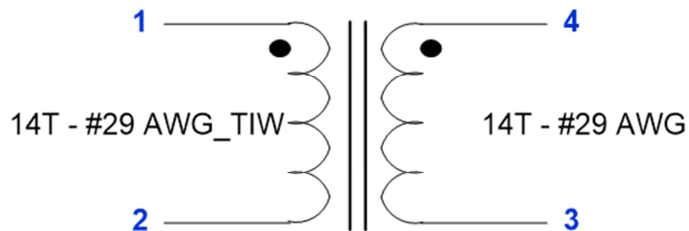


Figure 13 – Inductor Electrical Diagram.

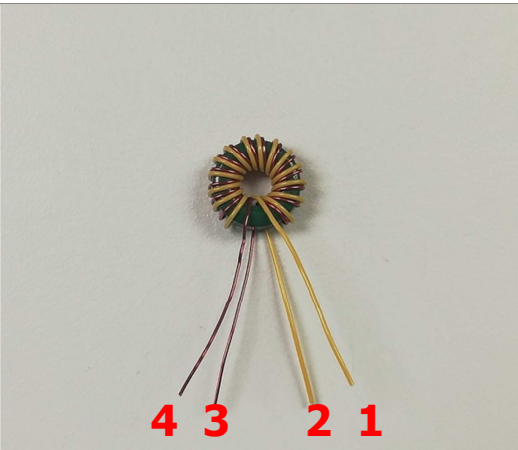
8.1.2 Electrical Specifications

Inductance	Across pin 1 to pin 2 (or pin 4 to pin 3) with the other winding open. LCR meter L_S measurement, 100 kHz switching frequency, 1.0 V test level.	810 $\mu\text{H} \pm 30\%$
Leakage Inductance	Across pin 1 to pin 2 (or pin 4 to pin 3) with the other winding shorted. LCR meter L_S measurement, 100 kHz switching frequency, 1.0 V test level.	0.3 μH (Max.)
DC Resistance	Across pin 1 to pin 2 (or pin 4 to pin 3) with the other winding open.	80 m Ω (Max.)

8.1.3 Material List

Item	Description
[1]	Core, Ferrite Inductor Toroid, 9 mm OD x 5 mm ID x 3mm H. AL = 4150 nH/N ² $\pm 30\%$ PI#: 32-00330-00.
[2]	Magnet Wire: #29 AWG, Triple Insulated Wire.
[3]	Magnet Wire: #29 AWG, Double Coated.
[4]	Varnish: Dolph BC-359.

8.1.4 Winding Instructions

	<p>Start as pin 1 for Item [2] and pin 4 for Item [3].</p> <p>Wind together 14 turns to core Item [1].</p> <p>Mark end of Item [2] as pin 2 and end of Item [3] as Pin 3.</p> <p>Varnish the CMC using Item [4].</p>
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8.2 10.3 mH Common Mode Choke (L2)

8.2.1 Electrical Diagram

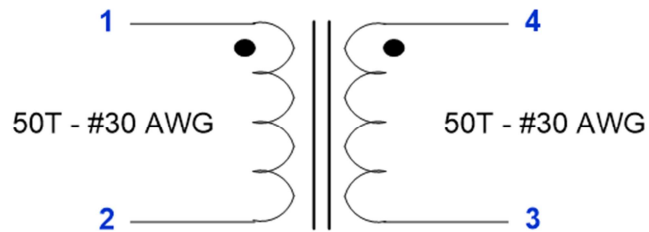


Figure 14 – Inductor Electrical Diagram.

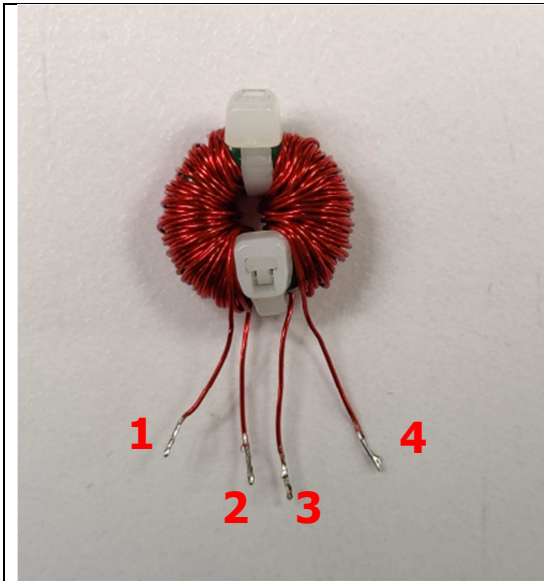
8.2.2 Electrical Specifications

Inductance	Across pin 1 to pin 2 (or pin 4 to pin 3) with the other winding open. LCR meter L_p measurement, 100 kHz switching frequency, 1.0 V test level.	10.3 mH $\pm 30\%$
Leakage Inductance	Across pin 1 to pin 2 (or pin 4 to pin 3) with the other winding shorted. LCR meter L_p measurement, 100 kHz switching frequency, 1.0 V test level.	50 μ H (Max.)
DC Resistance	Across pin 1 to pin 2 (or pin 4 to pin 3) with the other winding open.	0.6 Ω (Max.)

8.2.3 Material List

Item	Description
[1]	Core, Ferrite Inductor Toroid, 9 mm OD x 5 mm ID x 3mm H. AL = 4150 nH/N ² $\pm 30\%$ PI#: 32-00330-00.
[2]	Cable Tie, PLT.6SM-M, 1.8 mm thick. PI#: 75-00202-00
[3]	Magnet Wire: #30 AWG, Double Coated.
[4]	Varnish: Dolph BC-359.

8.2.4 Winding Instructions



Place cable ties Item [2] to divide core Item [1] into two sections.

Start as pin 1 with Item [3], wind 50 turns in four layers (18 turn on first layer + 15 turns on 2nd layer + 11 turns on 3rd layer + 6 turns on 4th layer) on the one core half. Mark end of wire as pin 2.

Repeat 50 turns of Item [3] on the next core half, starting as pin 4 and end as pin 3.

Varnish the CMC using Item [4].

9 Transformer Design Spreadsheet

1	ACDC_InnoSwitch3-PD_Flyback_020921; Rev.0.4; Copyright Power Integrations 2021	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-PD Flyback Design Spreadsheet
2	APPLICATION VARIABLES					
3	VAC_MIN	90		90	V	Minimum AC line voltage
4	VAC_MAX	265		265	V	Maximum AC input voltage
5	VAC_RANGE			UNIVERSAL		AC line voltage range
6	FLINE	50		50	Hz	AC line voltage frequency
7	CAP_INPUT	81.0		81.0	uF	Input capacitance
9	SET-POINT 1					
10	VOUT1	21.00		21.00	V	Output voltage 1, should be the highest output voltage required
11	IOUT1	2.250		2.250	A	Output current 1
12	POUT1			47.25	W	Output power 1
13	EFFICIENCY1	0.91		0.91		Converter efficiency for output 1
14	Z_FACTOR1	0.50		0.50		Z-factor for output 1
15	TYPE	APDO		APDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO (Additional Power Delivery Object)
17	SET-POINT 2					
18	VOUT2	20.00		20.14	V	Output voltage 2
19	IOUT2	2.250		2.250	A	Output current 2
20	POUT2			45.30	W	Output power 2
21	EFFICIENCY2	0.91		0.91		Converter efficiency for output 2
22	Z_FACTOR2	0.50		0.50		Z-factor for output 2
23	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO (Additional Power Delivery Object)
25	SET-POINT 3					
26	VOUT3	16.00		16.00	V	Output voltage 3
27	IOUT3	3.000		3.000	A	Output current 3
28	POUT3			48.00	W	Output power 3
29	EFFICIENCY3	0.91		0.91		Converter efficiency for output 3
30	Z_FACTOR3	0.50		0.50		Z-factor for output 3
31	TYPE	APDO		APDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO (Additional Power Delivery Object)
33	SET-POINT 4					
34	VOUT4	15.00		15.18	V	Output voltage 4
35	IOUT4	3.000		3.000	A	Output current 4
36	POUT4			45.54	W	Output power 4
37	EFFICIENCY4	0.91		0.91		Converter efficiency for output 4
38	Z_FACTOR4	0.50		0.50		Z-factor for output 4
39	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO (Additional Power Delivery Object)
41	SET-POINT 5					
42	VOUT5	11.00		11.00	V	Output voltage 5
43	IOUT5	4.050		4.050	A	Output current 5
44	POUT5			44.55	W	Output power 5
45	EFFICIENCY5	0.90		0.90		Converter efficiency for output 5
46	Z_FACTOR5	0.50		0.50		Z-factor for output 5
47	TYPE	APDO		APDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO (Additional Power Delivery Object)
49	SET-POINT 6					
50	VOUT6	9.00		9.30	V	Output voltage 6
51	IOUT6	5.000		5.000	A	Output current 6
52	POUT6			46.50	W	Output power 6



53	EFFICIENCY6	0.90		0.90		Converter efficiency for output 6
54	Z_FACTOR6	0.50		0.50		Z-factor for output 6
55	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO (Additional Power Delivery Object)
57	SET-POINT 7					
58	VOUT7	5.00		5.30	V	Output voltage 7
59	IOUT7	5.000		5.000	A	Output current 7
60	POUT7			26.50	W	Output power 7
61	EFFICIENCY7	0.89		0.89		Converter efficiency for output 7
62	Z_FACTOR7	0.50		0.50		Z-factor for output 7
63	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO (Additional Power Delivery Object)
65	SET-POINT 8					
66	VOUT8	3.30		3.30	V	Output voltage 8
67	IOUT8	5.000		5.000	A	Output current 8
68	POUT8			16.50	W	Output power 8
69	EFFICIENCY8	0.87		0.87		Converter efficiency for output 8
70	Z_FACTOR8	0.50		0.50		Z-factor for output 8
71	TYPE	APDO		APDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO (Additional Power Delivery Object)
73	SET-POINT 9					
74	VOUT9			0.00	V	Output voltage 9
75	IOUT9			0.000	A	Output current 9
76	POUT9			0.00	W	Output power 9
77	EFFICIENCY9			0.00		Converter efficiency for output 9
78	Z_FACTOR9			0.00		Z-factor for output 9
79	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO (Additional Power Delivery Object)
81	VOLTAGE_CDC	0.300		0.300	V	Cable drop compensation desired at maximum output current
85	PRIMARY CONTROLLER SELECTION					
86	ENCLOSURE	ADAPTER		ADAPTER		Power supply enclosure
87	ILIMIT_MODE	INCREASED		INCREASED		Device current limit mode
88	VDRAIN_BREAKDOWN	750		750	V	Device breakdown voltage
89	DEVICE_GENERIC	INN38X9		INN38X9		Device selection
90	DEVICE_CODE			INN3879C		Device code
91	PDEVICE_MAX			65	W	Device maximum power capability
92	RDSON_25DEG			0.44	Ω	Primary switch on-time resistance at 25°C
93	RDSON_100DEG			0.62	Ω	Primary switch on-time resistance at 100°C
94	ILIMIT_MIN			1.980	A	Primary switch minimum current limit
95	ILIMIT_TYP			2.130	A	Primary switch typical current limit
96	ILIMIT_MAX			2.279	A	Primary switch maximum current limit
97	VDRAIN_ON_PRSW			0.38	V	Primary switch on-time voltage drop
98	VDRAIN_OFF_PRSW			600.81	V	Peak drain voltage on the primary switch during turn-off
102	WORST CASE ELECTRICAL PARAMETERS					
103	FSWITCHING_MAX	75089		75089	Hz	Maximum switching frequency at full load and the valley of the minimum input AC voltage
104	VOR	157.5		157.5	V	Voltage reflected to the primary winding (corresponding to set-point 1) when the primary switch turns off
105	VMIN			82.47	V	Valley of the rectified minimum input AC voltage at full load
106	KP			0.641		Measure of continuous/discontinuous

						mode of operation
107	MODE_OPERATION			CCM		Mode of operation
108	DUTYCYCLE			0.640		Primary switch duty cycle
109	TIME_ON			11.31	us	Primary switch on-time
110	TIME_OFF			5.37	us	Primary switch off-time
111	LPRIMARY_MIN			403.8	uH	Minimum primary magnetizing inductance
112	LPRIMARY_TYP			425.0	uH	Typical primary magnetizing inductance
113	LPRIMARY_TOL			5.0	%	Primary magnetizing inductance tolerance
114	LPRIMARY_MAX			446.3	uH	Maximum primary magnetizing inductance
116	PRIMARY CURRENT					
117	IAVG_PRIMARY			0.614	A	Primary switch average current
118	IPEAK_PRIMARY			2.116	A	Primary switch peak current
119	IPEDESTAL_PRIMARY			0.682	A	Primary switch current pedestal
120	IRIPPLE_PRIMARY			2.109	A	Primary switch ripple current
121	IRMS_PRIMARY			0.931	A	Primary switch RMS current
123	SECONDARY CURRENT					
124	IPEAK_SECONDARY			15.868	A	Secondary winding peak current
125	IPEDESTAL_SECONDARY			5.113	A	Secondary winding pedestal current
126	IRMS_SECONDARY			7.596	A	Secondary winding RMS current
127	IRIPPLE_CAP_OUT			5.719	A	Output capacitor ripple current
131	TRANSFORMER CONSTRUCTION PARAMETERS					
132	CORE SELECTION					
133	CORE	ATQ23.7/14.6	Info	ATQ23.7/14.6		The transformer windings may not fit: pick a bigger core or bobbin and refer to the Transformer Parameters tab for fit calculations
134	CORE NAME			ATQ23.7/14.6		Core code
135	AE			103.0	mm ²	Core cross sectional area
136	LE			38.2	mm	Core magnetic path length
137	AL			7200	nH/N ²	Ungapped core effective inductance per turns squared
138	VE			3935	mm ³	Core volume
139	BOBBIN NAME			TBI-238-10051.17XX		Bobbin name
140	AW			22.1	mm ²	Bobbin window area
141	BW			6.60	mm	Bobbin width
142	MARGIN			0.0	mm	Bobbin safety margin
144	PRIMARY WINDING					
145	NPRIMARY			30		Primary winding number of turns
146	BPEAK			3369	Gauss	Peak flux density
147	BMAX			3017	Gauss	Maximum flux density
148	BAC			1502	Gauss	AC flux density (0.5 x Peak to Peak)
149	ALG			472	nH/N ²	Typical gapped core effective inductance per turns squared
150	LG			0.256	mm	Core gap length
151	LAYERS_PRIMARY			2		Primary winding number of layers
152	AWG_PRIMARY			27		Primary wire gauge
153	OD_PRIMARY_INSULATED			0.418	mm	Primary wire insulated outer diameter
154	OD_PRIMARY_BARE			0.361	mm	Primary wire bare outer diameter
155	CMA_PRIMARY			216.5	Cmils/A	Primary winding wire CMA
157	SECONDARY WINDING					
158	NSECONDARY	4		4		Secondary winding number of turns
159	AWG_SECONDARY			18		Secondary wire gauge
160	OD_SECONDARY_INSULATED			1.328	mm	Secondary wire insulated outer diameter
161	OD_SECONDARY_BARE			1.024	mm	Secondary wire bare outer diameter
162	CMA_SECONDARY			213.8	Cmils/A	Secondary winding wire CMA



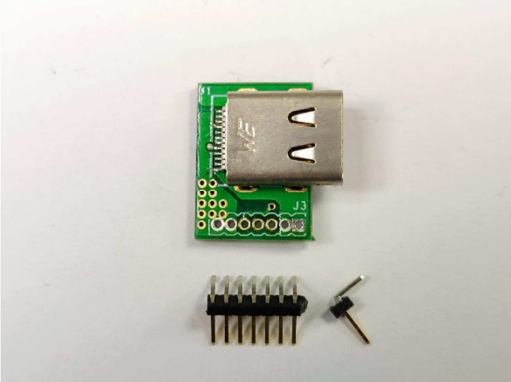
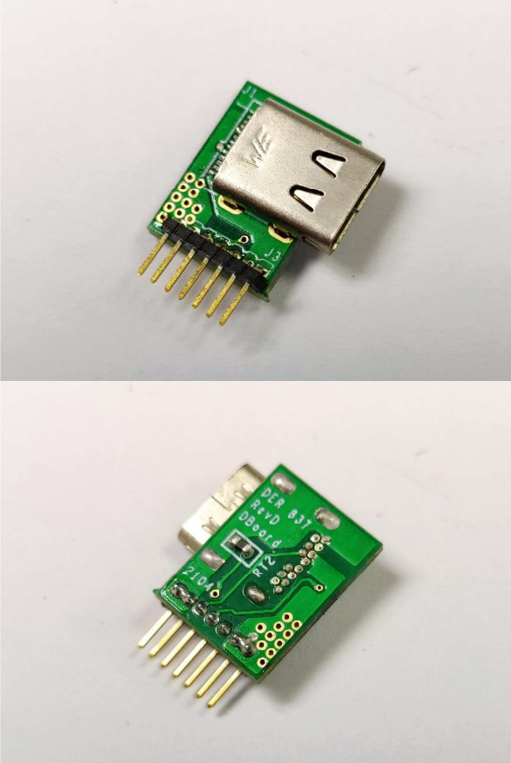
164	BIAS WINDING					
165	NBIAS			8		Bias winding number of turns
169	PRIMARY COMPONENTS SELECTION					
170	LINE UNDERVOLTAGE					
171	BROWN-IN REQUIRED	72.00		72.00	V	Required line brown-in threshold
172	RLS			3.82	MΩ	Connect two 1.91 MOhm resistors to the V-pin for the required UV/OV threshold
173	BROWN-IN ACTUAL			72.58	V	Actual brown-in threshold using standard resistors
174	BROWN-OUT ACTUAL			63.94	V	Actual brown-out threshold using standard resistors
176	LINE OVERVOLTAGE					
177	OVERVOLTAGE_LINE		Warning	319.20	V	The device voltage stress will be higher than 650V when overvoltage is triggered
179	BIAS WINDING					
180	VBIAS	9.00		9.00	V	Rectified bias voltage at the lowest output set-point
181	VF_BIAS			0.70	V	Bias winding diode forward drop
182	VREVERSE_BIASDIODE			108.55	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
183	CBIAS			22	uF	Bias winding rectification capacitor
184	CBPP			4.70	uF	BPP pin capacitor
188	SECONDARY COMPONENTS SELECTION					
189	RECTIFIER					
190	VDRAIN_OFF_SRFET			70.77	V	Secondary rectifier reverse voltage (not accounting parasitic voltage ring)
191	SRFET	AONS62922		AONS62922		Secondary rectifier (Logic MOSFET)
192	VBREAKDOWN_SRFET			120	V	Secondary rectifier breakdown voltage
193	RDSON_SRFET			7.0	mΩ	SRFET on time drain resistance at 25degC for VGS=4.4V
197	SET-POINTS ANALYSIS					
198	TOLERANCE CORNER					
199	USER_VAC	90		90	V	Input AC RMS voltage corner to be evaluated
200	USER_ILIMIT	MIN		1.980	A	Current limit corner to be evaluated
201	USER_LPRIMARY	MIN		403.8	uH	Primary inductance corner to be evaluated
203	SET-POINT SELECTION					
204	SET-POINT	6		6		Select the set-point which needs to be evaluated
205	FSWITCHING			75089.0	Hz	Switching frequency at full load and valley of the rectified minimum AC input voltage
206	VOR			70.2	V	Voltage reflected to the primary winding when the primary switch turns off
207	VMIN			83.41	V	Valley of the minimum input AC voltage
208	KP			0.654		Measure of continuous/discontinuous mode of operation
209	MODE_OPERATION			CCM		Mode of operation
210	DUTYCYCLE			0.458		Primary switch duty cycle
211	TIME_ON			6.10	us	Primary switch on-time
212	TIME_OFF			7.22	us	Primary switch off-time
214	PRIMARY CURRENT					
215	I AVG_PRIMARY			0.591	A	Primary switch average current
216	IPEAK_PRIMARY			1.918	A	Primary switch peak current
217	IPEDESTAL_PRIMARY			0.663	A	Primary switch current pedestal

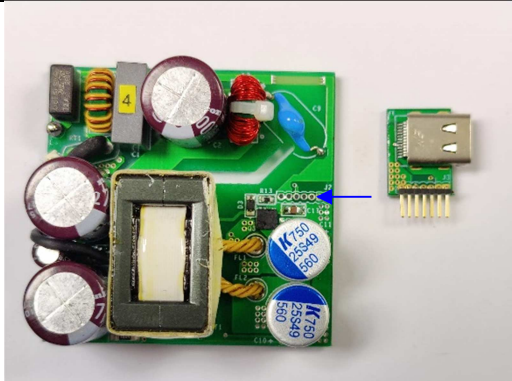
218	IRIPPLE_PRIMARY			1.254	A	Primary switch ripple current
219	IRMS_PRIMARY			0.907	A	Primary switch RMS current
221	SECONDARY CURRENT					
222	IPEAK_SECONDARY			14.384	A	Secondary winding peak current
223	IPEDESTAL_SECONDARY			4.975	A	Secondary winding pedestal current
224	IRMS_SECONDARY			7.401	A	Secondary winding RMS current
225	IRIPPLE_CAP_OUT			5.457	A	Output capacitor ripple current
227	MAGNETIC FLUX DENSITY					
228	BPEAK			2648	Gauss	Peak flux density
229	BMAX			2506	Gauss	Maximum flux density
230	BAC			820	Gauss	AC flux density (0.5 x Peak to Peak)

Note: The warning on line 177 (OVERVOLTAGE_LINE) has been verified to not be an issue for this design. The primary switch of INN3879C-H803 is rated at 750 V.

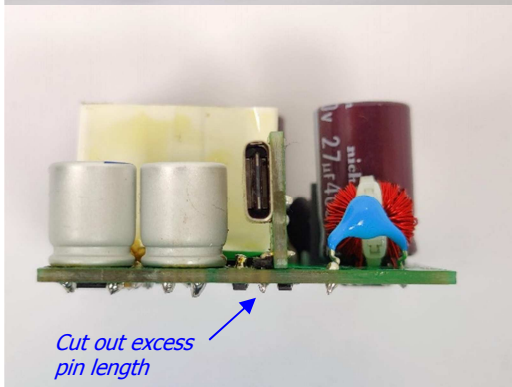
10 Assembly Details

10.1 USB Type-C PCB Assembly

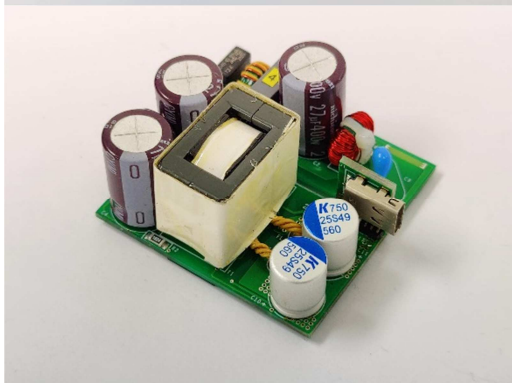
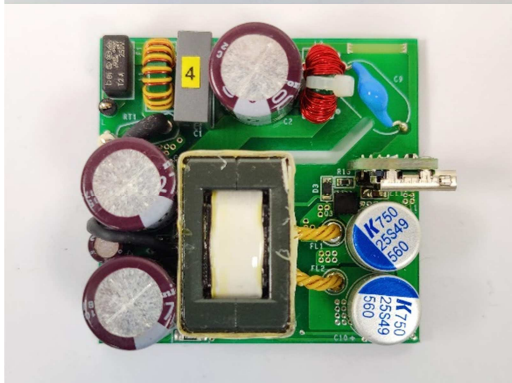
	<p>Remove one pin from header J3 to reduce total pin count to 7.</p>
	<p>Populate J3 to the USB Type-C PCB.</p>



Solder USB Type-C PCB header into the main board J2.



Cut short excess pin length from the 7-pin header.



11 Performance Data

Note: 1. Output voltage measured on the PCB unless otherwise specified.
2. Measurements taken at room temperature ambient (approximately 25 °C) unless otherwise specified.

11.1 *No-Load Input Power at 5 V_{OUT}*

Note: 1. Unit tested without Type-C cable connected to output.
2. For each line voltage, soak time = 10 min and integration time = 5 min.

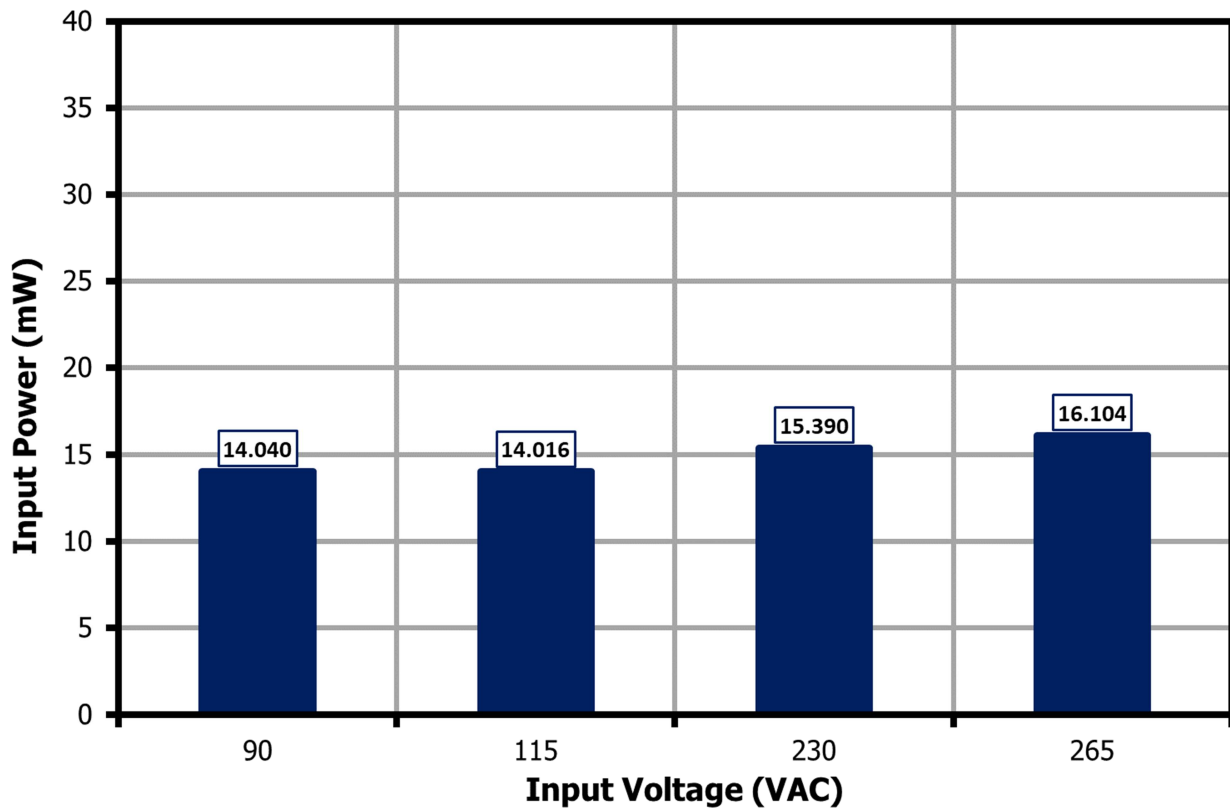


Figure 15 – No-Load Input Power vs. Input Line Voltage.

11.2 Full Load Efficiency (On-board)

V _{OUT} (V)	Load (A)	Power (W)	Full Load Efficiency (%)			
			90 VAC	115 VAC	230 VAC	265 VAC
5	5.0	25	89.34	90.34	90.63	90.37
9	5.0	45	89.72	91.03	92.19	92.01
15	3.0	45	91.17	92.19	92.95	92.82
20	2.25	45	91.10	92.15	92.92	92.77

11.3 Average and 10% Load Efficiency

11.3.1 Efficiency Requirements

		Test	Average Efficiency (%)		10% Load Efficiency (%)
			Effective	2016	Jan-16
V _{OUT} (V)	Model (V)	Power (W)	New EISA2007	CoC v5 Tier 2	CoC v5 Tier 2
5	<6	25	84.25	85.00	75.47
9	>6	45	87.73	88.85	78.85
15	>6	45	87.73	88.85	78.85
20	>6	45	87.73	88.85	78.85

11.3.2 Efficiency Performance Summary (On Board)

V _{OUT} (V)	Power (W)	Average Efficiency (%)		10% Load Efficiency (%)	
		115 VAC	230 VAC	115 VAC	230 VAC
5	25	91.01	90.55	90.72	87.41
9	45	91.75	92.05	90.62	88.40
15	45	92.03	92.27	87.59	85.72
20	45	91.55	91.80	84.70	82.72

11.3.3 Average and 10% Load Efficiency Measurements

Measurements were taken after 30-minute delay per input line voltage and 1-minute delay per load condition. Output voltage was measured on the board.

11.3.3.1 Output: 5 V / 5 A

Input (VAC)	Load (%)	Design Performance					Efficiency Standards		Remarks	
		PIN (W)	VOUT (V)	IOUT (A)	POUT (W)	Efficiency (%)	Average Efficiency (%)	DOE6 (%)		CoC v5 Tier 2 (%)
115	100	28.860	5.213	5.001	26.071	90.34	91.01	84.25	85.00	PASS
	75	21.360	5.169	3.751	19.389	90.77				
	50	14.009	5.115	2.501	12.791	91.31				
	25	6.885	5.046	1.250	6.309	91.63				
	10	2.758	5.004	0.500	2.502	90.72				
230	100	28.880	5.234	5.001	26.174	90.63	90.55	84.25	85.00	PASS
	75	21.420	5.185	3.751	19.449	90.80				
	50	14.100	5.124	2.501	12.812	90.87				
	25	7.020	5.049	1.250	6.312	89.91				
	10	2.867	5.011	0.500	2.506	87.41				

11.3.3.2 Output: 9 V / 5 A

Input (VAC)	Load (%)	Design Performance					Efficiency Standards		Remarks	
		PIN (W)	VOUT (V)	IOUT (A)	POUT (W)	Efficiency (%)	Average Efficiency (%)	DOE6 (%)		CoC v5 Tier 2 (%)
115	100	50.680	9.225	5.001	46.134	91.03	91.75	87.73	88.85	PASS
	75	37.540	9.181	3.751	34.437	91.73				
	50	24.820	9.138	2.501	22.849	92.06				
	25	12.304	9.072	1.250	11.341	92.17				
	10	4.977	9.020	0.500	4.510	90.62				
230	100	50.200	9.254	5.001	46.277	92.19	92.05	87.73	88.85	PASS
	75	37.440	9.209	3.751	34.542	92.26				
	50	24.800	9.149	2.501	22.877	92.25				
	25	12.400	9.078	1.250	11.349	91.52				
	10	5.104	9.025	0.500	4.512	88.40				

11.3.3.3 Output: 15 V / 3 A

Input (VAC)	Load (%)	Design Performance					Efficiency Standards		Remarks	
		PIN (W)	VOUT (V)	IOUT (A)	POUT (W)	Efficiency (%)	Average Efficiency (%)	DOE6 (%)		CoC v5 Tier 2 (%)
115	100	49.370	15.171	3.000	45.513	92.19	92.03	87.73	88.85	PASS
	75	36.920	15.144	2.250	34.070	92.28				
	50	24.570	15.111	1.500	22.660	92.23				
	25	12.348	15.064	0.750	11.290	91.43				
	10	5.133	15.024	0.299	4.496	87.59				
230	100	49.050	15.198	3.000	45.594	92.95	92.27	87.73	88.85	PASS
	75	36.750	15.164	2.250	34.118	92.84				
	50	24.530	15.124	1.500	22.679	92.45				
	25	12.430	15.068	0.749	11.293	90.85				
	10	5.247	15.031	0.299	4.498	85.72				

11.3.3.4 Output: 20 V / 2.25 A

Input (VAC)	Load (%)	Design Performance					Efficiency Standards			Remarks
		PIN (W)	VOUT (V)	IOUT (A)	POUT (W)	Efficiency (%)	Average Efficiency (%)	DOE6 (%)	CoC v5 Tier 2 (%)	
115	100	49.210	20.158	2.250	45.345	92.15	91.55	87.73	88.85	PASS
	75	36.880	20.133	1.687	33.957	92.07				
	50	24.630	20.102	1.124	22.599	91.75				
	25	12.494	20.063	0.562	11.272	90.22				
	10	5.301	20.028	0.224	4.490	84.70		78.85	PASS	
230	100	48.880	20.190	2.250	45.419	92.92	91.80	87.73	88.85	PASS
	75	36.700	20.156	1.687	33.997	92.63				
	50	24.580	20.119	1.124	22.617	92.01				
	25	12.580	20.071	0.562	11.276	89.63				
	10	5.427	20.034	0.224	4.491	82.75		78.85	PASS	



11.4 **Efficiency Across Line at 100% Load (On Board)**

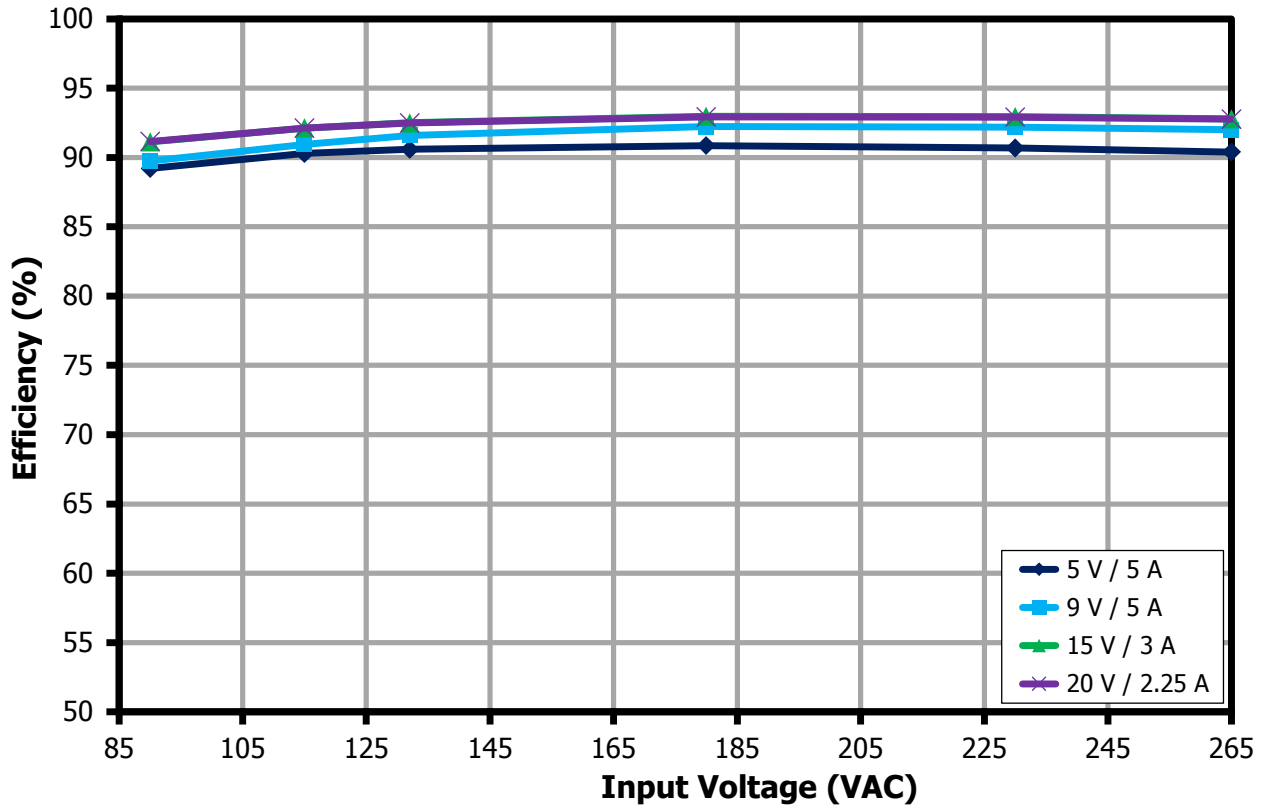


Figure 16 – Full Load Efficiency vs. Input Line for 5 V, 9 V, 15 V, and 20 V Output, Room Temperature.



11.5 Efficiency Across Load (On Board)

11.5.1 Output: 5 V / 5 A

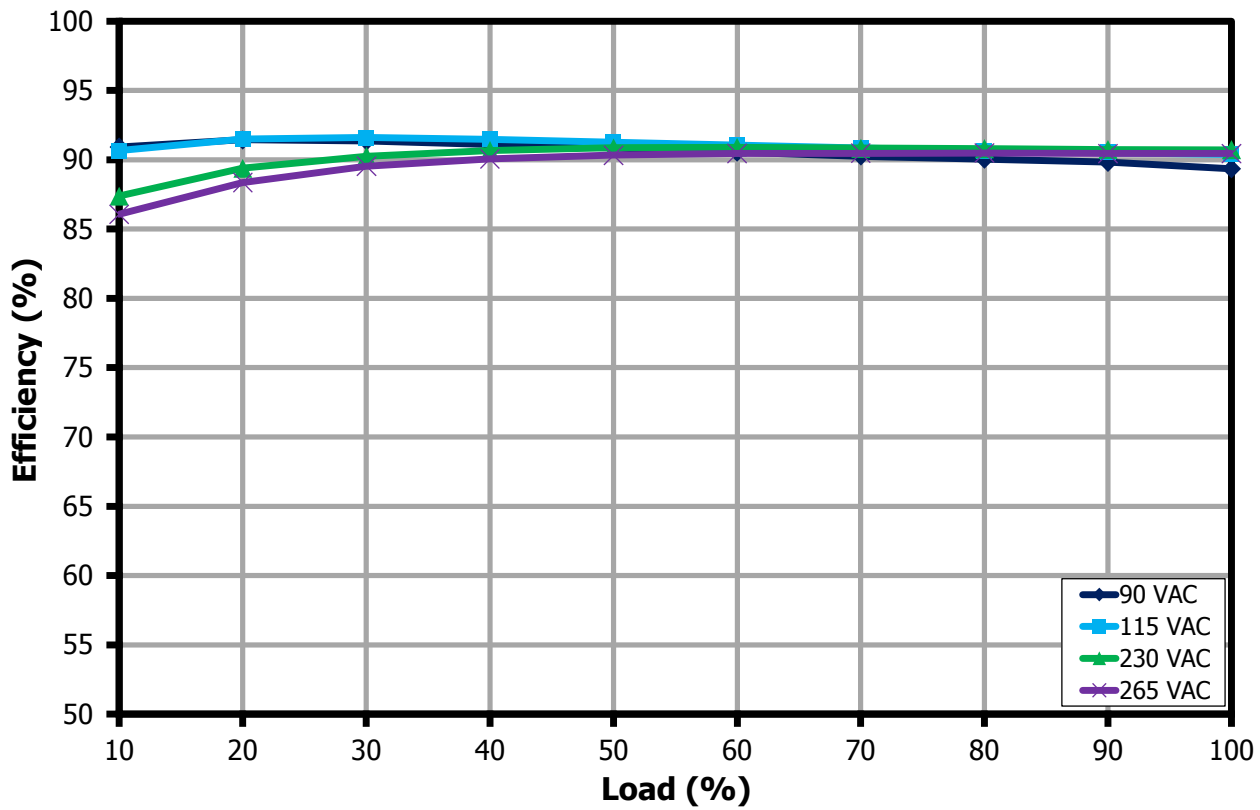


Figure 17 – Efficiency vs. Load for 5 V Output, Room Temperature.

11.5.2 Output: 9 V / 5 A

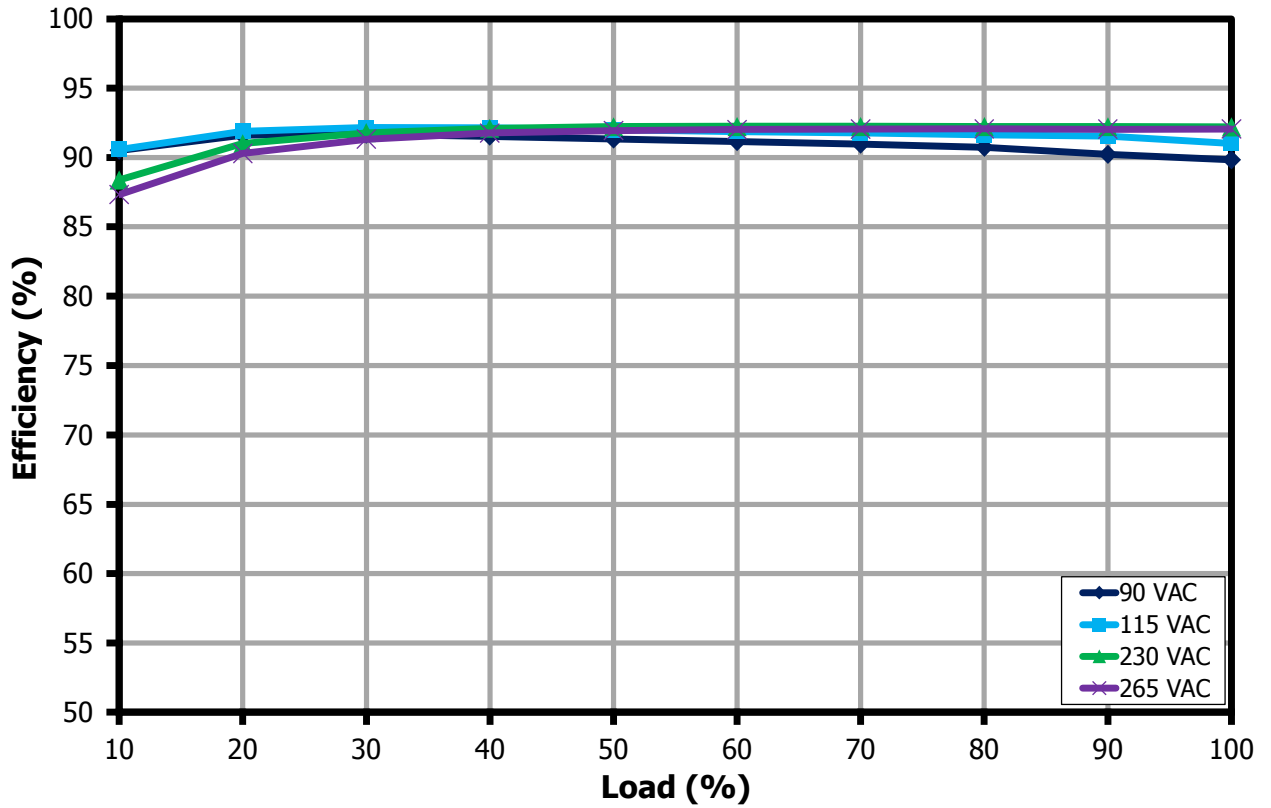


Figure 18 – Efficiency vs. Load for 9 V Output, Room Temperature.



11.5.3 Output: 15 V / 3 A

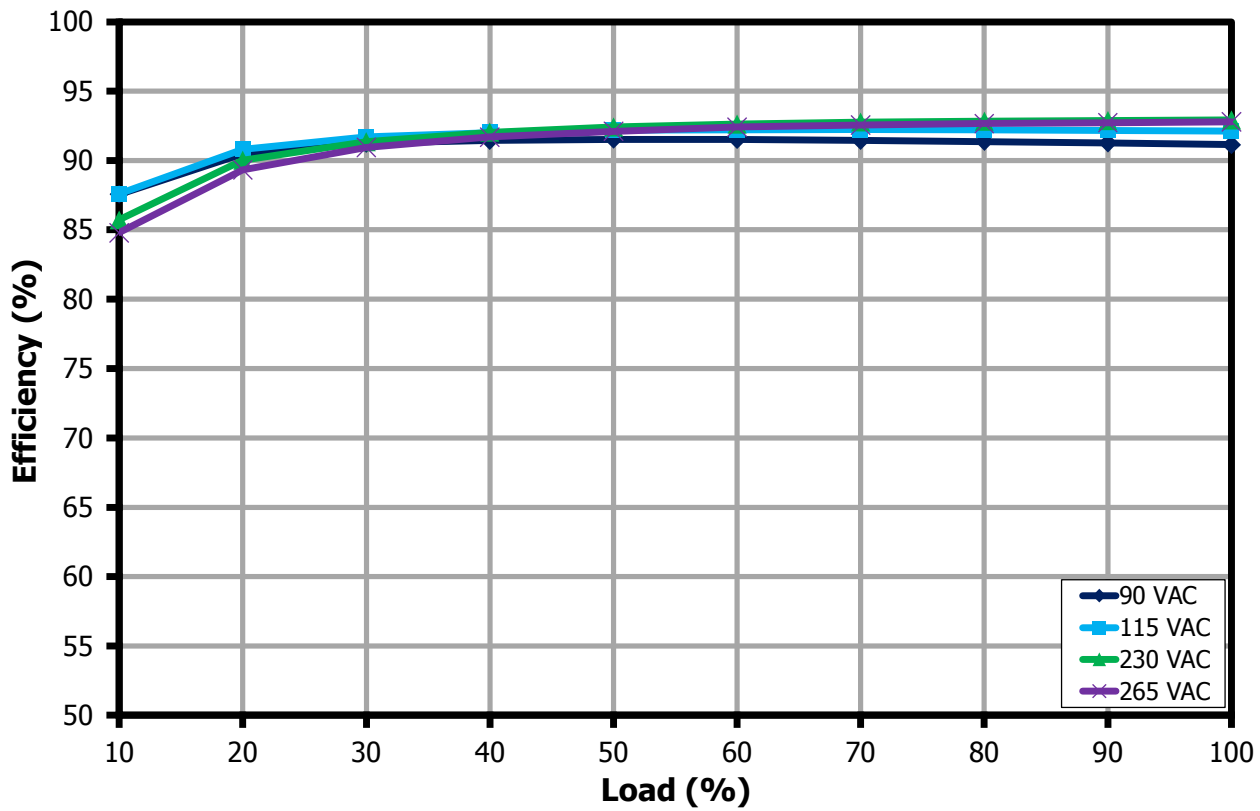


Figure 19 – Efficiency vs. Load for 15 V Output, Room Temperature.

11.5.4 Output: 20 V / 2.25 A

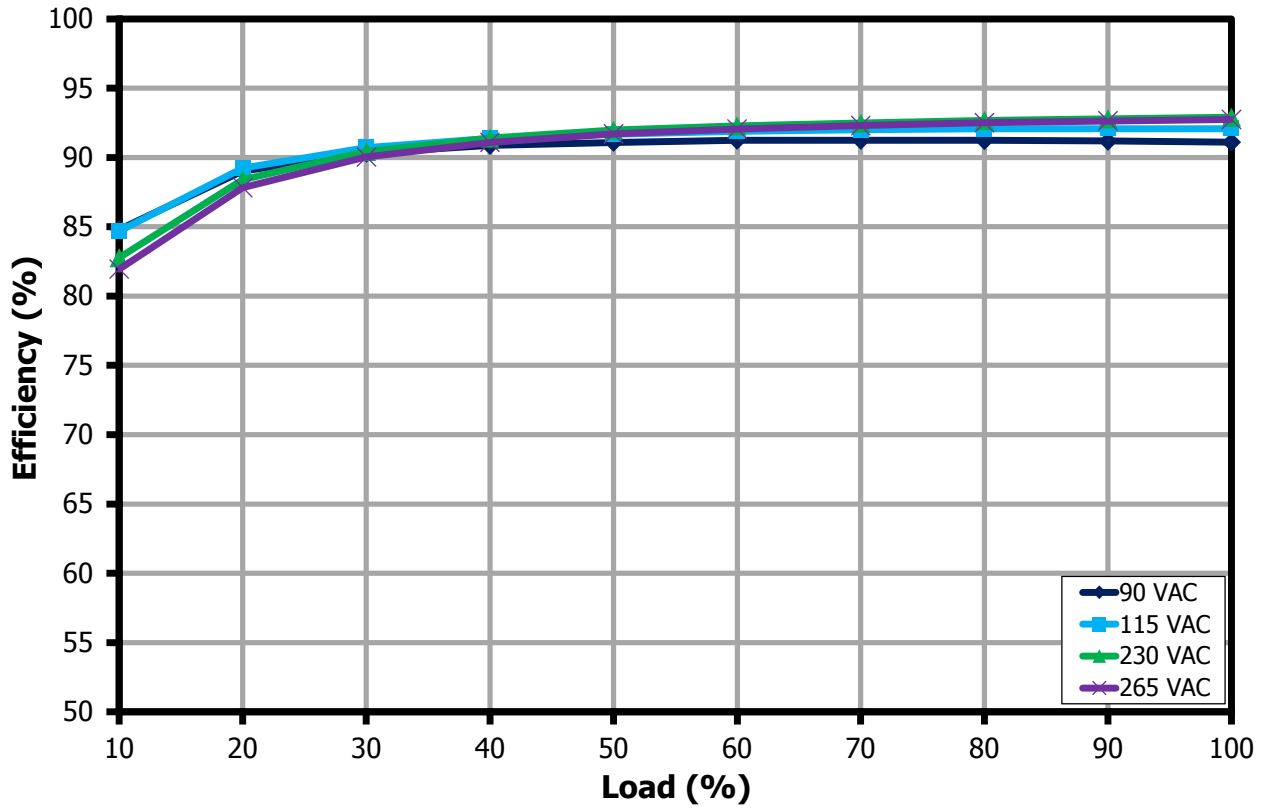


Figure 20 – Efficiency vs. Load for 20 V Output, Room Temperature.



11.6 Load Regulation (On Board)

For all Fixed PDOs (5 V, 9 V, 15 V, 20 V), a cable drop compensation is applied after a successful USB PD Contract. CDC value is set to 300 mV nominal.

11.6.1 Output: 5 V / 5 A

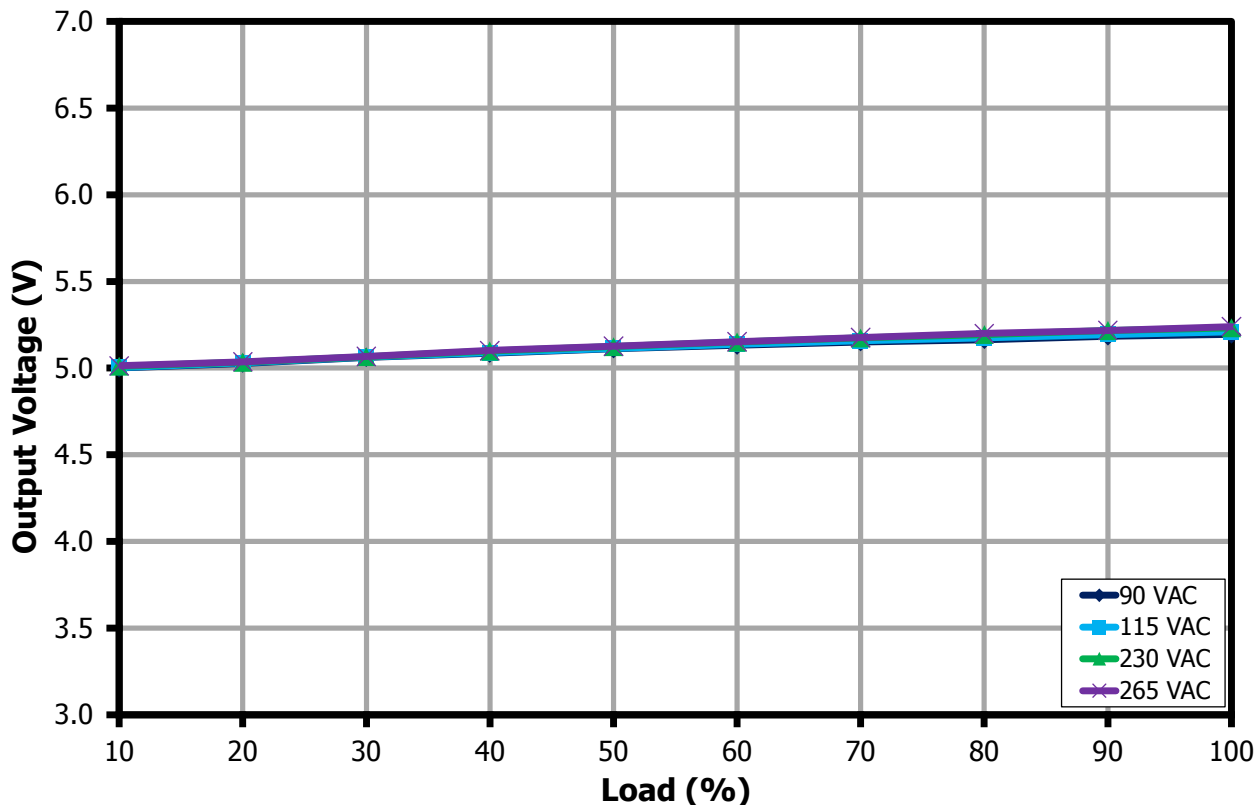


Figure 21 – Output Voltage vs. Output Load for 5 V Output, Room Temperature.

11.6.2 Output: 9 V / 5 A

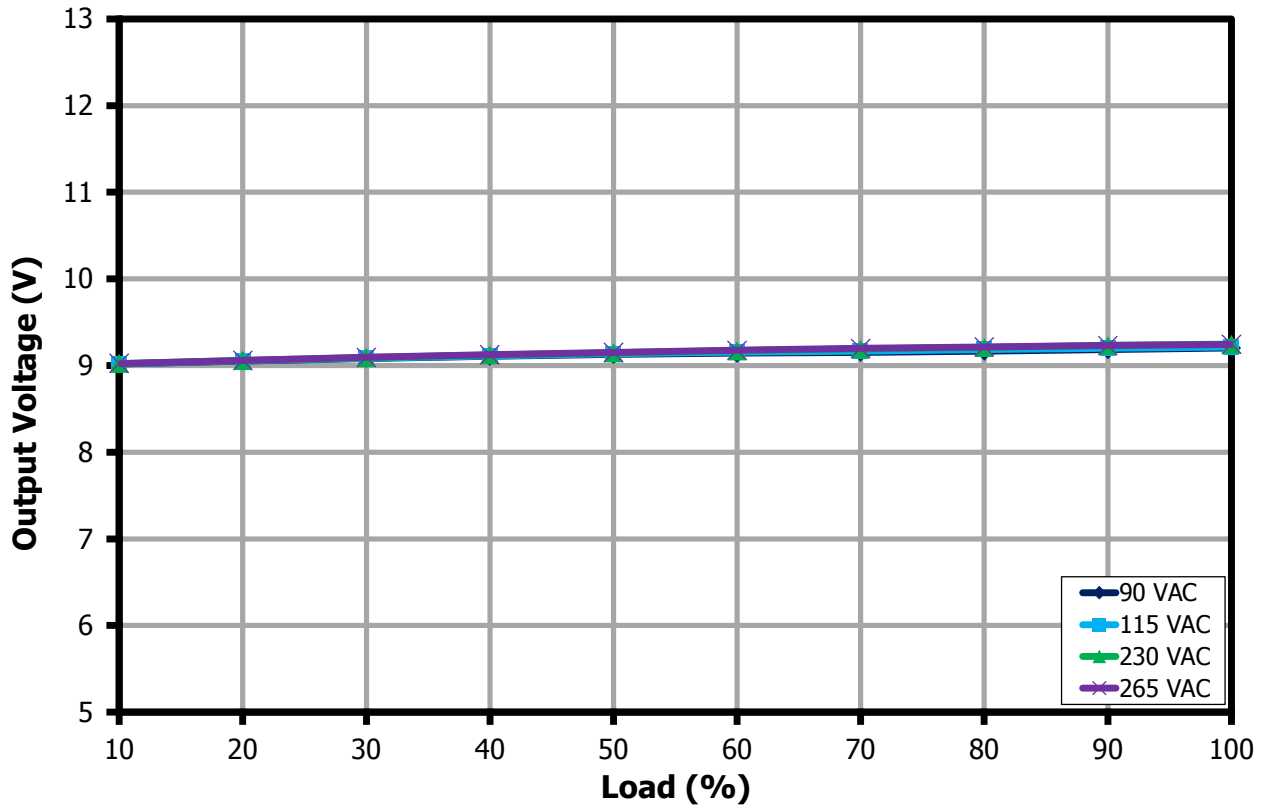


Figure 22 – Output Voltage vs. Output Load for 9 V Output, Room Temperature.



11.6.3 Output: 15 V / 3 A

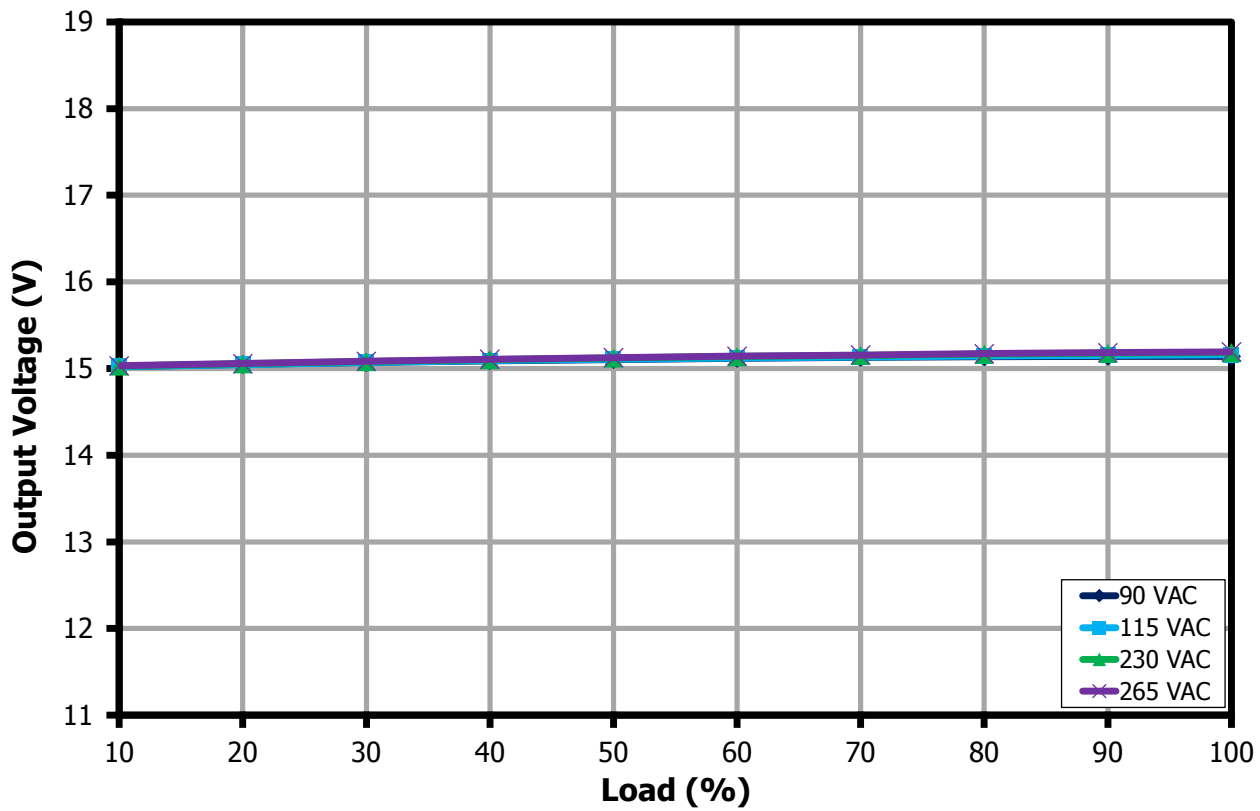


Figure 23 – Output Voltage vs. Output Load for 15 V Output, Room Temperature.

11.6.4 Output: 20 V / 2.25 A

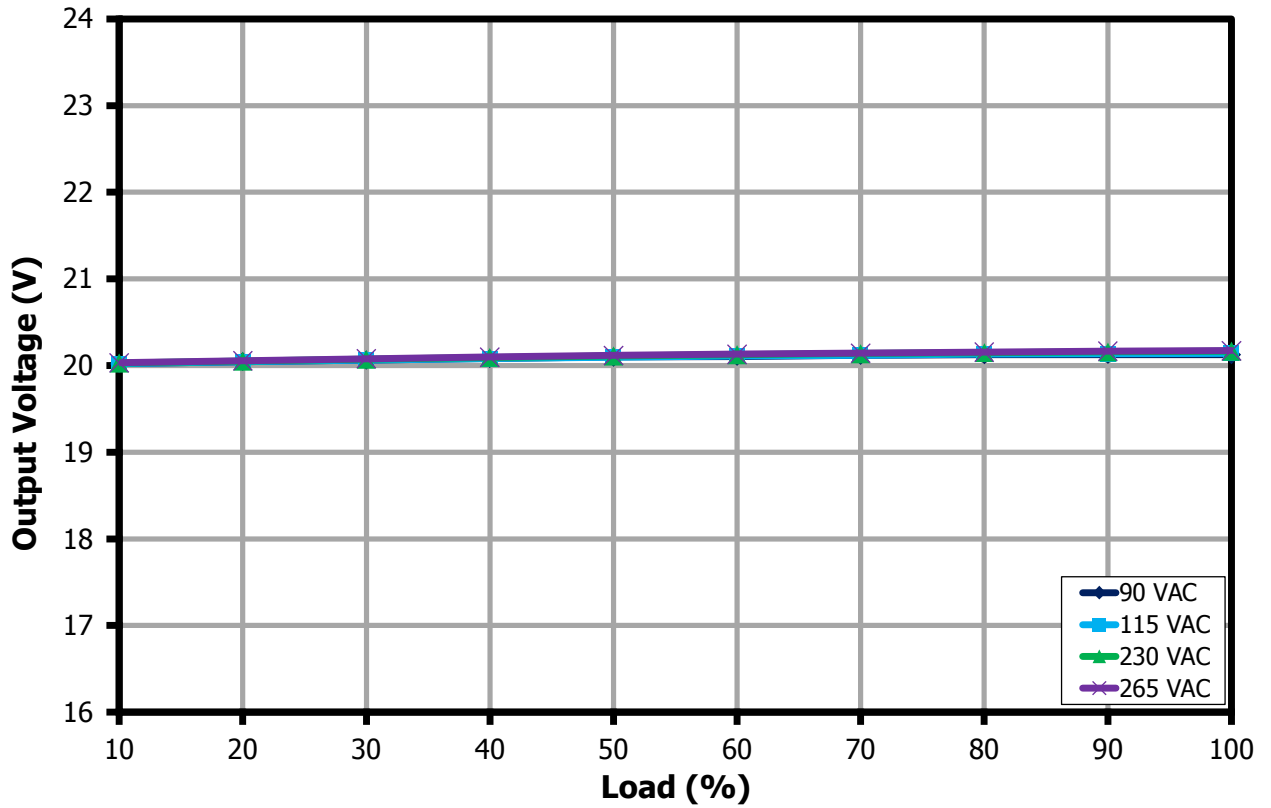


Figure 24 – Output Voltage vs. Output Load for 20 V Output, Room Temperature.



11.7 Line Regulation (On Board)

For all Fixed PDOs (5 V, 9 V, 15 V, 20 V), a cable drop compensation is applied after a successful USB PD Contract. CDC value is set to 300 mV nominal.

11.7.1 Output: 5 V / 5 A

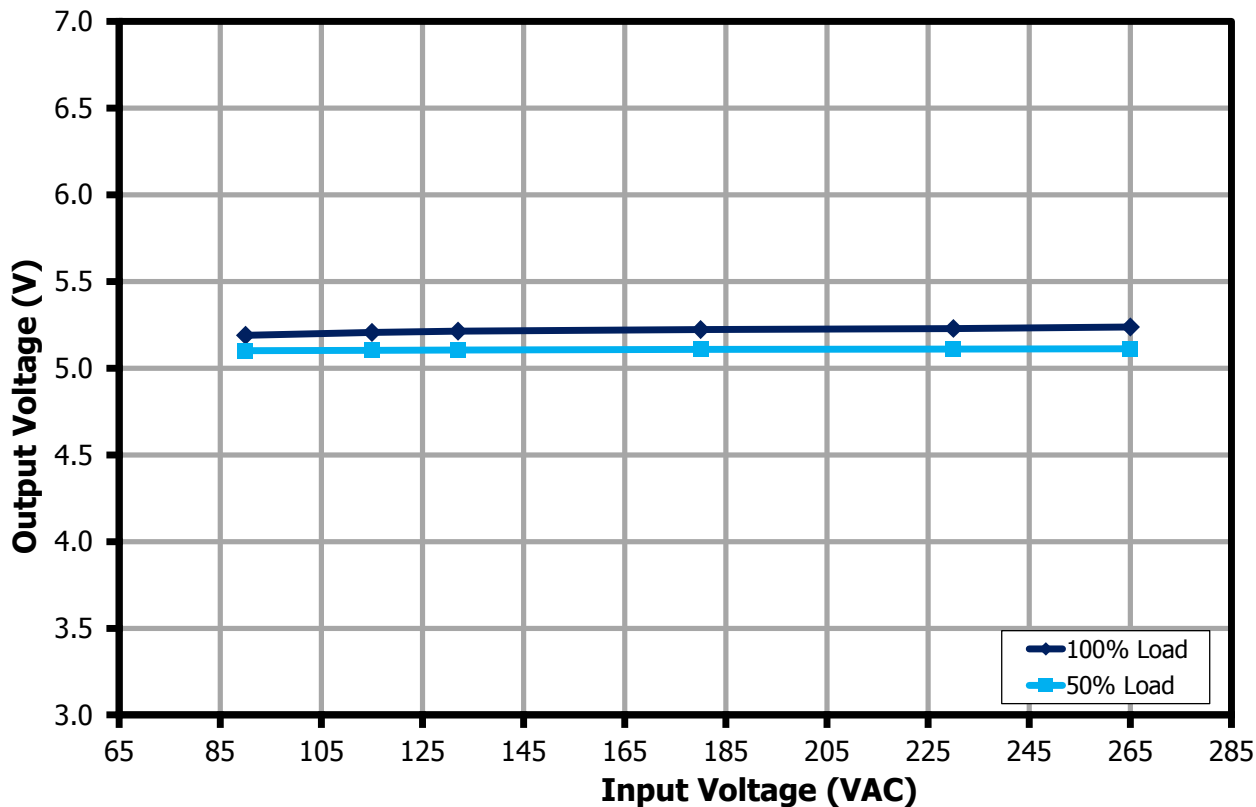


Figure 25 – Output Voltage vs. Input Line Voltage for 5 V Output, Room Temperature.

11.7.2 Output: 9 V / 5 A

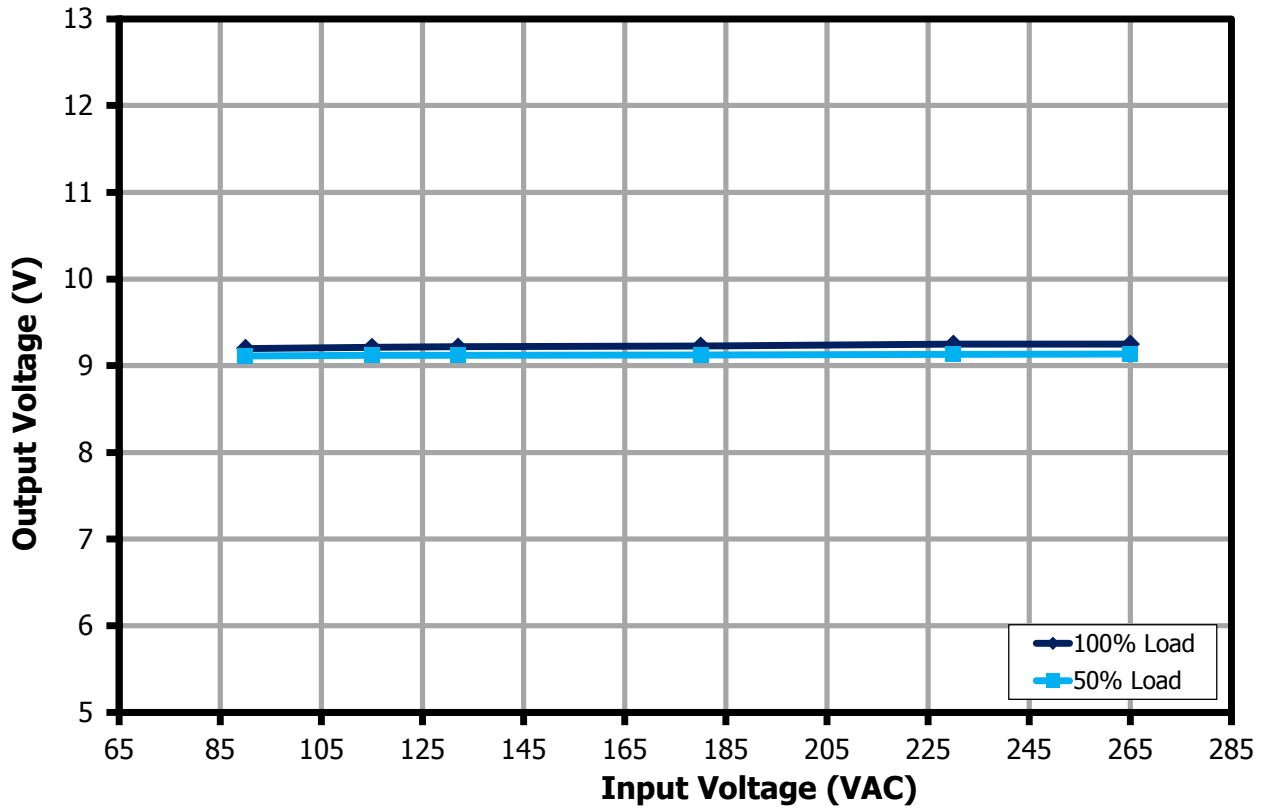


Figure 26 – Output Voltage vs. Input Line Voltage for 9 V Output, Room Temperature.



11.7.3 Output: 15 V / 3 A

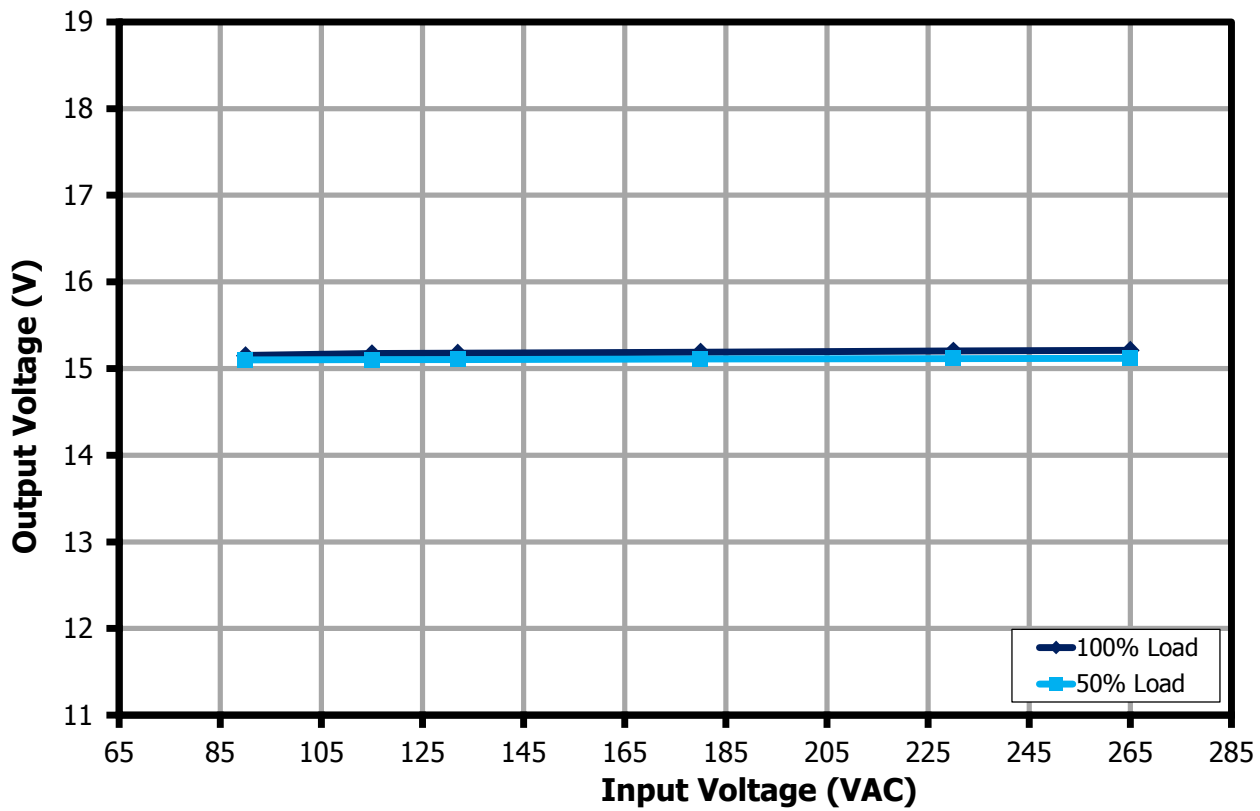


Figure 27 – Output Voltage vs. Input Line Voltage for 15 V Output, Room Temperature.

11.7.4 Output: 20 V / 2.25 A

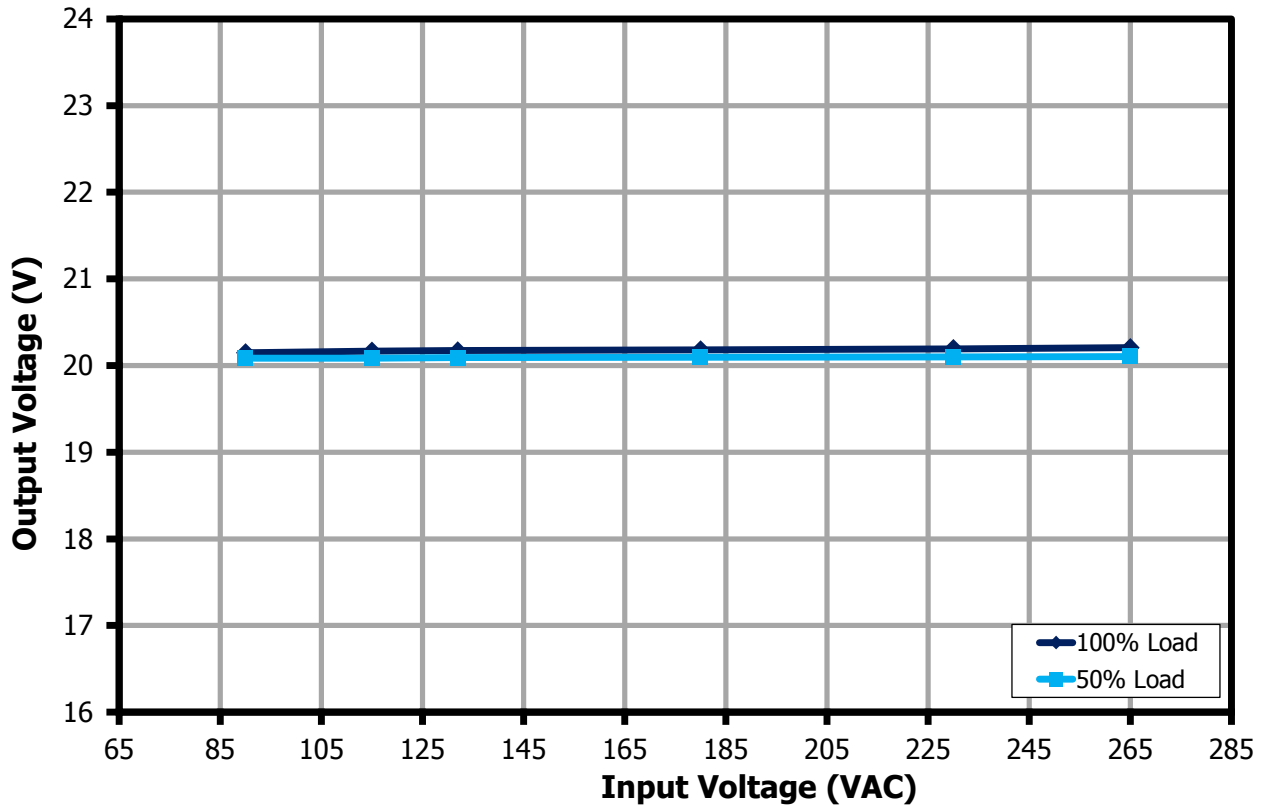


Figure 28 – Output Voltage vs. Input Line Voltage for 20 V Output, Room Temperature.



12 Thermal Performance

12.1 Thermal Performance in Open Case, Room Temperature

Note: Measurements taken after 1-hour soak.

12.1.1 Output: 5 V / 5 A (90 VAC)



Figure 29 – Top Thermal Image, $T_{AMB} = 28.4$ °C.
 Bx1: Transformer, T1 = 64.8 °C.
 Bx2: Thermistor, RT1 = 66.6 °C.
 Bx3: CMC 1, L1 = 52.6 °C.
 Bx4: CMC 2, L2 = 54.1 °C.

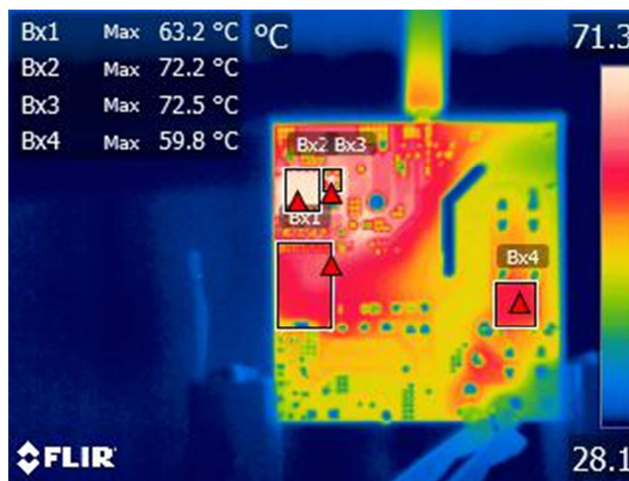


Figure 30 – Bottom Thermal Image, $T_{AMB} = 28.8$ °C.
 Bx1: InnoSwitch3-PD, U1 = 63.2 °C.
 Bx2: SR FET, Q2 = 72.2 °C.
 Bx3: SR FET Snubber, R10 = 72.5 °C.
 Bx4: Bridge Rectifier, BR1 = 59.8 °C.

12.1.2 Output: 5 V / 5 A (265 VAC)



Figure 31 – Top Thermal Image, $T_{AMB} = 25.6$ °C.
 Bx1: Transformer, $T_1 = 66.0$ °C.
 Bx2: Thermistor, $RT1 = 48.5$ °C.
 Bx3: CMC 1, $L1 = 40.5$ °C.
 Bx4: CMC 2, $L2 = 43.3$ °C.

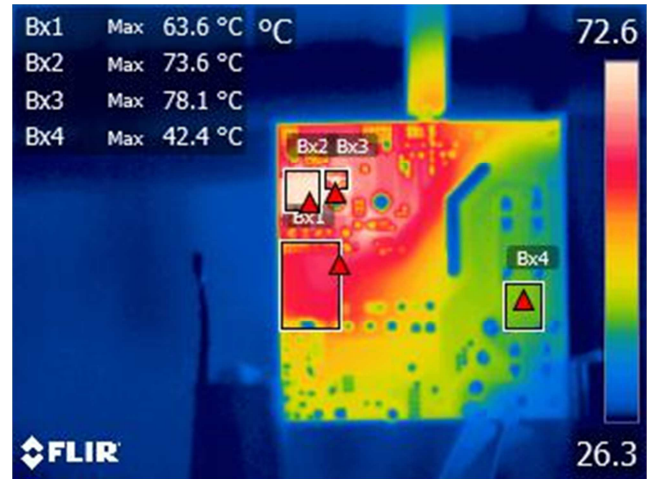


Figure 32 – Bottom Thermal Image, $T_{AMB} = 25.1$ °C.
 Bx1: InnoSwitch3-PD, $U1 = 63.6$ °C.
 Bx2: SR FET, $Q2 = 73.6$ °C.
 Bx3: SR FET Snubber, $R10 = 78.1$ °C.
 Bx4: Bridge Rectifier, $BR1 = 42.4$ °C.

12.1.3 Output: 9 V / 5 A (90 VAC)

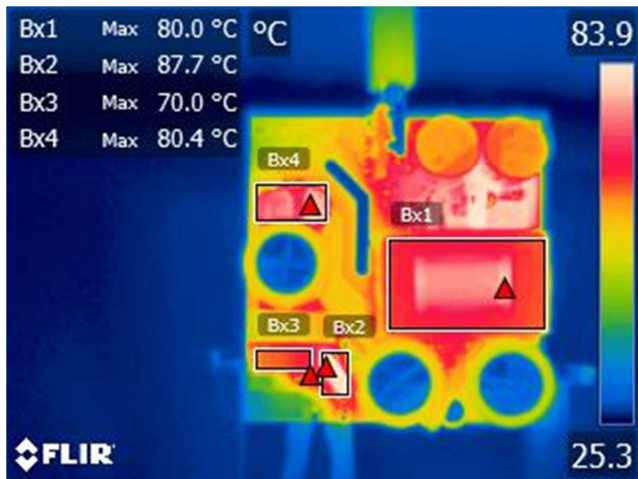


Figure 33 – Top Thermal Image, $T_{AMB} = 27.0$ °C.
 Bx1: Transformer, $T_1 = 80.0$ °C.
 Bx2: Thermistor, $RT_1 = 87.7$ °C.
 Bx3: CMC 1, $L_1 = 70.0$ °C.
 Bx4: CMC 2, $L_2 = 80.4$ °C.

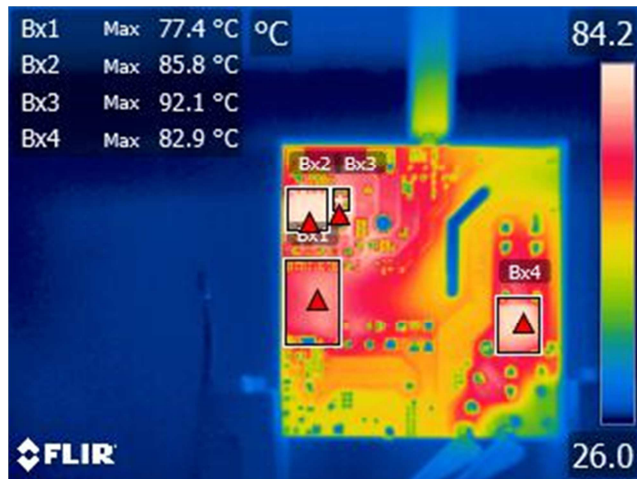


Figure 34 – Bottom Thermal Image, $T_{AMB} = 26.7$ °C.
 Bx1: InnoSwitch3-PD, $U_1 = 77.4$ °C.
 Bx2: SR FET, $Q_2 = 85.8$ °C.
 Bx3: SR FET Snubber, $R_{10} = 92.1$ °C.
 Bx4: Bridge Rectifier, $BR_1 = 82.9$ °C.

12.1.4 Output: 9 V / 5 A (265 VAC)

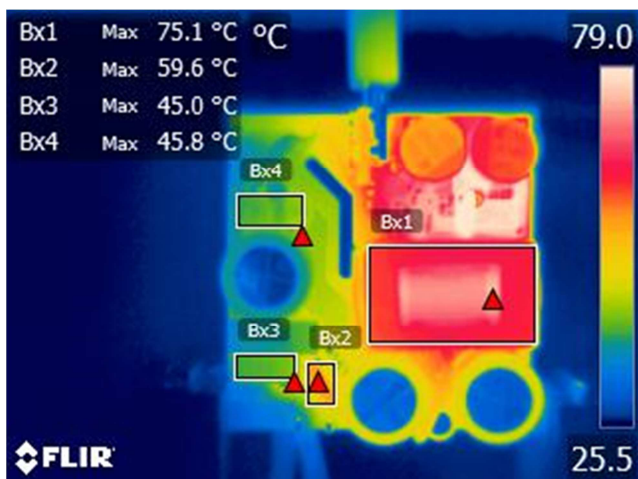


Figure 35 – Top Thermal Image, $T_{AMB} = 26.9$ °C.
 Bx1: Transformer, $T_1 = 75.1$ °C.
 Bx2: Thermistor, $RT_1 = 59.6$ °C.
 Bx3: CMC 1, $L_1 = 45.0$ °C.
 Bx4: CMC 2, $L_2 = 45.8$ °C.

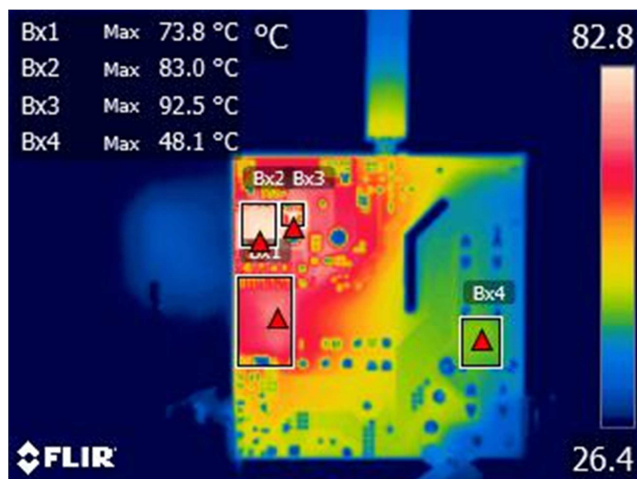


Figure 36 – Bottom Thermal Image, $T_{AMB} = 26.5$ °C.
 Bx1: InnoSwitch3-PD, $U_1 = 73.8$ °C.
 Bx2: SR FET, $Q_2 = 83.0$ °C.
 Bx3: SR FET Snubber, $R_{10} = 92.5$ °C.
 Bx4: Bridge Rectifier, $BR_1 = 48.1$ °C.

12.1.5 Output: 15 V / 3 A (90 VAC)

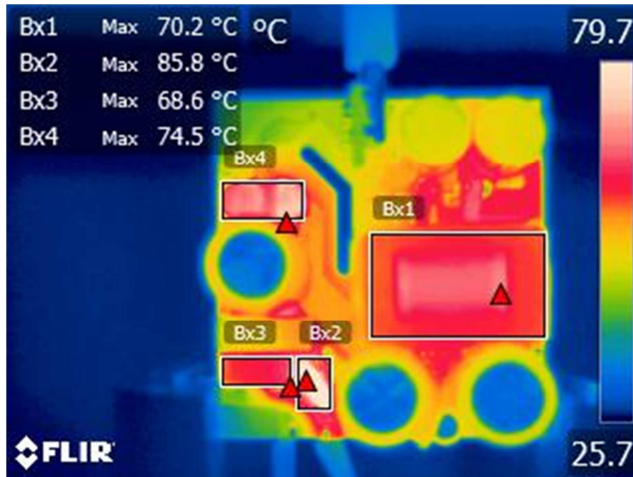


Figure 37 – Top Thermal Image, $T_{AMB} = 24.9$ °C.
 Bx1: Transformer, $T_1 = 70.2$ °C.
 Bx2: Thermistor, $RT_1 = 85.8$ °C.
 Bx3: CMC 1, $L_1 = 68.6$ °C.
 Bx4: CMC 2, $L_2 = 74.5$ °C.

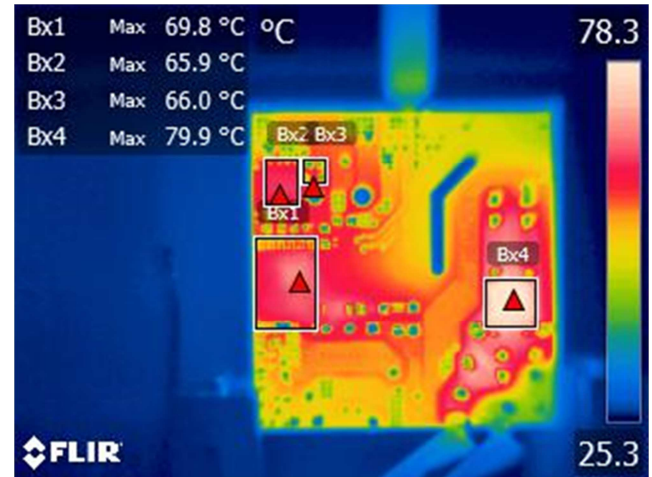


Figure 38 – Bottom Thermal Image, $T_{AMB} = 25.2$ °C.
 Bx1: InnoSwitch3-PD, $U_1 = 69.8$ °C.
 Bx2: SR FET, $Q_2 = 65.9$ °C.
 Bx3: SR FET Snubber, $R_{10} = 66.0$ °C.
 Bx4: Bridge Rectifier, $BR_1 = 79.9$ °C.

12.1.6 Output: 15 V / 3 A (265 VAC)

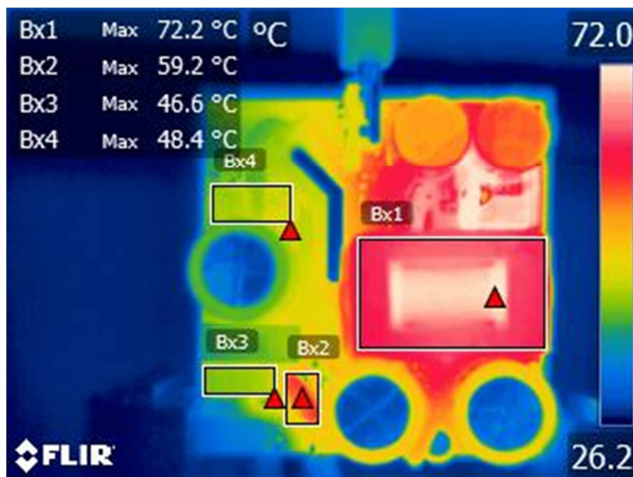


Figure 39 – Top Thermal Image, $T_{AMB} = 25.0$ °C.
 Bx1: Transformer, $T_1 = 72.2$ °C.
 Bx2: Thermistor, $RT_1 = 59.2$ °C.
 Bx3: CMC 1, $L_1 = 46.6$ °C.
 Bx4: CMC 2, $L_2 = 48.4$ °C.

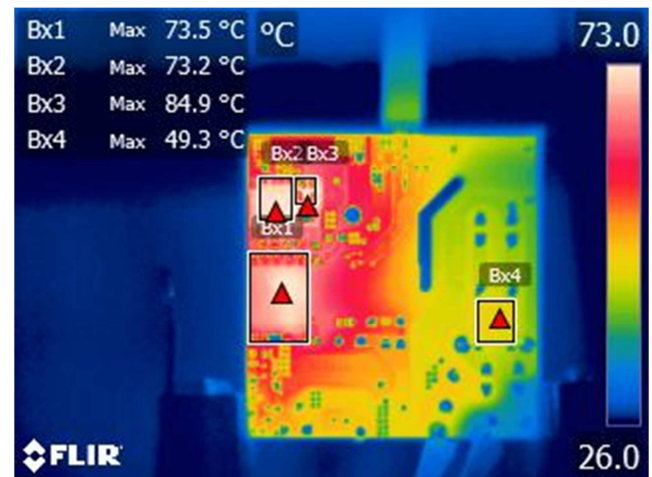


Figure 40 – Bottom Thermal Image, $T_{AMB} = 25.2$ °C.
 Bx1: InnoSwitch3-PD, $U_1 = 73.5$ °C.
 Bx2: SR FET, $Q_2 = 73.2$ °C.
 Bx3: SR FET Snubber, $R_{10} = 84.9$ °C.
 Bx4: Bridge Rectifier, $BR_1 = 49.3$ °C.

12.1.7 Output: 20 V / 2.25 A (90 VAC)

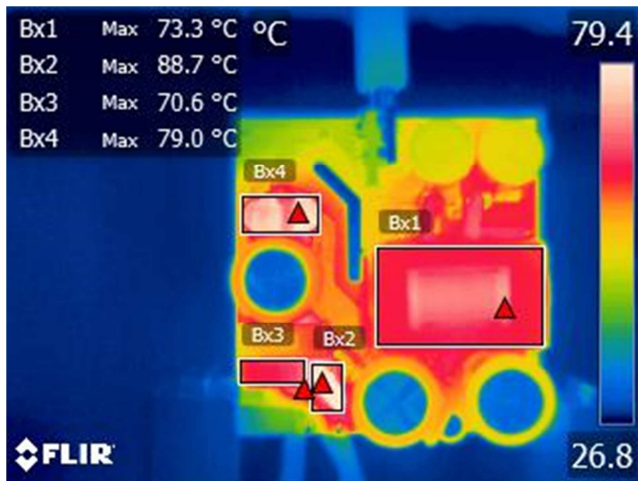


Figure 41 – Top Thermal Image, $T_{AMB} = 26.5\text{ }^{\circ}\text{C}$.
 Bx1: Transformer, $T_1 = 73.3\text{ }^{\circ}\text{C}$.
 Bx2: Thermistor, $RT_1 = 88.7\text{ }^{\circ}\text{C}$.
 Bx3: CMC 1, $L_1 = 70.6\text{ }^{\circ}\text{C}$.
 Bx4: CMC 2, $L_2 = 79.0\text{ }^{\circ}\text{C}$.

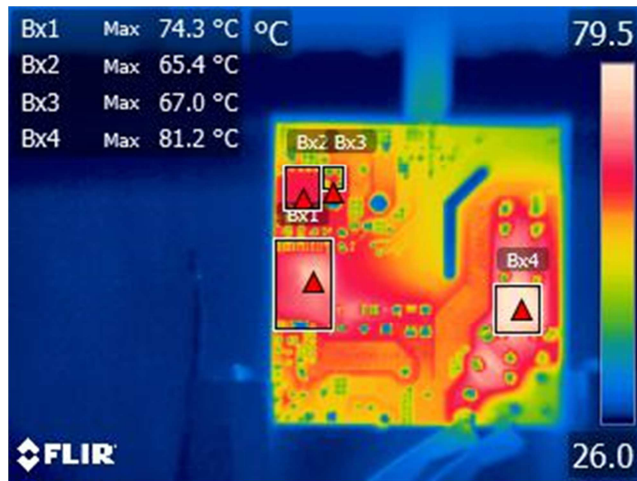


Figure 42 – Bottom Thermal Image, $T_{AMB} = 26.0\text{ }^{\circ}\text{C}$.
 Bx1: InnoSwitch3-PD, $U_1 = 74.3\text{ }^{\circ}\text{C}$.
 Bx2: SR FET, $Q_2 = 65.4\text{ }^{\circ}\text{C}$.
 Bx3: SR FET Snubber, $R_{10} = 67.0\text{ }^{\circ}\text{C}$.
 Bx4: Bridge Rectifier, $BR_1 = 81.2\text{ }^{\circ}\text{C}$.

12.1.8 Output: 20 V / 2.25 A (265 VAC)

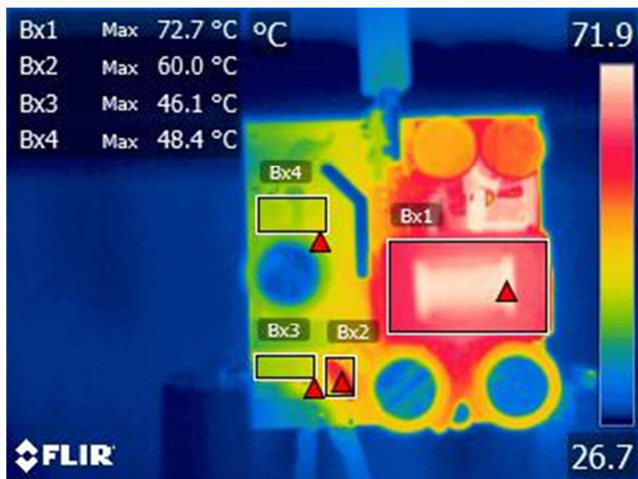


Figure 43 – Top Thermal Image, $T_{AMB} = 25.3\text{ }^{\circ}\text{C}$.
 Bx1: Transformer, $T_1 = 72.7\text{ }^{\circ}\text{C}$.
 Bx2: Thermistor, $RT_1 = 60.0\text{ }^{\circ}\text{C}$.
 Bx3: CMC 1, $L_1 = 46.1\text{ }^{\circ}\text{C}$.
 Bx4: CMC 2, $L_2 = 48.4\text{ }^{\circ}\text{C}$.

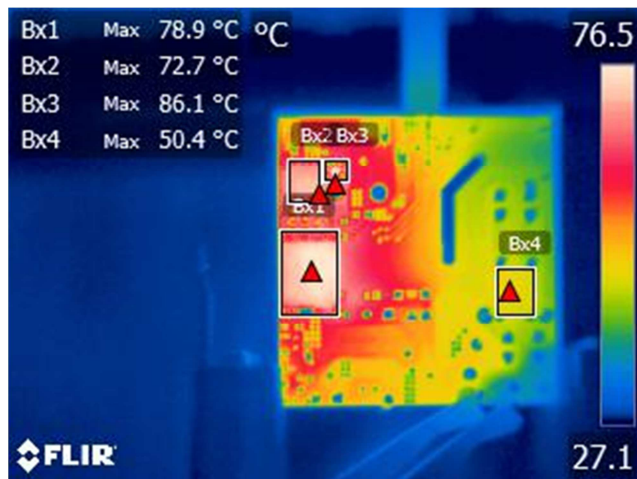


Figure 44 – Bottom Thermal Image, $T_{AMB} = 25.4\text{ }^{\circ}\text{C}$.
 Bx1: InnoSwitch3-PD, $U_1 = 78.9\text{ }^{\circ}\text{C}$.
 Bx2: SR FET, $Q_2 = 72.7\text{ }^{\circ}\text{C}$.
 Bx3: SR FET Snubber, $R_{10} = 86.1\text{ }^{\circ}\text{C}$.
 Bx4: Bridge Rectifier, $BR_1 = 50.4\text{ }^{\circ}\text{C}$.

12.2 Thermal Performance in Open Case, 45 °C Ambient

Note: Measurements taken using Type-T thermocouple and with the board inside a thermal chamber.

12.2.1 Components Temperature Summary

Condition	Component	Temperature (°C) After 1.5 Hour Soak			
		5 V / 5 A		9 V / 5 A	
		90 VAC	265 VAC	90 VAC	265 VAC
Open Frame Unit, 45 °C Ambient	RT1	70.7	60.2	87.1	69.8
	BR1	71.1	58.4	92.0	65.4
	INN3879C	70.6	72.7	89.4	85.5
	SRFET	78.5	80.1	95.2	95.0
	T1-core	67.2	68.9	80.0	82.2
	T1-wire	74.0	75.1	90.3	90.1
	Primary Clamp	69.9	69.0	86.7	80.2
	Bus Switch	75.5	75.2	88.2	86.5
Ambient	45.0	45.2	45.7	46.1	

Condition	Component	Temperature (°C) After 1.5 Hour Soak			
		15 V / 3 A		20 V / 2.25 A	
		90 VAC	265 VAC	90 VAC	265 VAC
Open Frame Unit, 45 °C Ambient	RT1	83.9	66.3	85.7	68.1
	BR1	84.1	61.7	89.6	65.0
	INN3879C	74.7	76.8	82.4	82.9
	SRFET	70.4	74.1	78.6	79.5
	T1-core	71.2	71.8	76.0	75.4
	T1-wire	77.5	77.3	82.8	81.0
	Primary Clamp	74.5	72.2	81.4	78.0
	Bus Switch	64.8	65.1	72.6	69.7
Ambient	45.7	45.2	45.2	45.1	

12.2.2 Output: 5 V / 5 A (90 VAC)

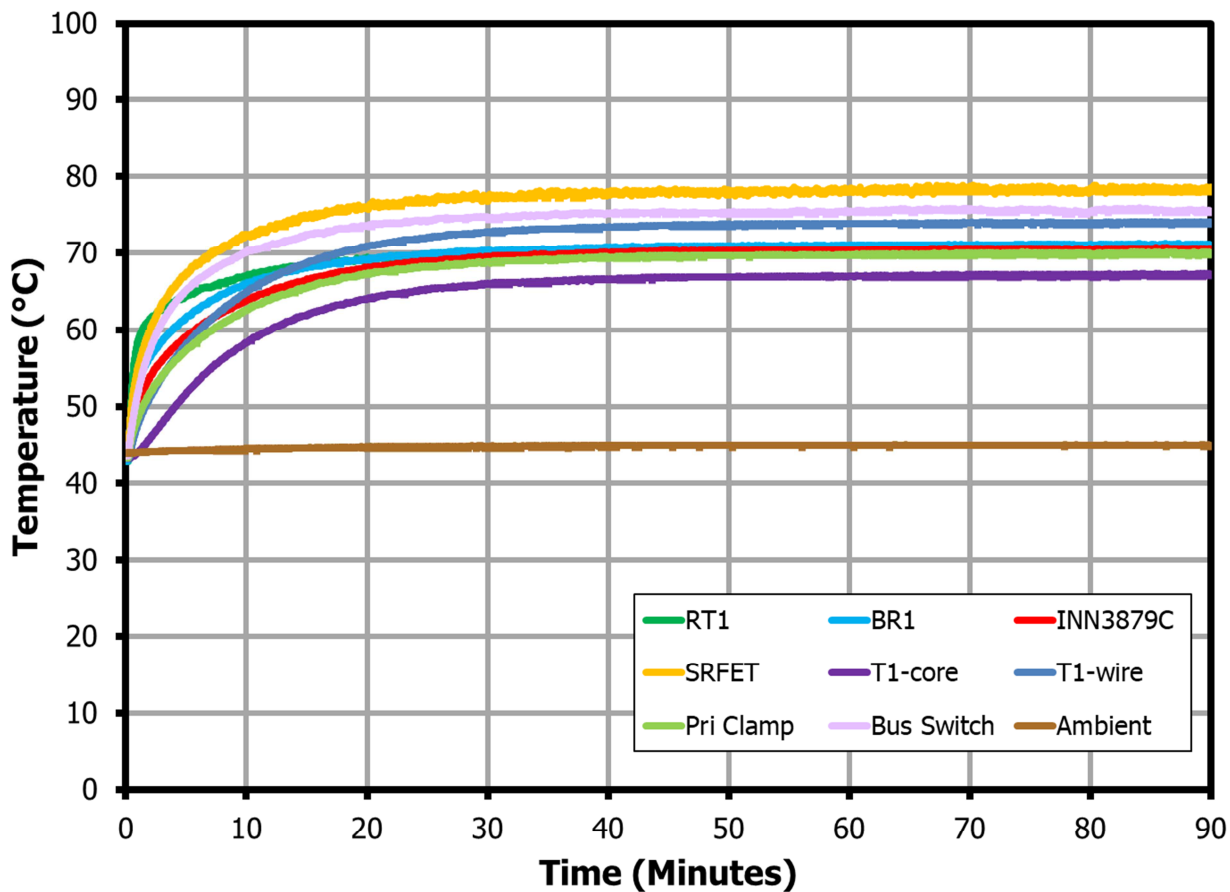


Figure 45 – Enclosed Unit Thermal Performance at 5 V / 5 A Output, 90 VAC, 45 °C Ambient.

12.2.3 Output: 5 V / 5 A (265 VAC)

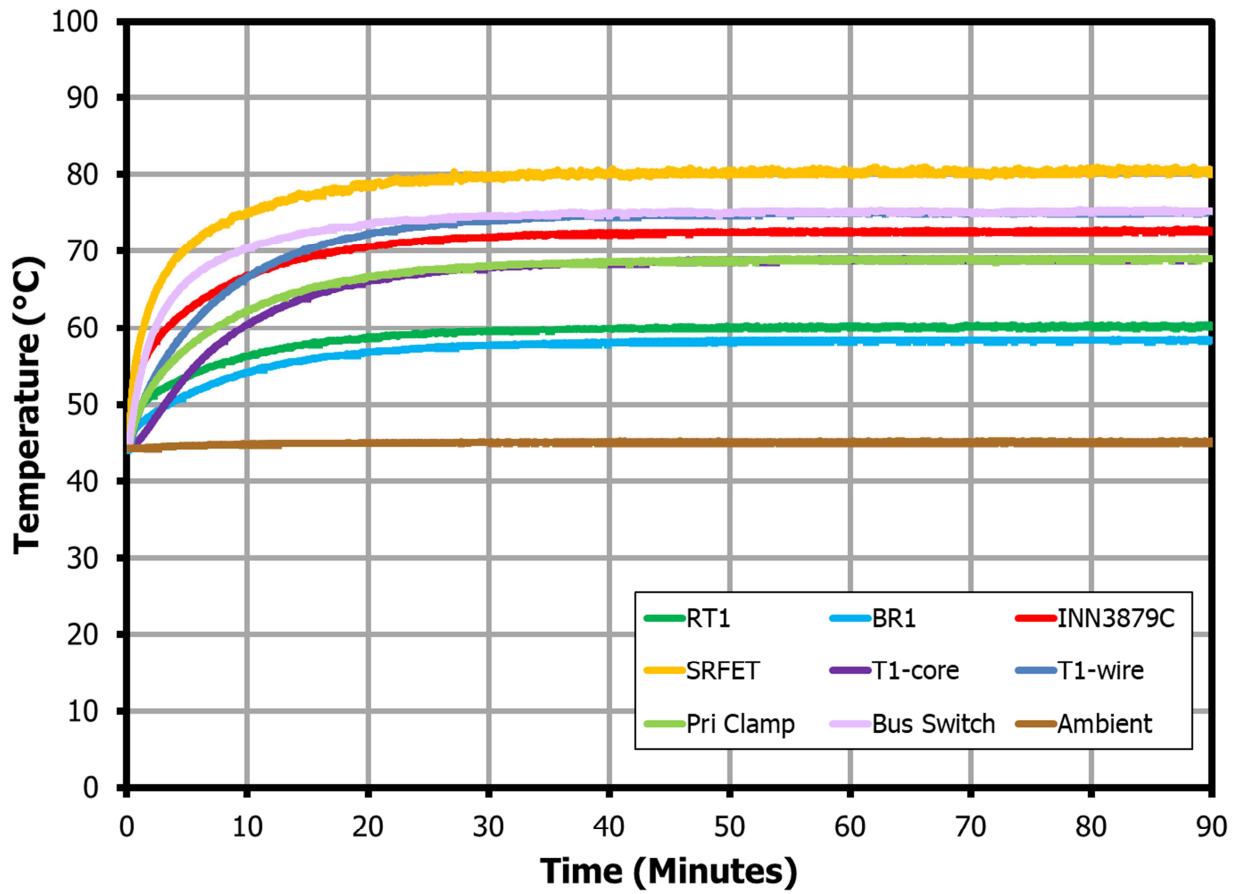


Figure 46 – Enclosed Unit Thermal Performance at 5 V / 5 A Output, 265 VAC, 45 °C Ambient.



12.2.4 Output: 9 V / 5 A (90 VAC)

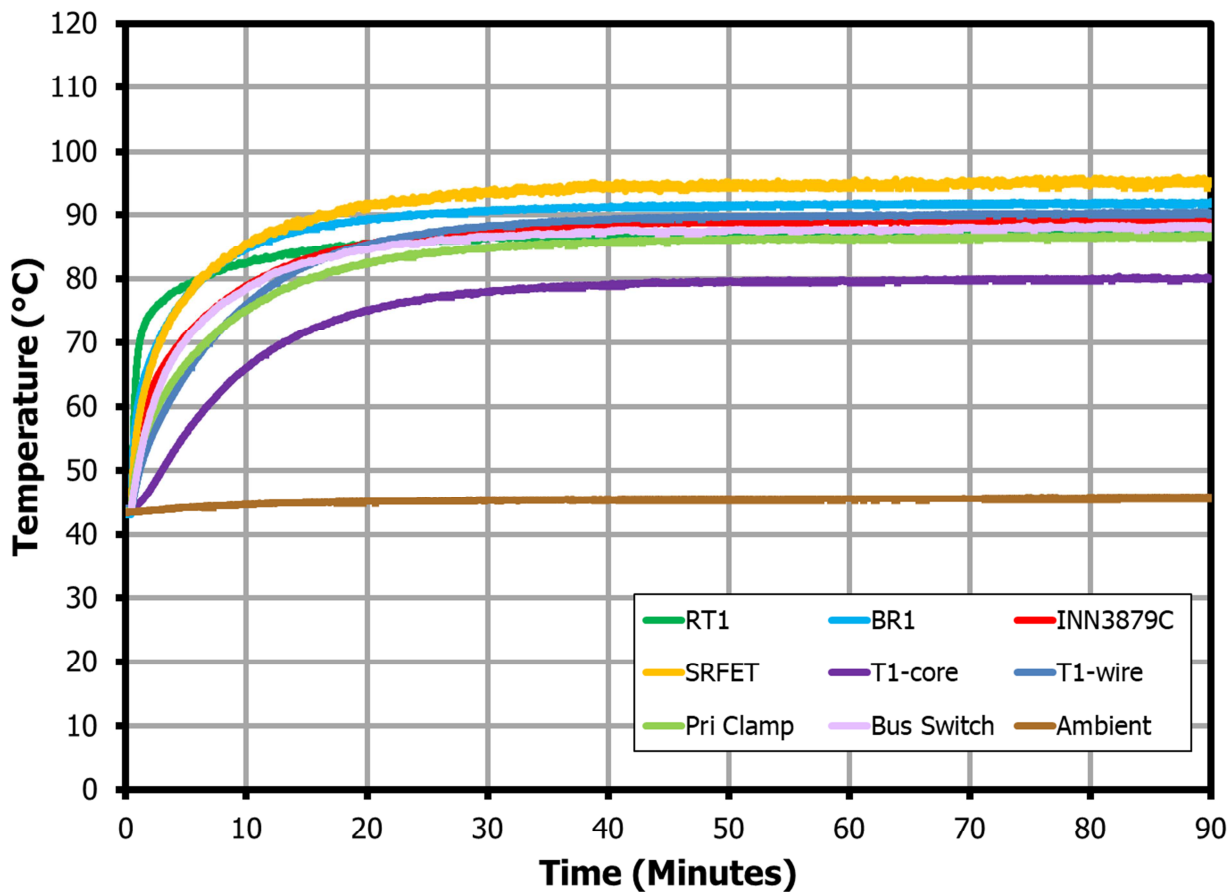


Figure 47 – Enclosed Unit Thermal Performance at 9 V / 5 A Output, 90 VAC, 45 °C Ambient.

12.2.5 Output: 9 V / 5 A (265 VAC)

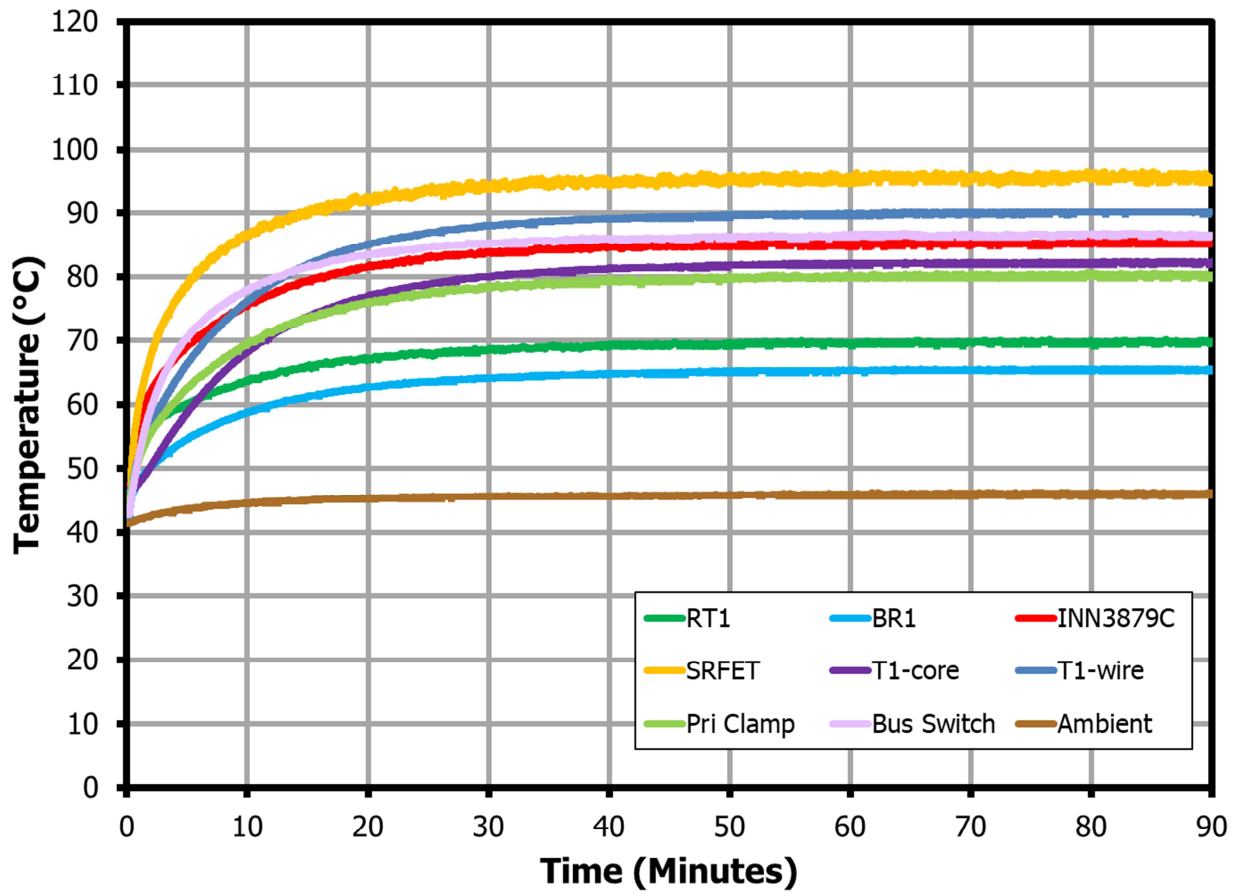


Figure 48 – Enclosed Unit Thermal Performance at 9 V / 5 A Output, 265 VAC, 45 °C Ambient.



12.2.6 Output: 15 V / 3 A (90 VAC)

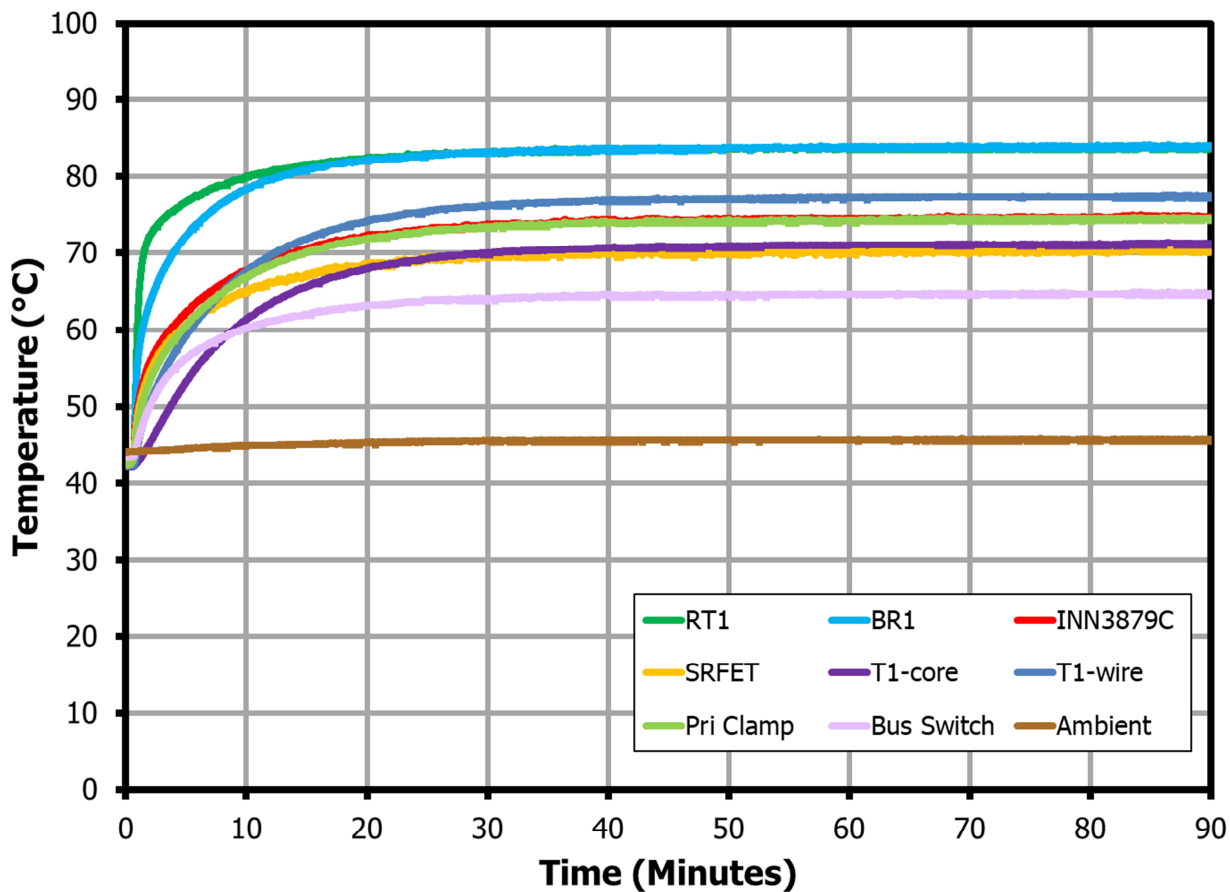


Figure 49 – Enclosed Unit Thermal Performance at 15 V / 3 A Output, 90 VAC, 45 °C Ambient.

12.2.7 Output: 15 V / 3 A (265 VAC)

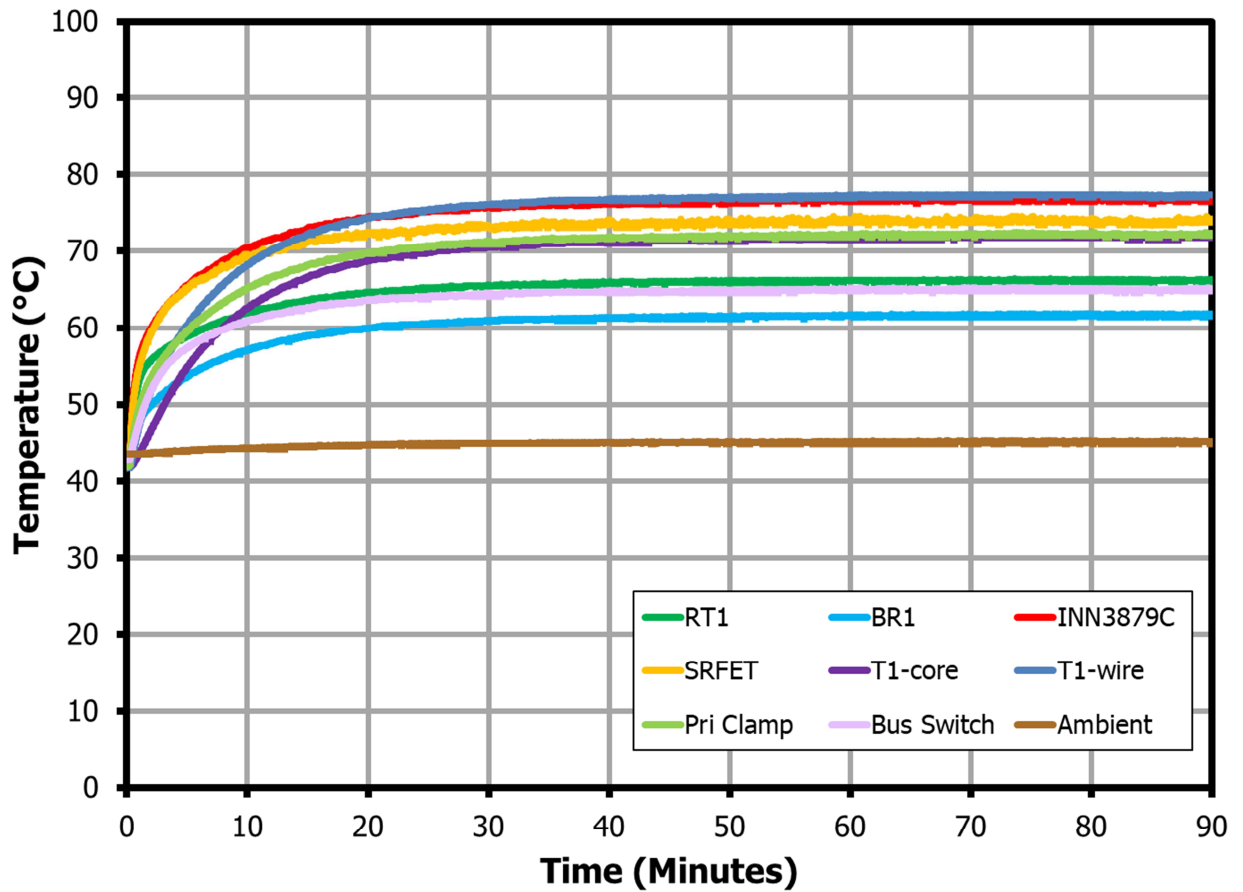


Figure 50 – Enclosed Unit Thermal Performance at 15 V / 3 A Output, 265 VAC, 45 °C Ambient.



12.2.8 Output: 20 V / 2.25 A (90 VAC)

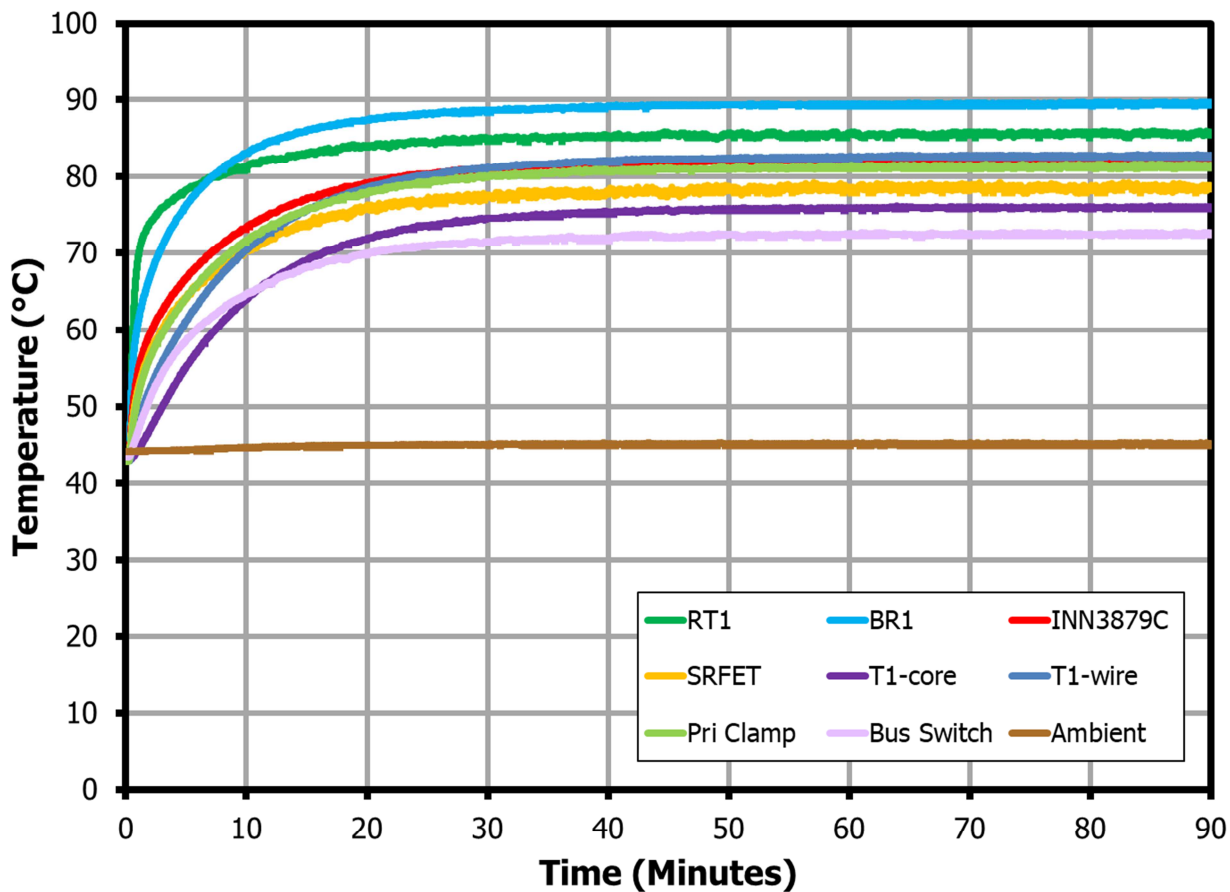


Figure 51 – Enclosed Unit Thermal Performance at 20 V / 2.25 A Output, 90 VAC, 45 °C Ambient.

12.2.9 Output: 20 V / 2.25 A (265 VAC)

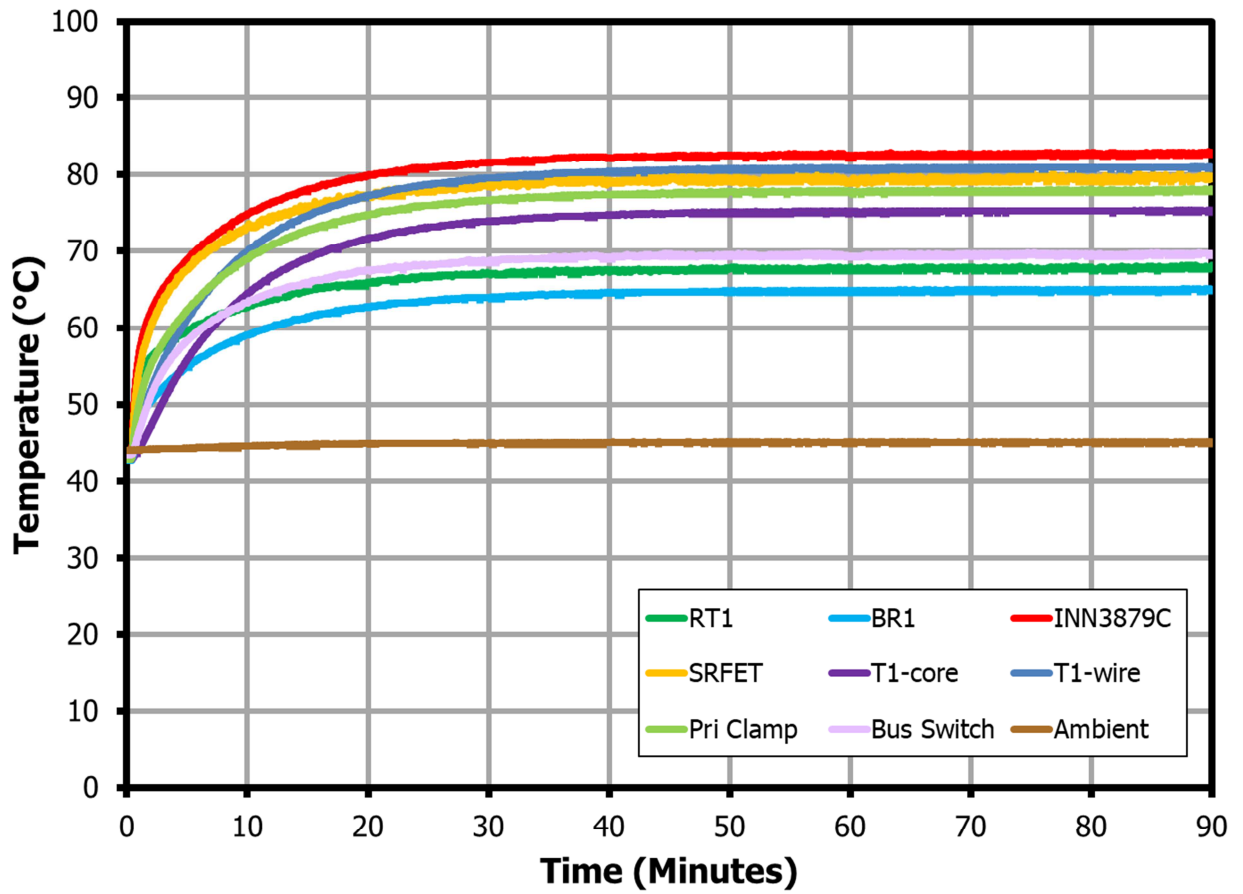


Figure 52 – Enclosed Unit Thermal Performance at 20 V / 2.25 A Output, 265 VAC, 45 °C Ambient.



13 Waveforms

Note: Waveforms taken at room temperature ambient (approximately 25 °C)

13.1 Start-up Waveforms

13.1.1 Output Voltage and Current

Output voltage was captured at the end of 100 mΩ cable. For all Fixed PDOs (5 V, 9 V, 15 V, 20 V), a cable drop compensation is applied after a successful USB PD Contract. CDC value is set to 300 mV nominal.

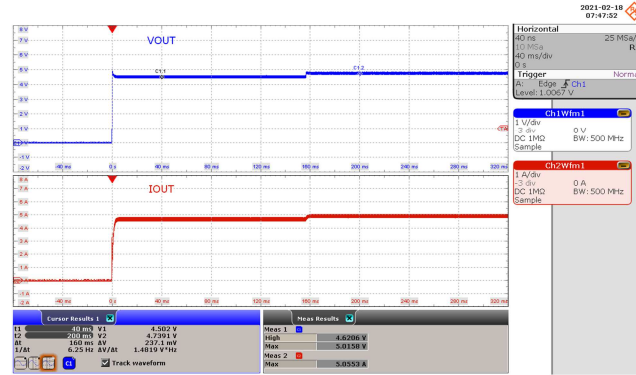
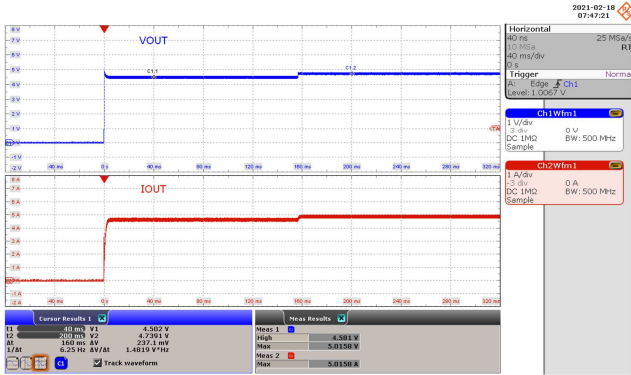


Figure 53 – Output Voltage and Current.
 90 VAC, 5.0 V, 5 A (CR Mode,
 930 mΩ at the End of 100 mΩ Cable).
 $V_{OUT} = 4.7391$ V Steady-State.
 CH1: V_{OUT} , 1 V / div.
 CH2: I_{LOAD} , 1 A / div.
 Time: 40 ms / div.

Figure 54 – Output Voltage and Current.
 265 VAC, 5.0 V, 5 A (CR Mode,
 930 mΩ at the End of 100 mΩ Cable).
 $V_{OUT} = 4.7391$ V Steady-State.
 CH1: V_{OUT} , 1 V / div.
 CH2: I_{LOAD} , 1 A / div.
 Time: 40 ms / div.

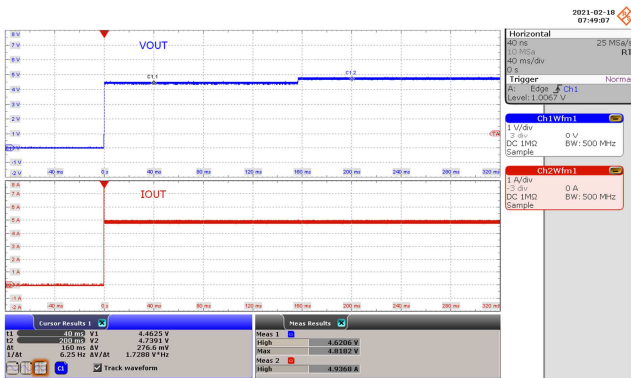


Figure 55 – Output Voltage and Current.
 90 VAC, 5.0 V, 5 A (CC Mode).
 $V_{OUT} = 4.7391$ V Steady-State.
 CH1: V_{OUT} , 1 V / div.
 CH2: I_{LOAD} , 1 A / div.
 Time: 40 ms / div.

Figure 56 – Output Voltage and Current.
 265 VAC, 5.0 V, 5 A (CC Mode).
 $V_{OUT} = 4.7787$ V Steady-State.
 CH1: V_{OUT} , 1 V / div.
 CH2: I_{LOAD} , 1 A / div.
 Time: 40 ms / div.

13.1.2 Primary Drain Voltage and Current

Primary Drain Voltage, Drain Current, and output voltage before the bus switch were captured. For all fixed PDOs (5 V, 9 V, 15 V, 20 V), a cable drop compensation is applied after a successful USB PD Contract. CDC value is set to 300 mV nominal.

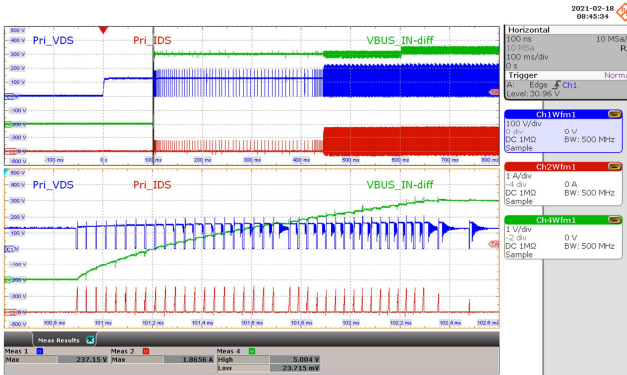


Figure 57 – Primary Drain Voltage and Current.
 90 VAC, 5.0 V, 5 A (CR Mode, 930 mΩ at the End of 100 mΩ Cable).
 $V_{DS_PRI} = 237$ V Maximum.
 CH1: V_{DS_PRI} , 100 V / div.
 CH2: I_{DS_PRI} , 1 A / div.
 CH4: V_{BUS_IN} , 1 V / div.
 Time: 100 ms / div. (200 μs / div. Zoom).

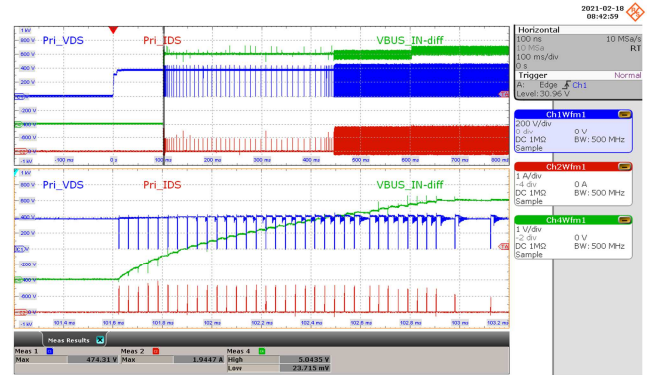


Figure 58 – Primary Drain Voltage and Current.
 265 VAC, 5.0 V, 5 A (CR Mode, 930 mΩ at the End of 100 mΩ Cable).
 $V_{DS_PRI} = 474$ V Maximum.
 CH1: V_{DS_PRI} , 200 V / div.
 CH2: I_{DS_PRI} , 1 A / div.
 CH4: V_{BUS_IN} , 1 V / div.
 Time: 100 ms / div. (200 μs / div. Zoom).

13.1.3 SR FET Drain Voltage and Current

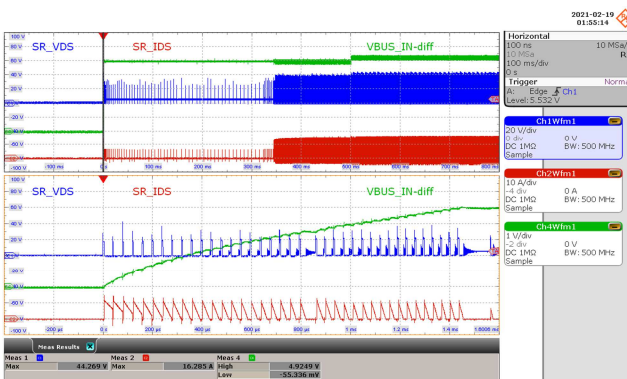


Figure 59 – SR FET Drain Voltage and Current.
 90 VAC, 5.0 V, 5 A (CR Mode, 930 mΩ at the End of 100 mΩ Cable).
 $V_{DS_SRFET} = 44.2$ V Maximum.
 CH1: V_{DS_SRFET} , 20 V / div.
 CH2: I_{DS_SRFET} , 10 A / div.
 CH4: V_{BUS_IN} , 1 V / div.
 Time: 100 ms / div. (200 μs / div. Zoom).

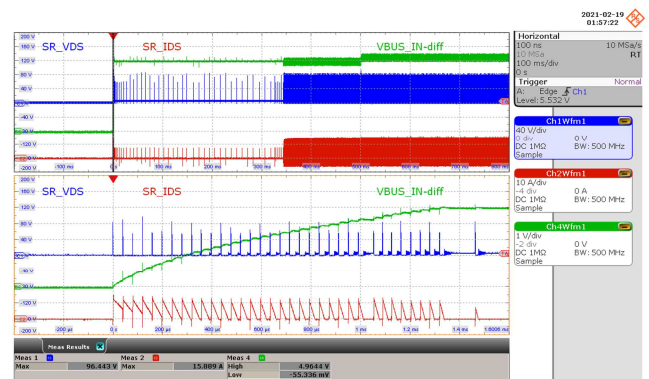


Figure 60 – SR FET Drain Voltage and Current.
 265 VAC, 5.0 V, 5 A (CR Mode, 930 mΩ at the End of 100 mΩ Cable).
 $V_{DS_SRFET} = 96.4$ V Maximum.
 CH1: V_{DS_SRFET} , 40 V / div.
 CH2: I_{DS_SRFET} , 10 A / div.
 CH4: V_{BUS_IN} , 1 V / div.
 Time: 100 ms / div. (200 μs / div. Zoom).



13.2 Primary Drain Voltage and Current (Steady-State)

13.2.1 Output: 5 V / 5 A

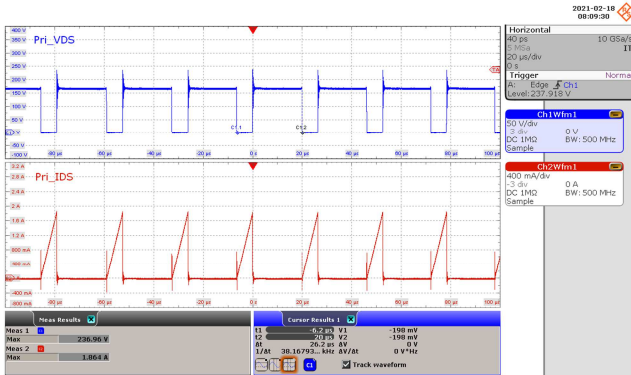


Figure 61 – Primary Drain Voltage and Current.
 90 VAC, 5.0 V, 5 A Load.
 $V_{DS_PRI} = 236\text{ V}$ Maximum.
 CH1: V_{DS_PRI} , 50 V / div.
 CH2: I_{DS_PRI} , 400 mA / div.
 Time: 20 μs / div.

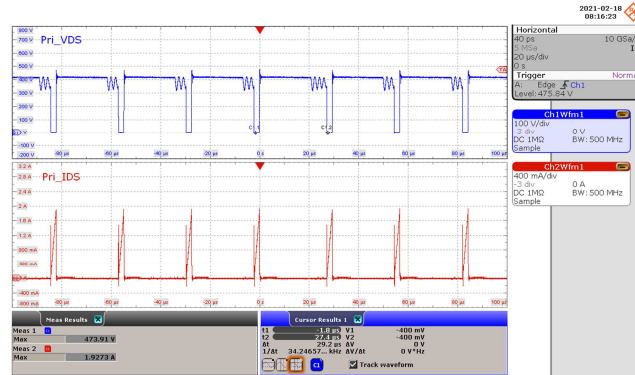


Figure 62 – Primary Drain Voltage and Current.
 265 VAC, 5.0 V, 5 A Load.
 $V_{DS_PRI} = 473\text{ V}$ Maximum.
 CH1: V_{DS_PRI} , 100 V / div.
 CH2: I_{DS_PRI} , 400 mA / div.
 Time: 20 μs / div.

13.2.2 Output: 9 V / 5 A

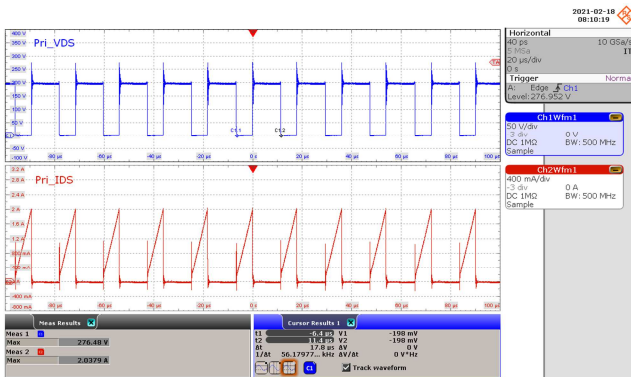


Figure 63 – Primary Drain Voltage and Current.
 90 VAC, 9.0 V, 5 A Load.
 $V_{DS_PRI} = 276\text{ V}$ Maximum.
 CH1: V_{DS_PRI} , 50 V / div.
 CH2: I_{DS_PRI} , 400 mA / div.
 Time: 20 μs / div.

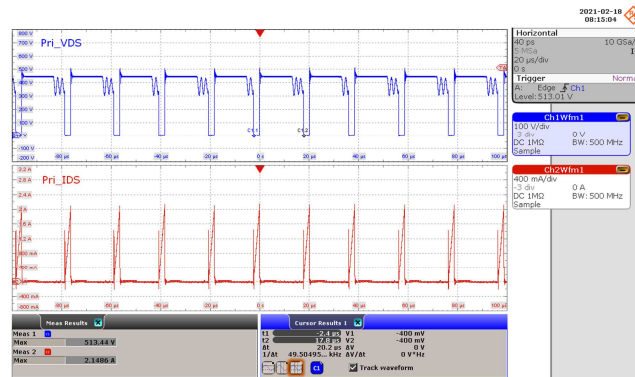


Figure 64 – Primary Drain Voltage and Current.
 265 VAC, 9.0 V, 5 A Load.
 $V_{DS_PRI} = 513\text{ V}$ Maximum.
 CH1: V_{DS_PRI} , 100 V / div.
 CH2: I_{DS_PRI} , 400 mA / div.
 Time: 20 μs / div.

13.2.3 Output: 15 V / 3 A

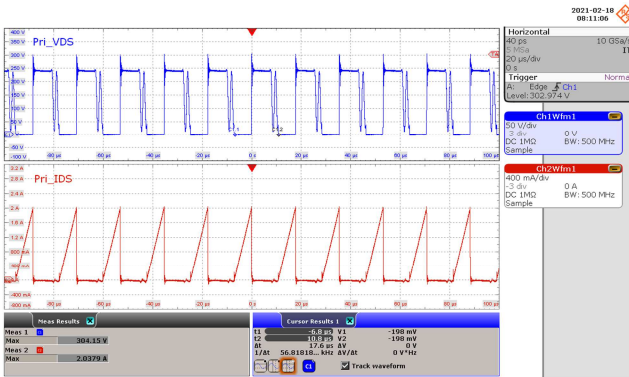


Figure 65 – Primary Drain Voltage and Current.
 90 VAC, 15.0 V, 3 A Load.
 $V_{DS_PRI} = 304\text{ V}$ Maximum.
 CH1: V_{DS_PRI} , 50 V / div.
 CH2: I_{DS_PRI} , 400 mA / div.
 Time: 20 μ s / div.

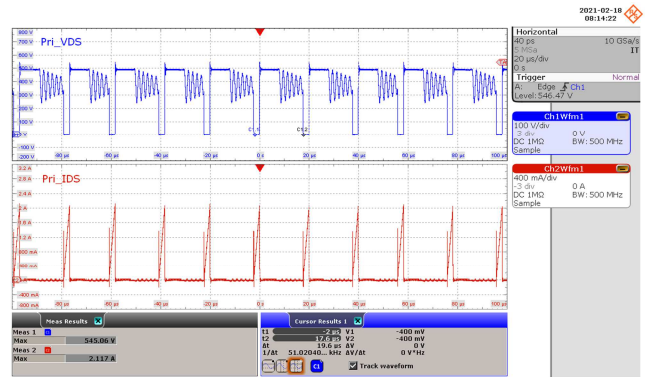


Figure 66 – Primary Drain Voltage and Current.
 265 VAC, 15.0 V, 3 A Load.
 $V_{DS_PRI} = 545\text{ V}$ Maximum.
 CH1: V_{DS_PRI} , 100 V / div.
 CH2: I_{DS_PRI} , 400 mA / div.
 Time: 20 μ s / div.

13.2.4 Output: 20 V / 2.25 A

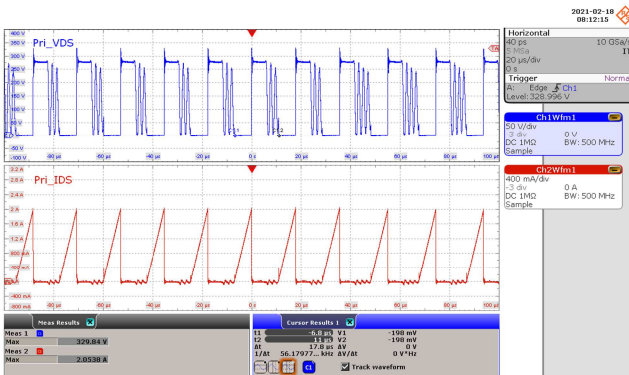


Figure 67 – Primary Drain Voltage and Current.
 90 VAC, 20.0 V, 2.25 A Load.
 $V_{DS_PRI} = 329\text{ V}$ Maximum.
 CH1: V_{DS_PRI} , 50 V / div.
 CH2: I_{DS_PRI} , 400 mA / div.
 Time: 20 μ s / div.

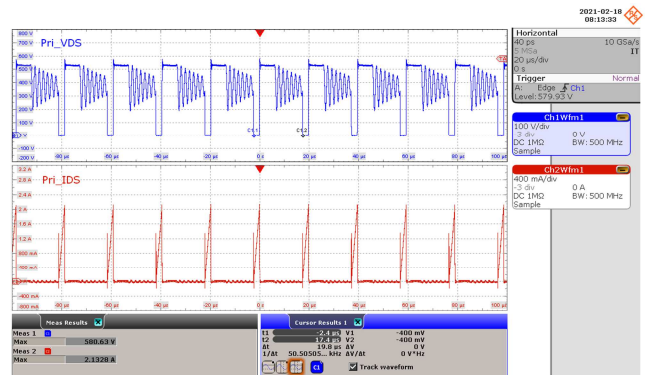


Figure 68 – Primary Drain Voltage and Current.
 265 VAC, 20.0 V, 2.25 A Load.
 $V_{DS_PRI} = 580\text{ V}$ Maximum.
 CH1: V_{DS_PRI} , 100 V / div.
 CH2: I_{DS_PRI} , 400 mA / div.
 Time: 20 μ s / div.



13.3 SR FET Drain Voltage and Current (Steady-State)

13.3.1 Output: 5 V / 5 A

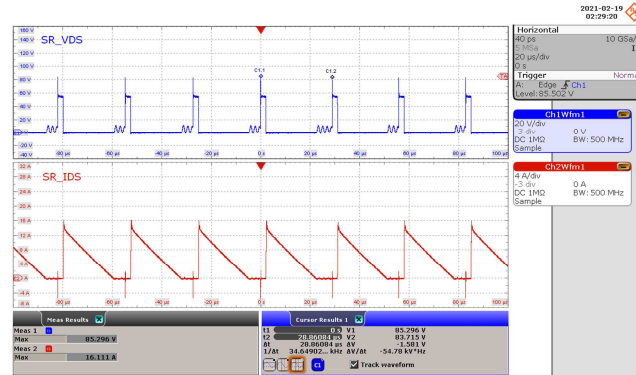
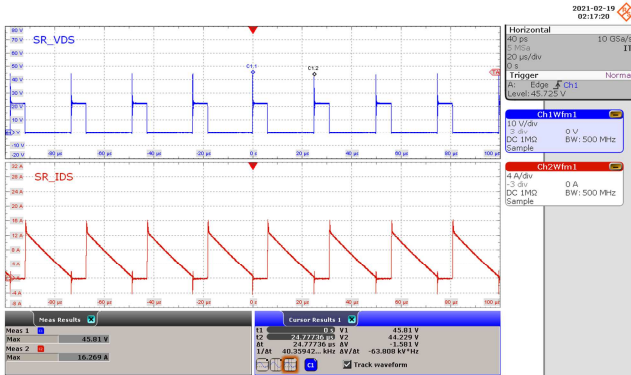


Figure 69 – SR FET Drain Voltage and Current.
 90 VAC, 5.0 V, 5 A Load.
 $V_{DS_SRFET} = 45.8 \text{ V}$ Maximum.
 CH1: V_{DS_SRFET} , 10 V / div.
 CH2: I_{DS_SRFET} , 4 A / div.
 Time: 20 μs / div.

Figure 70 – SR FET Drain Voltage and Current.
 265 VAC, 5.0 V, 5 A Load.
 $V_{DS_SRFET} = 85.2 \text{ V}$ Maximum.
 CH1: V_{DS_SRFET} , 20 V / div.
 CH2: I_{DS_SRFET} , 4 A / div.
 Time: 20 μs / div.

13.3.2 Output: 9 V / 5 A

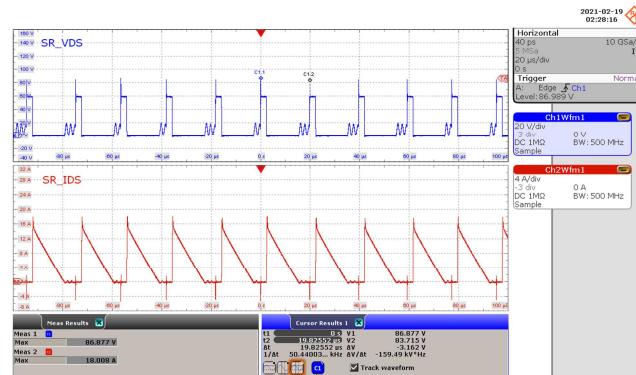
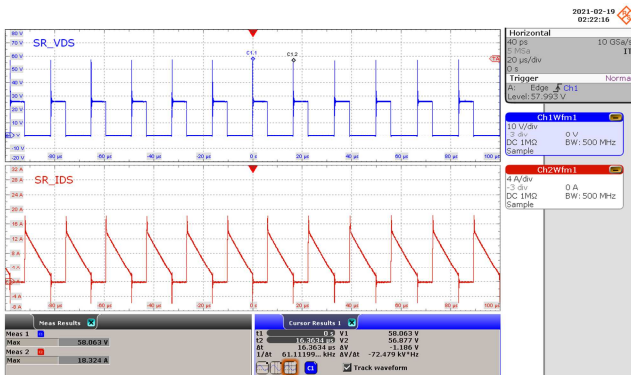


Figure 71 – SR FET Drain Voltage and Current.
 90 VAC, 9.0 V, 5 A Load.
 $V_{DS_SRFET} = 58.0 \text{ V}$ Maximum.
 CH1: V_{DS_SRFET} , 10 V / div.
 CH2: I_{DS_SRFET} , 4 A / div.
 Time: 20 μs / div.

Figure 72 – SR FET Drain Voltage and Current.
 265 VAC, 9.0 V, 5 A Load.
 $V_{DS_SRFET} = 86.8 \text{ V}$ Maximum.
 CH1: V_{DS_SRFET} , 20 V / div.
 CH2: I_{DS_SRFET} , 10 A / div.
 Time: 20 μs / div.

13.3.3 Output: 15 V / 3 A

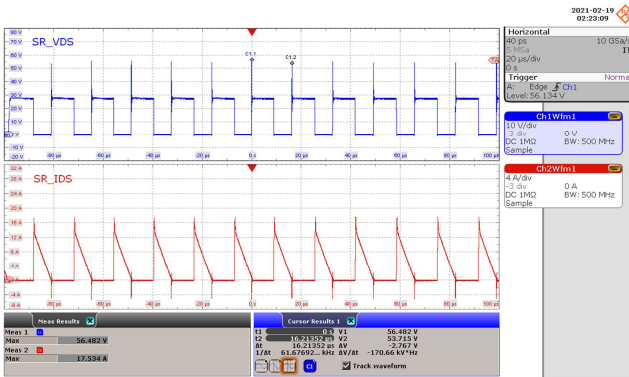


Figure 73 – SR FET Drain Voltage and Current.
 90 VAC, 15.0 V, 3 A Load.
 $V_{DS_SRFET} = 56.4 \text{ V}$ Maximum.
 CH1: V_{DS_SRFET} , 10 V / div.
 CH2: I_{DS_SRFET} , 4 A / div.
 Time: 20 μs / div.

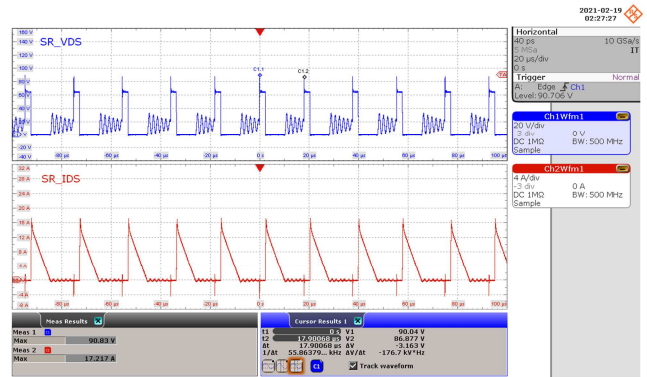


Figure 74 – SR FET Drain Voltage and Current.
 265 VAC, 15.0 V, 3 A Load.
 $V_{DS_SRFET} = 90.8 \text{ V}$ Maximum.
 CH1: V_{DS_SRFET} , 20 V / div.
 CH2: I_{DS_SRFET} , 4 A / div.
 Time: 20 μs / div.

13.3.4 Output: 20 V / 2.25 A

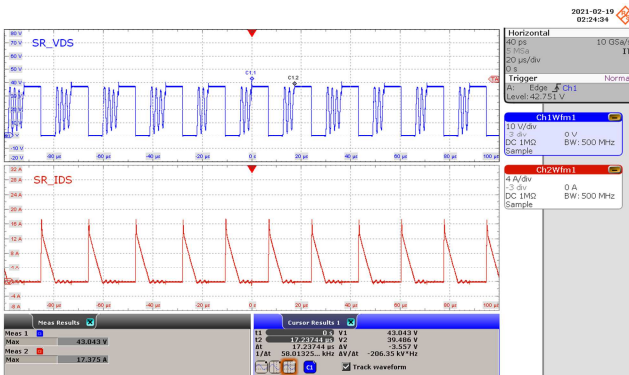


Figure 75 – SR FET Drain Voltage and Current.
 90 VAC, 20.0 V, 2.25 A Load.
 $V_{DS_SRFET} = 43.0 \text{ V}$ Maximum.
 CH1: V_{DS_SRFET} , 10 V / div.
 CH2: I_{DS_SRFET} , 4 A / div.
 Time: 20 μs / div.

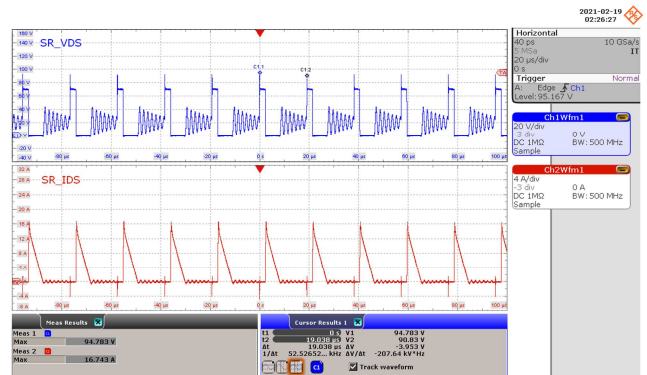


Figure 76 – SR FET Drain Voltage and Current.
 265 VAC, 20.0 V, 2.25 A Load.
 $V_{DS_SRFET} = 94.7 \text{ V}$ Maximum.
 CH1: V_{DS_SRFET} , 20 V / div.
 CH2: I_{DS_SRFET} , 4 A / div.
 Time: 20 μs / div.



13.4 Primary and SR FET Drain Voltage and Current (during Output Voltage Transition)

13.4.1 Primary Drain Voltage and Current, 3.3 V to 21 V PPS Transition

Primary Drain Voltage, Drain Current, and output voltage on the board were captured. The USB PD Sink Request was changed from 3.3 V to 21 V / 2.25 A PPS (PDO7) while operating at 95% load.

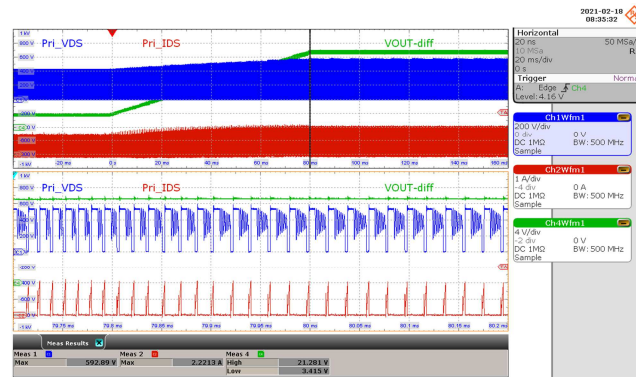
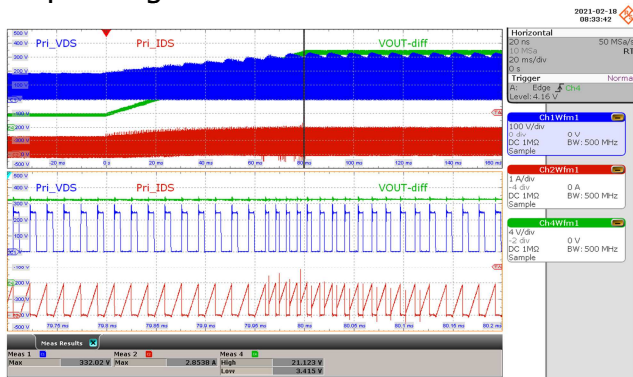


Figure 77 – Primary Drain Voltage and Current.
 90 VAC, 3.3 V to 21 V V_{OUT} Transition,
 2.1375 A Load.
 V_{DS_PRI} = 332 V Maximum.
 CH1: V_{DS_PRI} , 100 V / div.
 CH2: I_{DS_PRI} , 1 A / div.
 CH4: V_{OUT} , 4 V / div.
 Time: 20 ms / div. (50 μ s / div. Zoom).

Figure 78 – Primary Drain Voltage and Current.
 265 VAC, 3.3 V to 21 V V_{OUT} Transition,
 2.1375 A Load.
 V_{DS_PRI} = 592 V Maximum.
 CH1: V_{DS_PRI} , 200 V / div.
 CH2: I_{DS_PRI} , 1 A / div.
 CH4: V_{OUT} , 4 V / div.
 Time: 20 ms / div. (50 μ s / div. Zoom).

13.4.2 SR FET Drain Voltage and Current, 3.3 V to 21 V Transition

SR FET Drain Voltage, Drain Current, and output voltage on the board were captured. The USB PD Sink Request was changed from 3.3 V to 21 V / 2.25 A PPS while operating at 95% load.

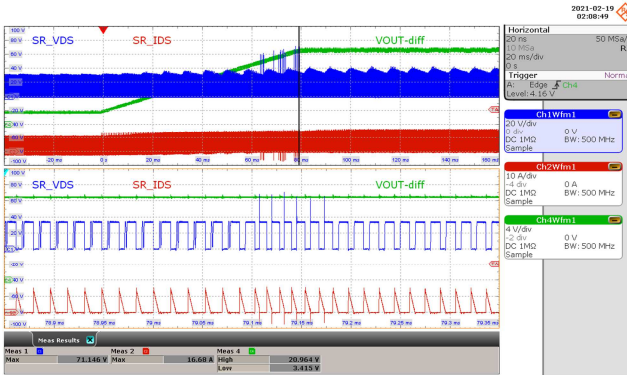


Figure 79 – Primary Drain Voltage and Current.
 90 VAC, 3.3 V to 21 V V_{OUT} Transition,
 2.1375 A Load.
 $V_{DS_SRFET} = 71.1$ V Maximum.
 CH1: V_{DS_SRFET} , 20 V / div.
 CH2: I_{DS_SRFET} , 10 A / div.
 CH4: V_{OUT} , 4 V / div.
 Time: 20 ms / div. (50 μ s / div. Zoom).

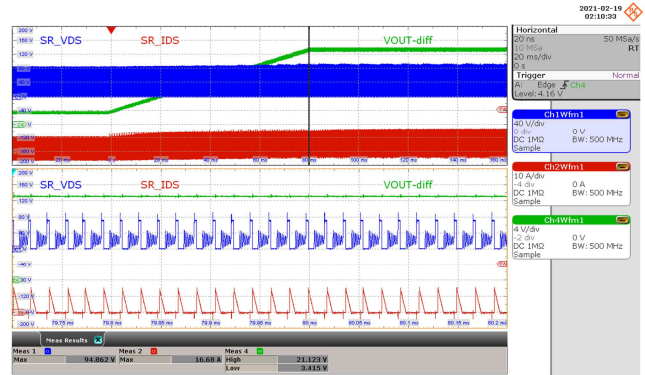


Figure 80 – Primary Drain Voltage and Current.
 265 VAC, 3.3 V to 21 V V_{OUT} Transition,
 2.1375 A Load.
 $V_{DS_SRFET} = 94.8$ V Maximum.
 CH1: V_{DS_SRFET} , 40 V / div.
 CH2: I_{DS_SRFET} , 10 A / div.
 CH4: V_{OUT} , 4 V / div.
 Time: 20 ms / div. (50 μ s / div. Zoom).

13.5 Load Transient and Output Ripple Measurements

13.5.1 Ripple Measurement Technique

For load transient response and DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 $\mu\text{F}/50\text{ V}$ ceramic type and one (1) 47 $\mu\text{F}/50\text{ V}$ aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

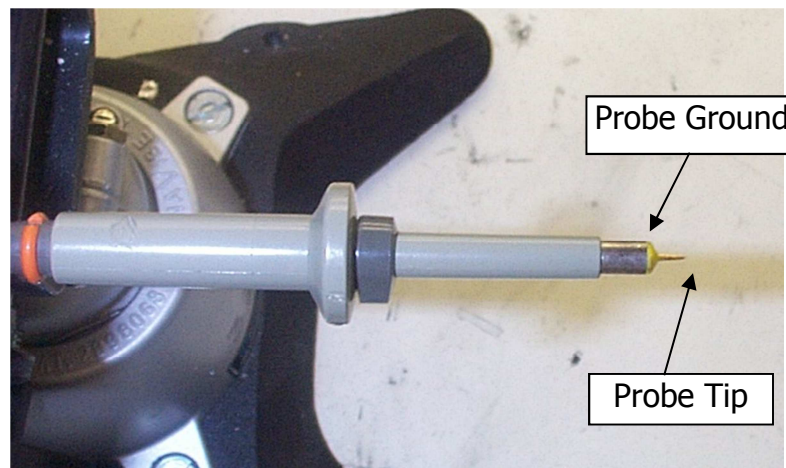


Figure 81 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

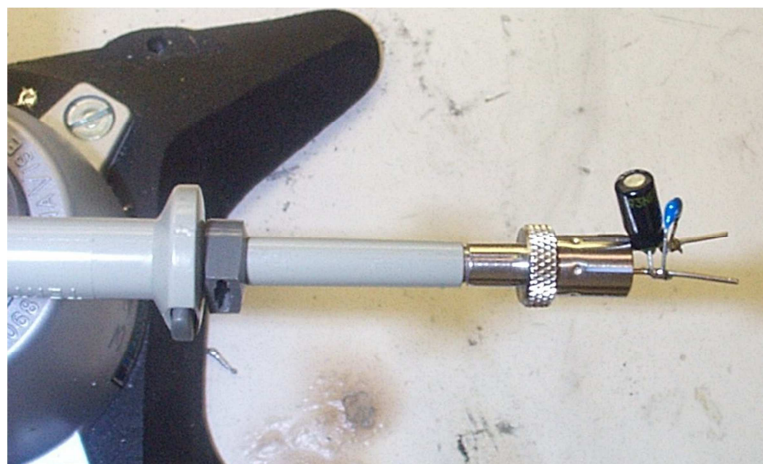


Figure 82 – Oscilloscope Probe with Probe Master (www.probemaster.com) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

13.5.2 Load Transient Response

Output voltage waveform was captured at the end of 100 mΩ cable using the ripple measurement probe with decoupling capacitors. Duration for load states (high = 20 ms; low = 20 ms) was chosen to clearly show steady-state for each load condition. Load slew rate (150 mA / μs) is based on USB PD 3.0 PPS specification.

13.5.2.1 Output: 5 V / 5 A

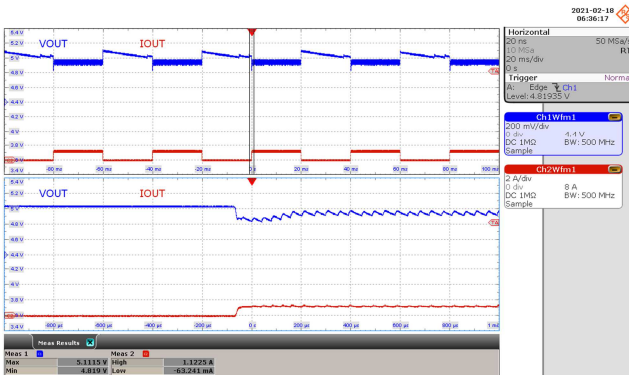


Figure 83 – Transient Response.
 90 VAC, 5.0 V, 0 to 25% Load.
 $V_{OUT} = 5.11 \text{ V Max.}, 4.81 \text{ V Min.}$
 CH1: V_{OUT} , 200 mV / div.
 CH2: I_{OUT} , 2 A / div.
 Time: 20 ms / div. (200 μs / div. Zoom).

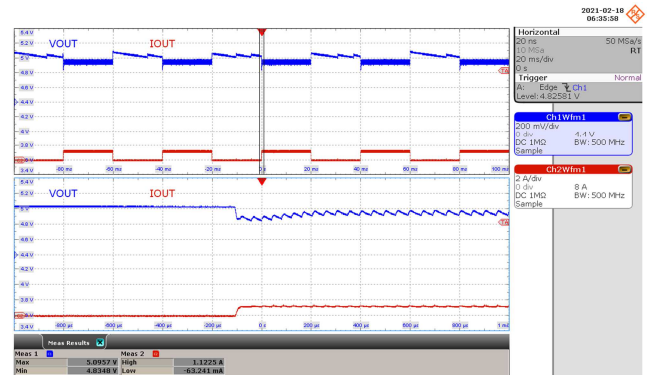


Figure 84 – Transient Response.
 265 VAC, 5.0 V, 0 to 25% Load.
 $V_{OUT} = 5.09 \text{ V Max.}, 4.83 \text{ V Min.}$
 CH1: V_{OUT} , 200 mV / div.
 CH2: I_{OUT} , 2 A / div.
 Time: 20 ms / div. (200 μs / div. Zoom).

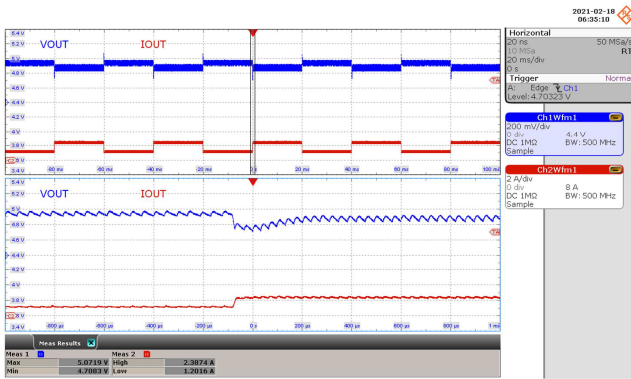


Figure 85 – Transient Response.
 90 VAC, 5.0 V, 25% to 50% Load.
 $V_{OUT} = 5.07 \text{ V Max.}, 4.70 \text{ V Min.}$
 CH1: V_{OUT} , 200 mV / div.
 CH2: I_{OUT} , 2 A / div.
 Time: 20 ms / div. (200 μ s / div. Zoom).

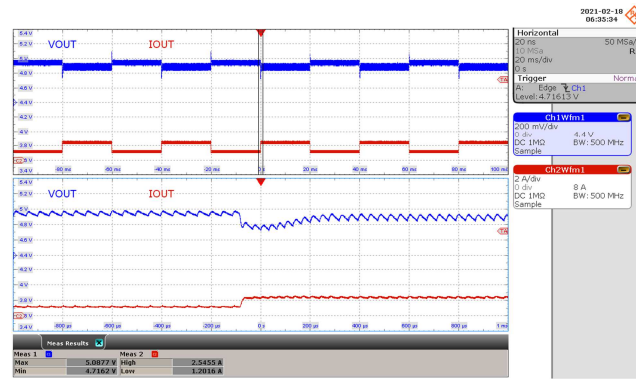


Figure 86 – Transient Response.
 265 VAC, 5.0 V, 25% to 50% Load.
 $V_{OUT} = 5.08 \text{ V Max.}, 4.71 \text{ V Min.}$
 CH1: V_{OUT} , 200 mV / div.
 CH2: I_{OUT} , 2 A / div.
 Time: 20 ms / div. (200 μ s / div. Zoom).

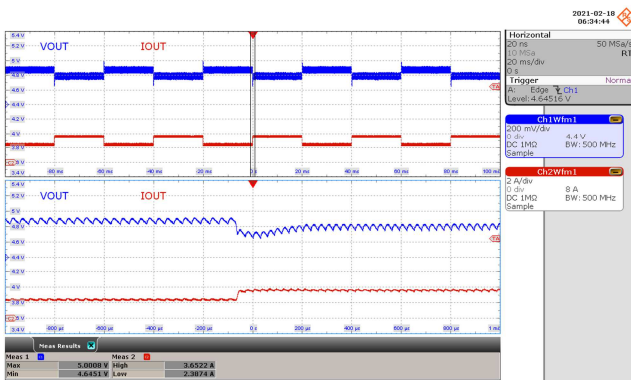


Figure 87 – Transient Response.
 90 VAC, 5.0 V, 50% to 75% Load.
 $V_{OUT} = 5.00 \text{ V Max.}, 4.64 \text{ V Min.}$
 CH1: V_{OUT} , 200 mV / div.
 CH2: I_{OUT} , 2 A / div.
 Time: 20 ms / div. (200 μ s / div. Zoom).

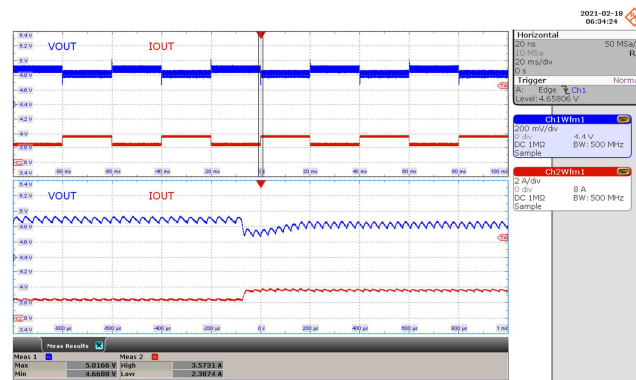


Figure 88 – Transient Response.
 265 VAC, 5.0 V, 50% to 75% Load.
 $V_{OUT} = 5.01 \text{ V Max.}, 4.66 \text{ V Min.}$
 CH1: V_{OUT} , 200 mV / div.
 CH2: I_{OUT} , 2 A / div.
 Time: 20 ms / div. (200 μ s / div. Zoom).

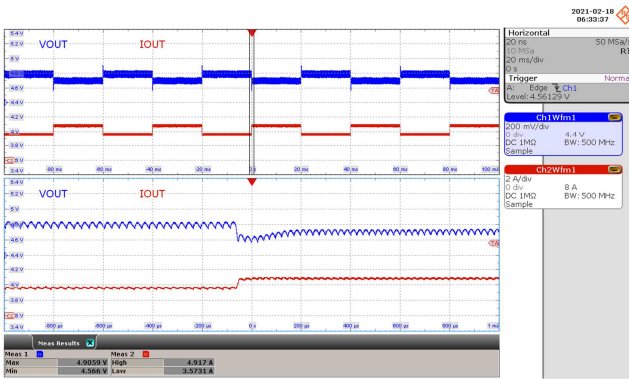


Figure 89 – Transient Response.
 90 VAC, 5.0 V, 75% to 100% Load.
 $V_{OUT} = 4.90 \text{ V Max.}, 4.56 \text{ V Min.}$
 CH1: V_{OUT} , 200 mV / div.
 CH2: I_{OUT} , 2 A / div.
 Time: 20 ms / div. (200 μ s / div. Zoom).

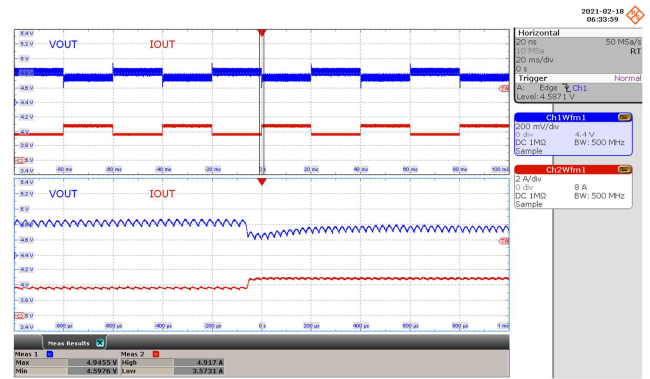


Figure 90 – Transient Response.
 265 VAC, 5.0 V, 75% to 100% Load.
 $V_{OUT} = 4.94 \text{ V Max.}, 4.59 \text{ V Min.}$
 CH1: V_{OUT} , 200 mV / div.
 CH2: I_{OUT} , 2 A / div.
 Time: 20 ms / div. (200 μ s / div. Zoom).

13.5.2.2 Output: 9 V / 5 A

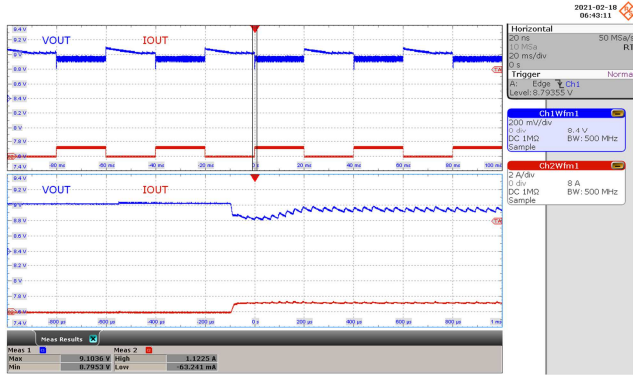


Figure 91 – Transient Response.
 90 VAC, 9.0 V, 0 to 25% Load.
 $V_{OUT} = 9.10 \text{ V Max.}, 8.79 \text{ V Min.}$
 CH1: V_{OUT} , 200 mV / div.
 CH2: I_{OUT} , 2 A / div.
 Time: 20 ms / div. (200 μ s / div. Zoom).

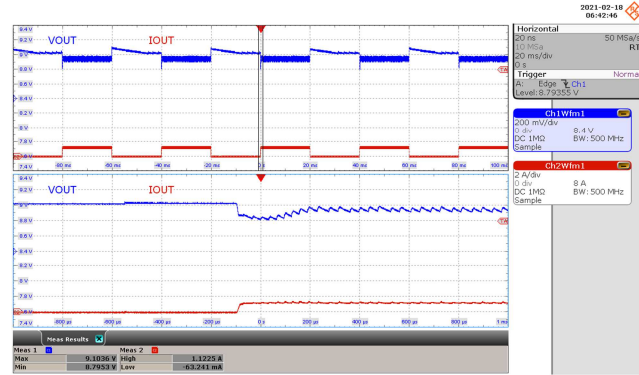


Figure 92 – Transient Response.
 265 VAC, 9.0 V, 0 to 25% Load.
 $V_{OUT} = 9.10 \text{ V Max.}, 8.79 \text{ V Min.}$
 CH1: V_{OUT} , 200 mV / div.
 CH2: I_{OUT} , 2 A / div.
 Time: 20 ms / div. (200 μ s / div. Zoom).

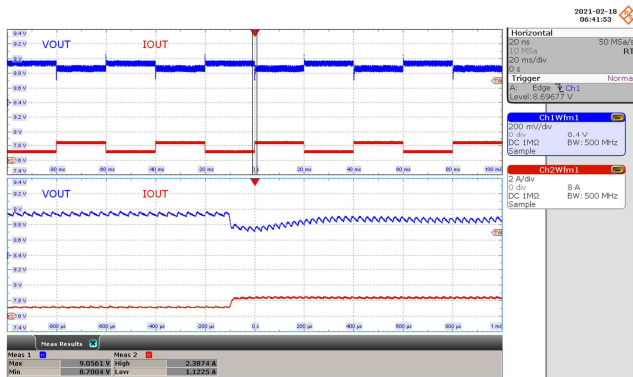


Figure 93 – Transient Response.
 90 VAC, 9.0 V, 25% to 50% Load.
 $V_{OUT} = 9.05 \text{ V Max.}, 8.70 \text{ V Min.}$
 CH1: V_{OUT} , 200 mV / div.
 CH2: I_{OUT} , 2 A / div.
 Time: 20 ms / div. (200 μ s / div. Zoom).

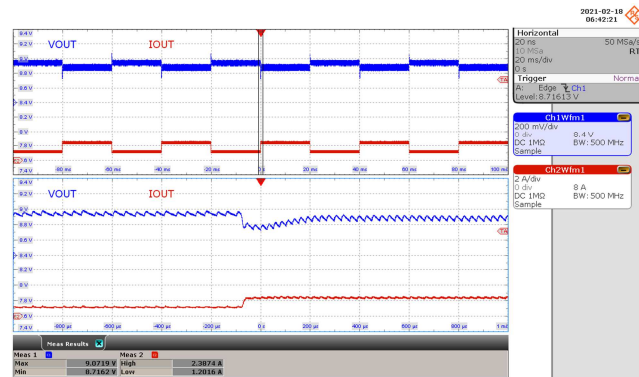


Figure 94 – Transient Response.
 265 VAC, 9.0 V, 25% to 50% Load.
 $V_{OUT} = 9.07 \text{ V Max.}, 8.71 \text{ V Min.}$
 CH1: V_{OUT} , 200 mV / div.
 CH2: I_{OUT} , 2 A / div.
 Time: 20 ms / div. (200 μ s / div. Zoom).

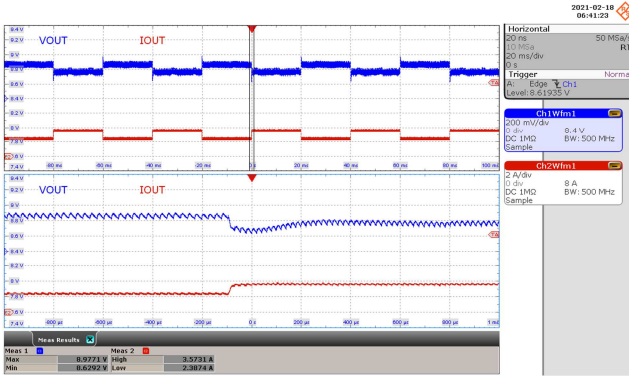


Figure 95 – Transient Response.
 90 VAC, 9.0 V, 50% to 75% Load.
 $V_{OUT} = 8.97 \text{ V Max.}, 8.62 \text{ V Min.}$
 CH1: V_{OUT} , 200 mV / div.
 CH2: I_{OUT} , 2 A / div.
 Time: 20 ms / div. (200 μs / div. Zoom).

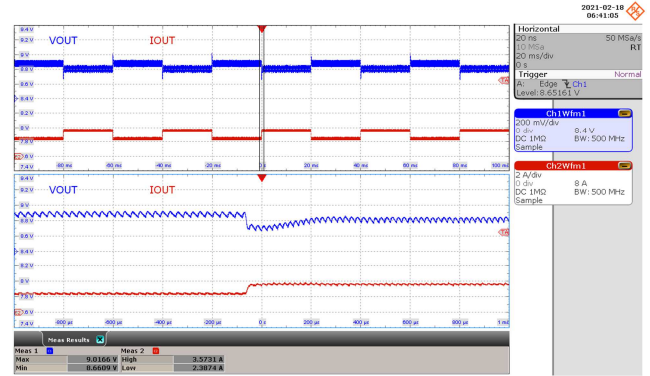


Figure 96 – Transient Response.
 265 VAC, 9.0 V, 50% to 75% Load.
 $V_{OUT} = 9.01 \text{ V Max.}, 8.66 \text{ V Min.}$
 CH1: V_{OUT} , 200 mV / div.
 CH2: I_{OUT} , 2 A / div.
 Time: 20 ms / div. (200 μs / div. Zoom).

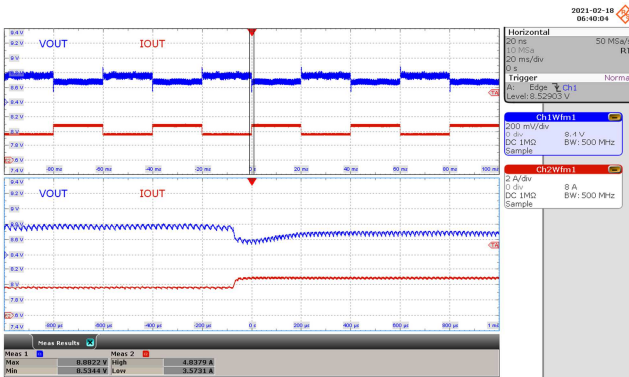


Figure 97 – Transient Response.
 90 VAC, 9.0 V, 75% to 100% Load.
 $V_{OUT} = 8.88 \text{ V Max.}, 8.53 \text{ V Min.}$
 CH1: V_{OUT} , 200 mV / div.
 CH2: I_{OUT} , 2 A / div.
 Time: 20 ms / div. (200 μs / div. Zoom).

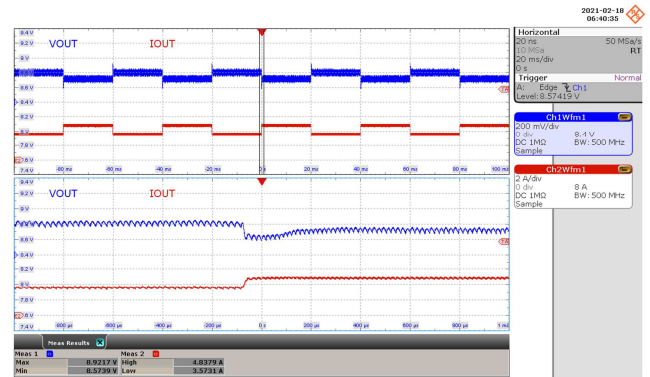


Figure 98 – Transient Response.
 265 VAC, 9.0 V, 75% to 100% Load.
 $V_{OUT} = 8.92 \text{ V Max.}, 8.57 \text{ V Min.}$
 CH1: V_{OUT} , 200 mV / div.
 CH2: I_{OUT} , 2 A / div.
 Time: 20 ms / div. (200 μs / div. Zoom).

13.5.2.3 Output: 15 V / 3 A

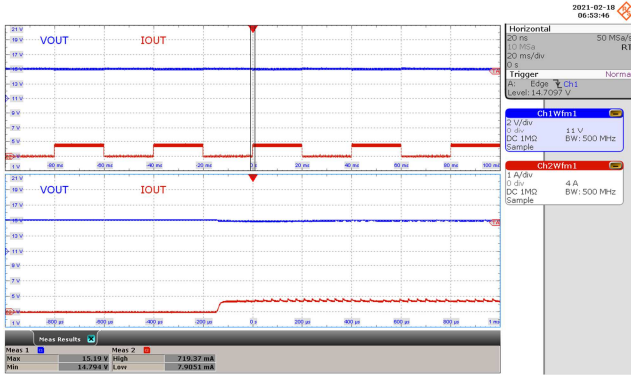


Figure 99 – Transient Response.
 90 VAC, 15.0 V, 0 to 25% Load.
 $V_{OUT} = 15.19 \text{ V Max.}, 14.79 \text{ V Min.}$
 CH1: V_{OUT} , 2 V / div.
 CH2: I_{OUT} , 1 A / div.
 Time: 20 ms / div. (200 μs / div. Zoom).

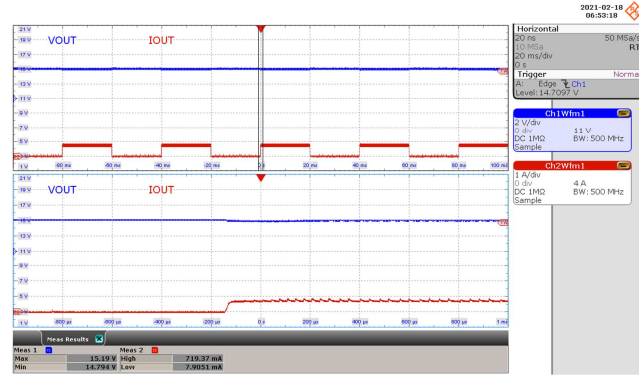


Figure 100 – Transient Response.
 265 VAC, 15.0 V, 0 to 25% Load.
 $V_{OUT} = 15.19 \text{ V Max.}, 14.79 \text{ V Min.}$
 CH1: V_{OUT} , 2 V / div.
 CH2: I_{OUT} , 1 A / div.
 Time: 20 ms / div. (200 μs / div. Zoom).

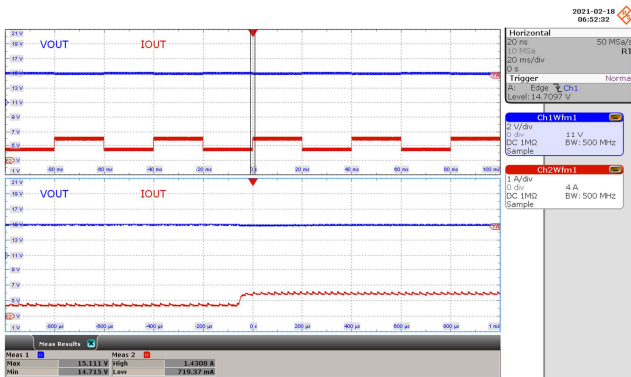


Figure 101 – Transient Response.
 90 VAC, 15.0 V, 25% to 50% Load.
 $V_{OUT} = 15.11 \text{ V Max.}, 14.71 \text{ V Min.}$
 CH1: V_{OUT} , 2 V / div.
 CH2: I_{OUT} , 1 A / div.
 Time: 20 ms / div. (200 μs / div. Zoom).

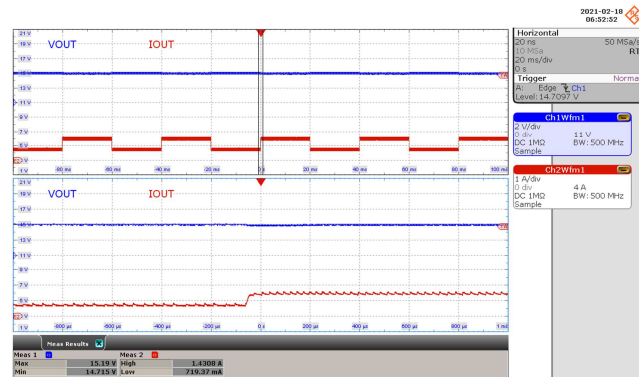


Figure 102 – Transient Response.
 265 VAC, 15.0 V, 25% to 50% Load.
 $V_{OUT} = 15.19 \text{ V Max.}, 14.71 \text{ V Min.}$
 CH1: V_{OUT} , 2 V / div.
 CH2: I_{OUT} , 1 A / div.
 Time: 20 ms / div. (200 μs / div. Zoom).

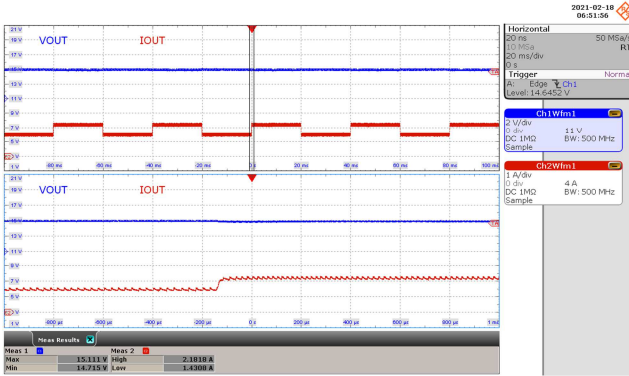


Figure 103 – Transient Response.
 90 VAC, 15.0 V, 50% to 75% Load.
 $V_{OUT} = 15.11 \text{ V Max.}, 14.71 \text{ V Min.}$
 CH1: V_{OUT} , 2 V / div.
 CH2: I_{OUT} , 1 A / div.
 Time: 20 ms / div. (200 μs / div. Zoom).

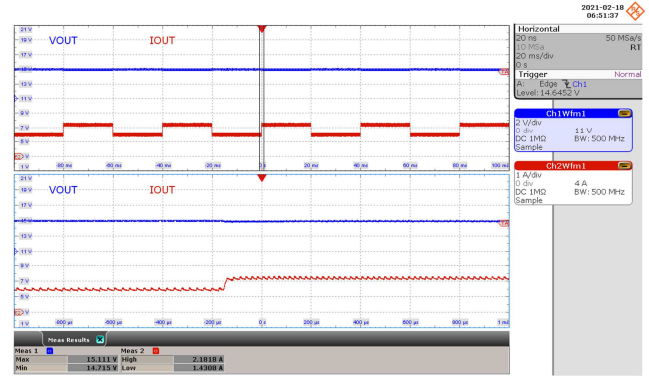


Figure 104 – Transient Response.
 265 VAC, 15.0 V, 50% to 75% Load.
 $V_{OUT} = 15.11 \text{ V Max.}, 14.71 \text{ V Min.}$
 CH1: V_{OUT} , 2 V / div.
 CH2: I_{OUT} , 1 A / div.
 Time: 20 ms / div. (200 μs / div. Zoom).

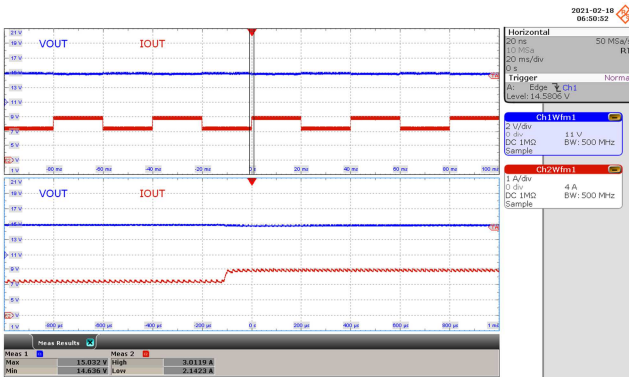


Figure 105 – Transient Response.
 90 VAC, 15.0 V, 75% to 100% Load.
 $V_{OUT} = 15.03 \text{ V Max.}, 14.63 \text{ V Min.}$
 CH1: V_{OUT} , 2 V / div.
 CH2: I_{OUT} , 1 A / div.
 Time: 20 ms / div. (200 μs / div. Zoom).

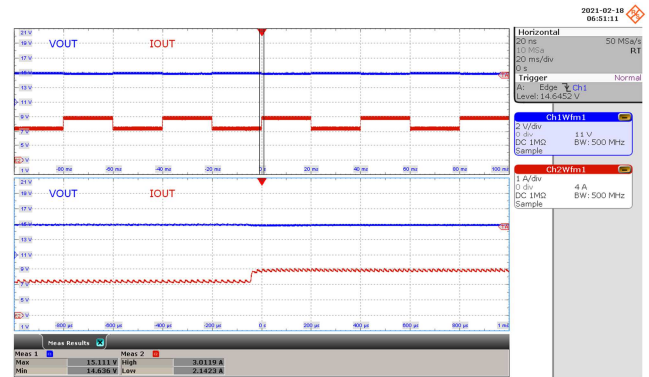


Figure 106 – Transient Response.
 265 VAC, 15.0 V, 75% to 100% Load.
 $V_{OUT} = 15.11 \text{ V Max.}, 14.63 \text{ V Min.}$
 CH1: V_{OUT} , 2 V / div.
 CH2: I_{OUT} , 1 A / div.
 Time: 20 ms / div. (200 μs / div. Zoom).



13.5.2.4 Output: 20 V / 2.25 A

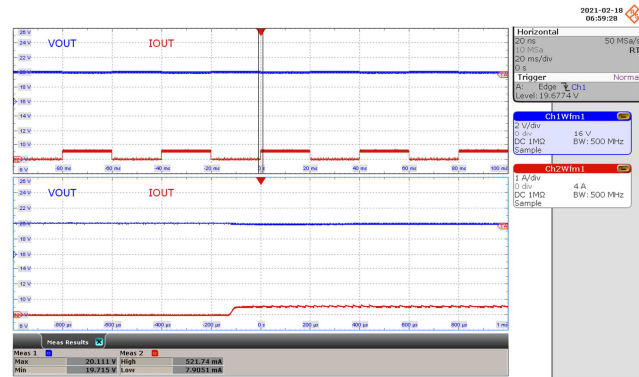
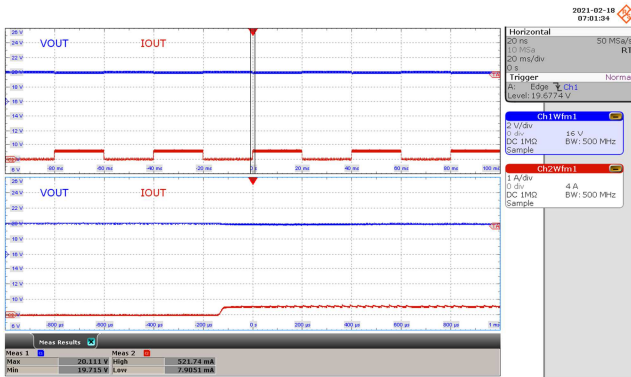


Figure 107 – Transient Response.
 90 VAC, 20.0 V, 0 to 25% Load.
 $V_{OUT} = 20.11$ V Max., 19.71 V Min.
 CH1: V_{OUT} , 2 V / div.
 CH2: I_{OUT} , 1 A / div.
 Time: 20 ms / div. (200 μ s / div. Zoom).

Figure 108 – Transient Response.
 265 VAC, 20.0 V, 0 to 25% Load.
 $V_{OUT} = 20.11$ V Max., 19.71 V Min.
 CH1: V_{OUT} , 2 V / div.
 CH2: I_{OUT} , 1 A / div.
 Time: 20 ms / div. (200 μ s / div. Zoom).

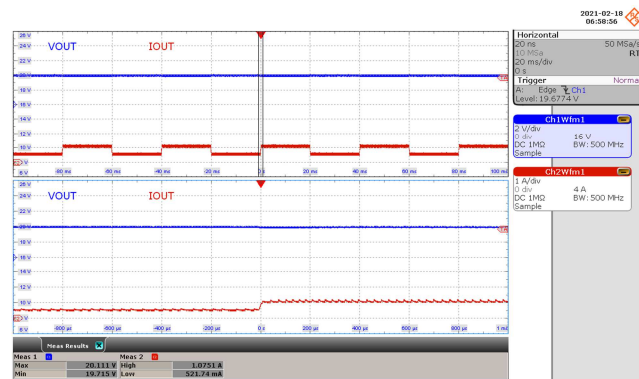
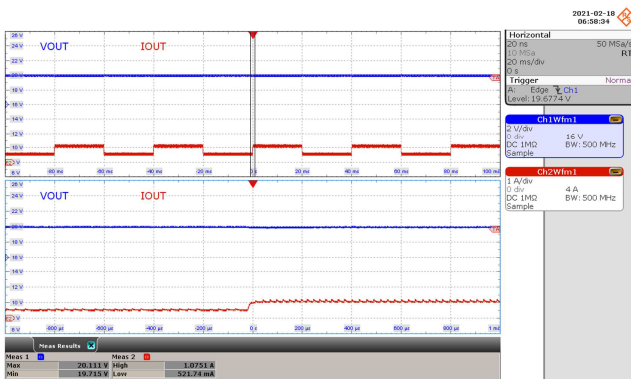


Figure 109 – Transient Response.
 90 VAC, 20.0 V, 25% to 50% Load.
 $V_{OUT} = 20.11$ V Max., 19.71 V Min.
 CH1: V_{OUT} , 2 V / div.
 CH2: I_{OUT} , 1 A / div.
 Time: 20 ms / div. (200 μ s / div. Zoom).

Figure 110 – Transient Response.
 265 VAC, 20.0 V, 25% to 50% Load.
 $V_{OUT} = 20.11$ V Max., 19.71 V Min.
 CH1: V_{OUT} , 2 V / div.
 CH2: I_{OUT} , 1 A / div.
 Time: 20 ms / div. (200 μ s / div. Zoom).

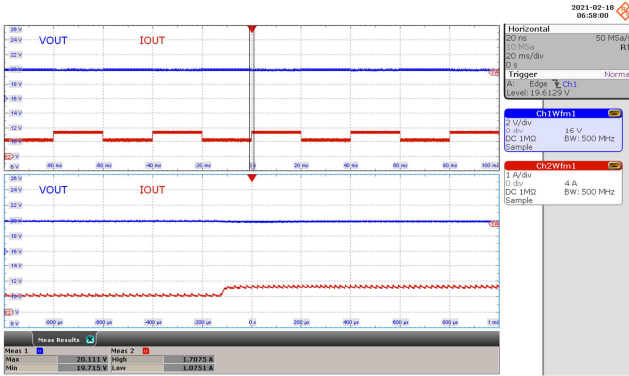


Figure 111 – Transient Response.
 90 VAC, 20.0 V, 50% to 75% Load.
 $V_{OUT} = 20.11 \text{ V Max.}, 19.71 \text{ V Min.}$
 CH1: V_{OUT} , 2 V / div.
 CH2: I_{OUT} , 1 A / div.
 Time: 20 ms / div. (200 μs / div. Zoom).

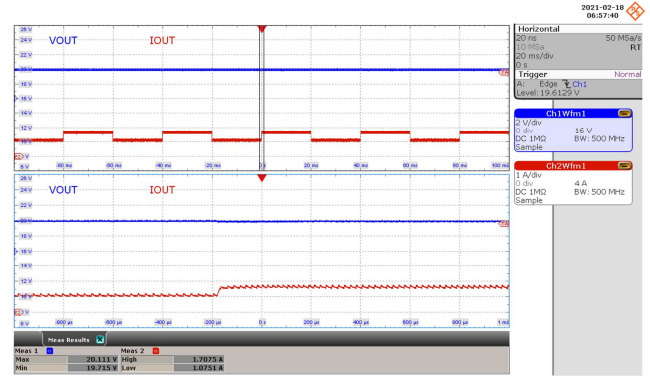


Figure 112 – Transient Response.
 265 VAC, 20.0 V, 50% to 75% Load.
 $V_{OUT} = 20.11 \text{ V Max.}, 19.71 \text{ V Min.}$
 CH1: V_{OUT} , 2 V / div.
 CH2: I_{OUT} , 1 A / div.
 Time: 20 ms / div. (200 μs / div. Zoom).

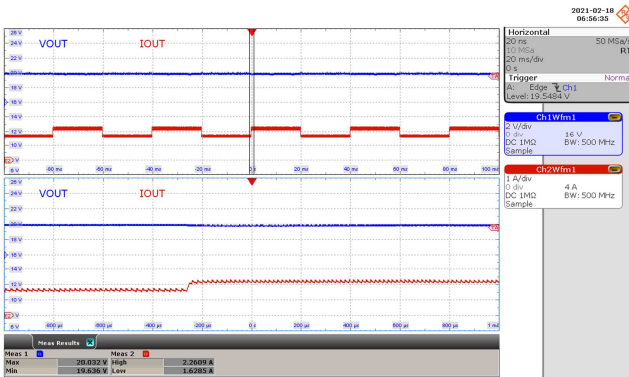


Figure 113 – Transient Response.
 90 VAC, 20.0 V, 75% to 100% Load.
 $V_{OUT} = 20.03 \text{ V Max.}, 19.63 \text{ V Min.}$
 CH1: V_{OUT} , 2 V / div.
 CH2: I_{OUT} , 1 A / div.
 Time: 20 ms / div. (200 μs / div. Zoom).

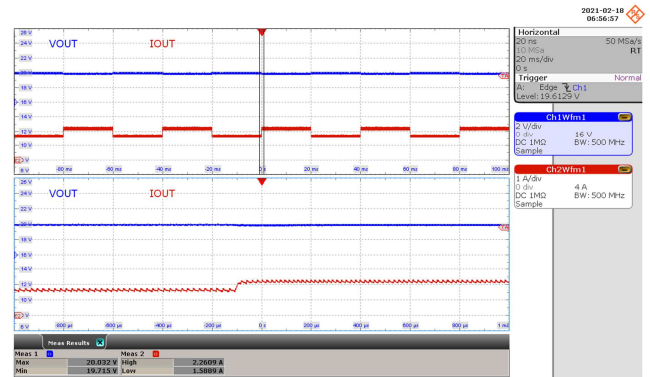


Figure 114 – Transient Response.
 265 VAC, 20.0 V, 75% to 100% Load.
 $V_{OUT} = 20.03 \text{ V Max.}, 19.71 \text{ V Min.}$
 CH1: V_{OUT} , 2 V / div.
 CH2: I_{OUT} , 1 A / div.
 Time: 20 ms / div. (200 μs / div. Zoom).



13.5.3 Output Voltage Ripple Waveforms

Output voltage ripple waveform at full load was captured at the end of 100 mΩ cable using the ripple measurement probe with decoupling capacitors.

13.5.3.1 Output: 5 V / 5 A

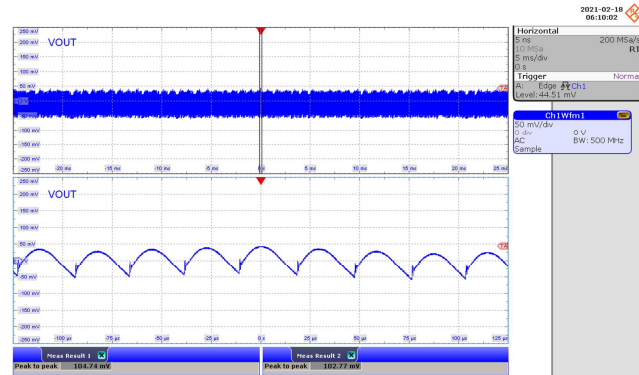
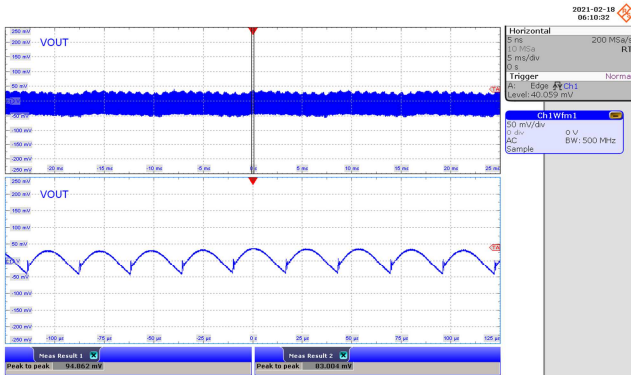


Figure 115 – Output Voltage Ripple.
 90 VAC, 5.0 V, 5 A Load.
 $V_{OUT(AC)} = 94 \text{ mV Peak-to-Peak}$.
 CH1: $V_{OUT(AC)}$, 50 mV / div.
 Time: 5 ms / div. (25 μs / div. Zoom).

Figure 116 – Output Voltage Ripple.
 265 VAC, 5.0 V, 5 A Load.
 $V_{OUT(AC)} = 104 \text{ mV Peak-to-Peak}$.
 CH1: $V_{OUT(AC)}$, 50 mV / div.
 Time: 5 ms / div. (25 μs / div. Zoom).

13.5.3.2 Output: 9 V / 5 A

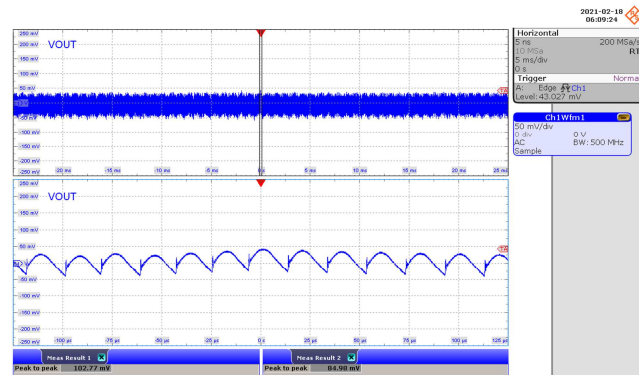
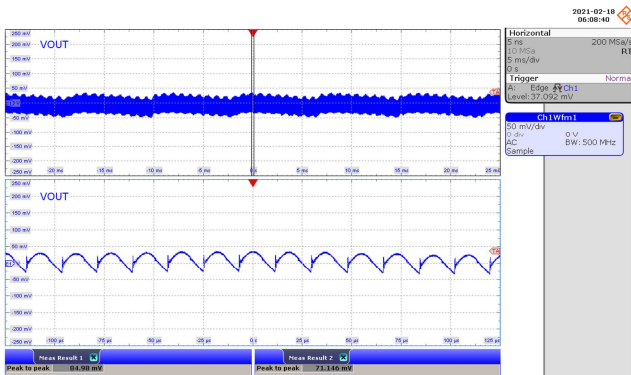


Figure 117 – Output Voltage Ripple.
 90 VAC, 9.0 V, 5 A Load.
 $V_{OUT(AC)} = 84 \text{ mV Peak-to-Peak}$.
 CH1: $V_{OUT(AC)}$, 50 mV / div.
 Time: 5 ms / div. (25 μs / div. Zoom).

Figure 118 – Output Voltage Ripple.
 265 VAC, 9.0 V, 5 A Load.
 $V_{OUT(AC)} = 102 \text{ mV Peak-to-Peak}$.
 CH1: $V_{OUT(AC)}$, 50 mV / div.
 Time: 5 ms / div. (25 μs / div. Zoom).

13.5.3.3 Output: 15 V / 3 A

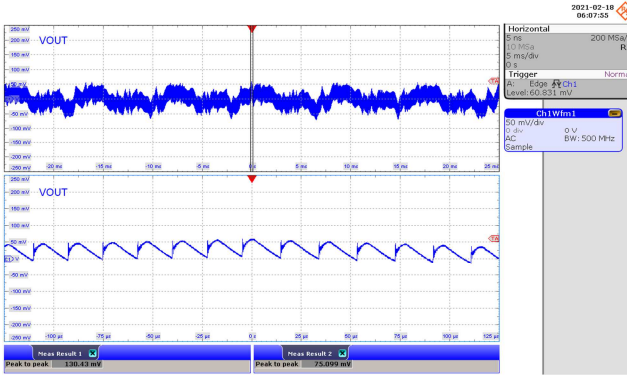


Figure 119 – Output Voltage Ripple.
 90 VAC, 15.0 V, 3 A Load.
 $V_{OUT(AC)} = 130 \text{ mV}$ Peak-to-Peak.
 CH1: $V_{OUT(AC)}$, 50 mV / div.
 Time: 5 ms / div. (25 μs / div. Zoom).

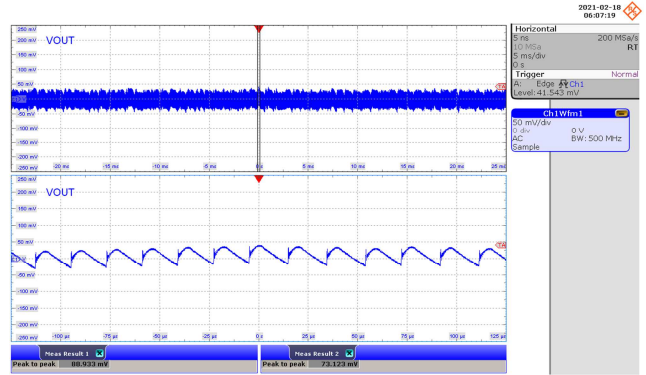


Figure 120 – Output Voltage Ripple.
 265 VAC, 15.0 V, 3 A Load.
 $V_{OUT(AC)} = 88 \text{ mV}$ Peak-to-Peak.
 CH1: $V_{OUT(AC)}$, 50 mV / div.
 Time: 5 ms / div. (25 μs / div. Zoom).

13.5.3.4 Output: 20 V / 2.25 A

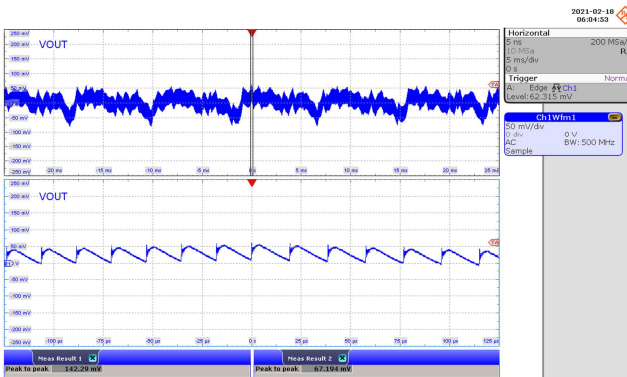


Figure 121 – Output Voltage Ripple.
 90 VAC, 20.0 V, 2.25 A Load.
 $V_{OUT(AC)} = 142 \text{ mV}$ Peak-to-Peak.
 CH1: $V_{OUT(AC)}$, 50 mV / div.
 Time: 5 ms / div. (25 μs / div. Zoom).

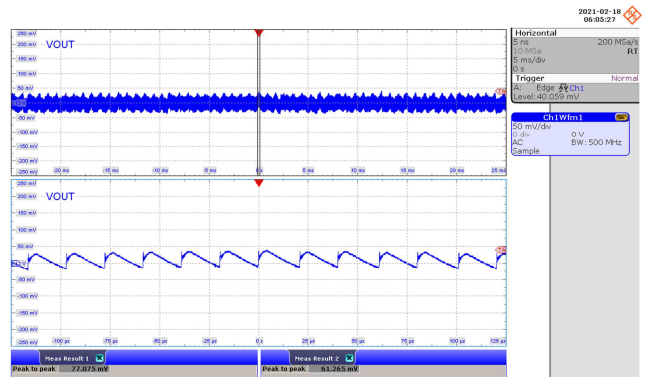


Figure 122 – Output Voltage Ripple.
 265 VAC, 20.0 V, 2.25 A Load.
 $V_{OUT(AC)} = 77 \text{ mV}$ Peak-to-Peak.
 CH1: $V_{OUT(AC)}$, 50 mV / div.
 Time: 5 ms / div. (25 μs / div. Zoom).



13.5.4 Output Voltage Ripple Amplitude vs. Load

13.5.4.1 Output: 5 V / 5 A

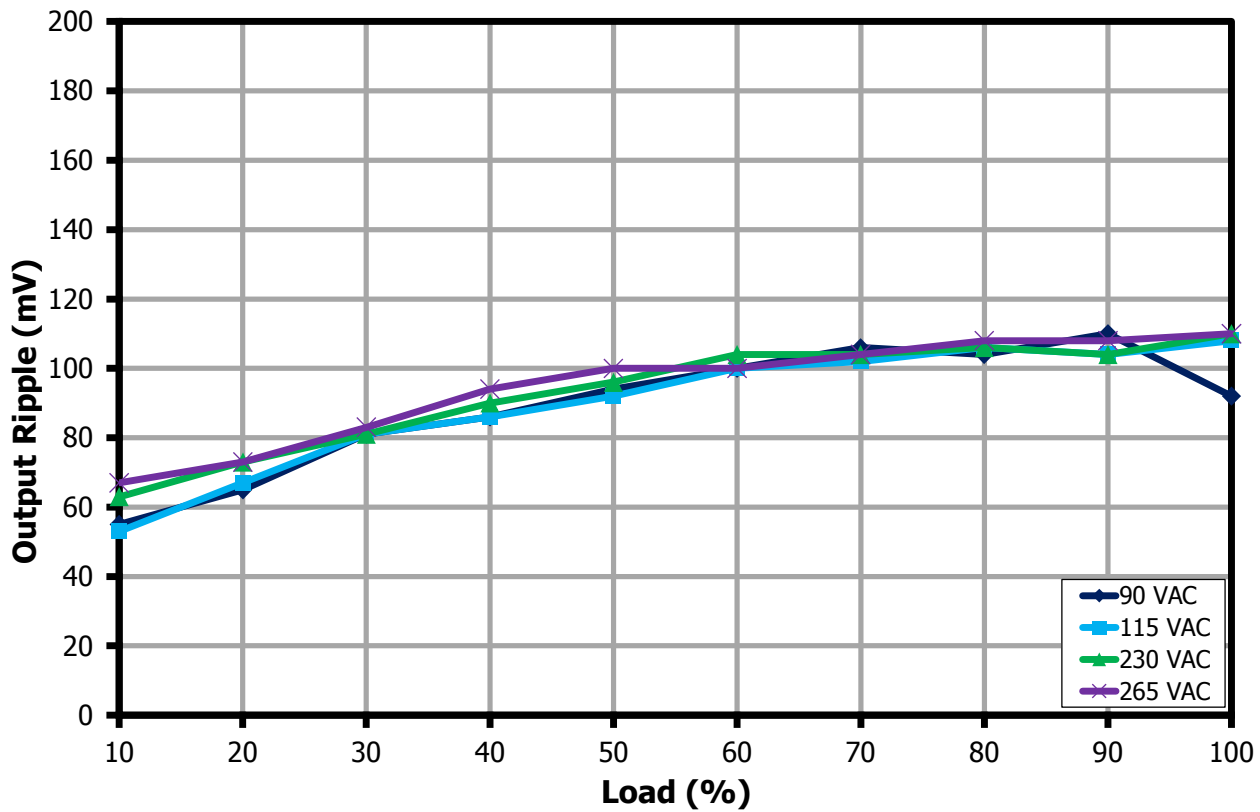


Figure 123 – Peak-to-Peak Output Voltage Ripple Amplitude vs. Load for 5 V Output.

13.5.4.2 Output: 9 V / 5 A

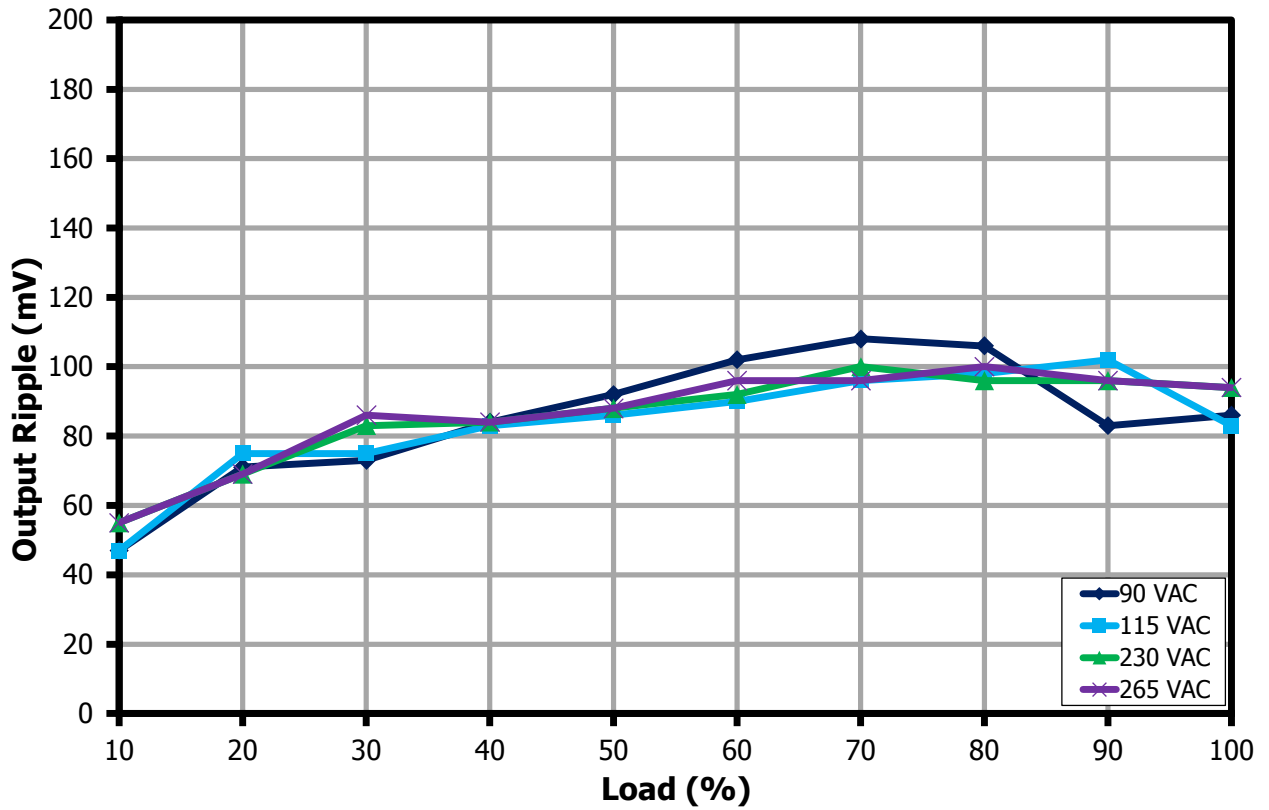


Figure 124 – Peak-to-Peak Output Voltage Ripple Amplitude vs. Load for 9 V Output.



13.5.4.3 Output: 15 V / 3 A

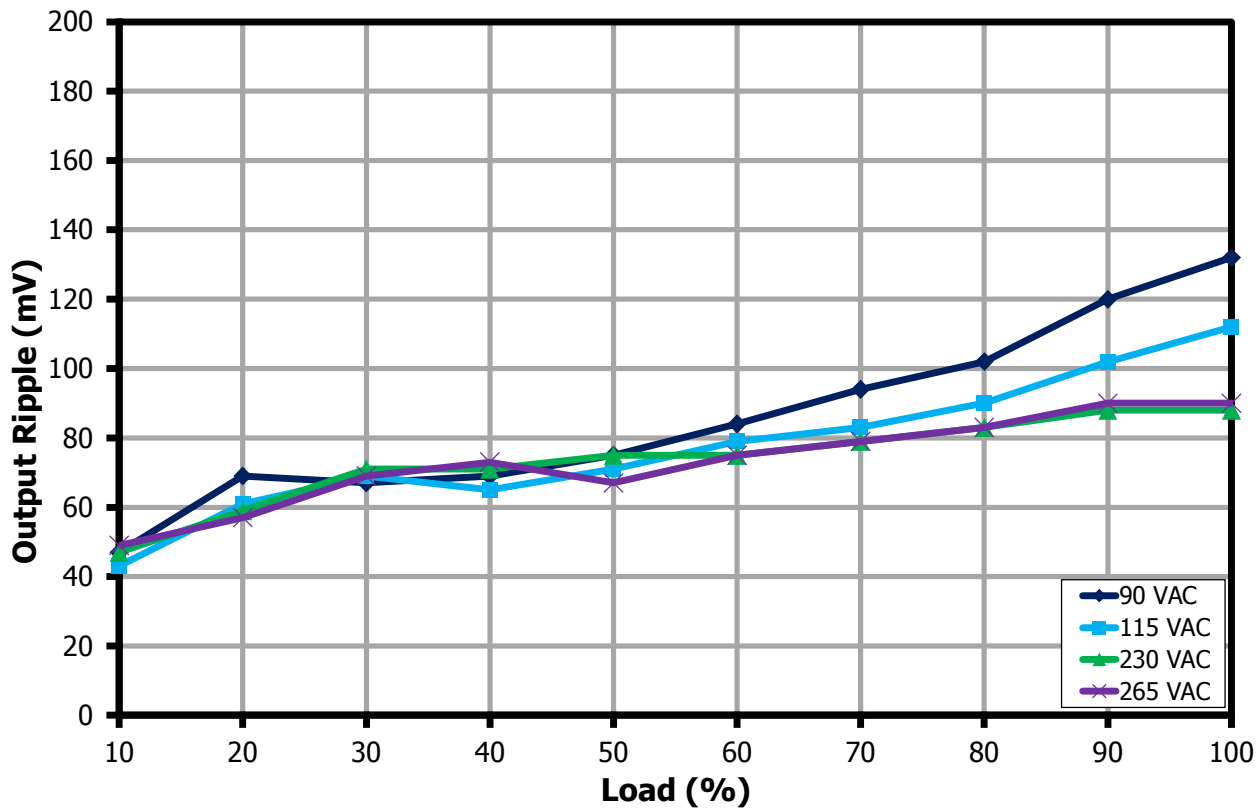


Figure 125 – Peak-to-Peak Output Voltage Ripple Amplitude vs. Load for 15 V Output.

13.5.4.4 Output: 20 V / 2.25 A

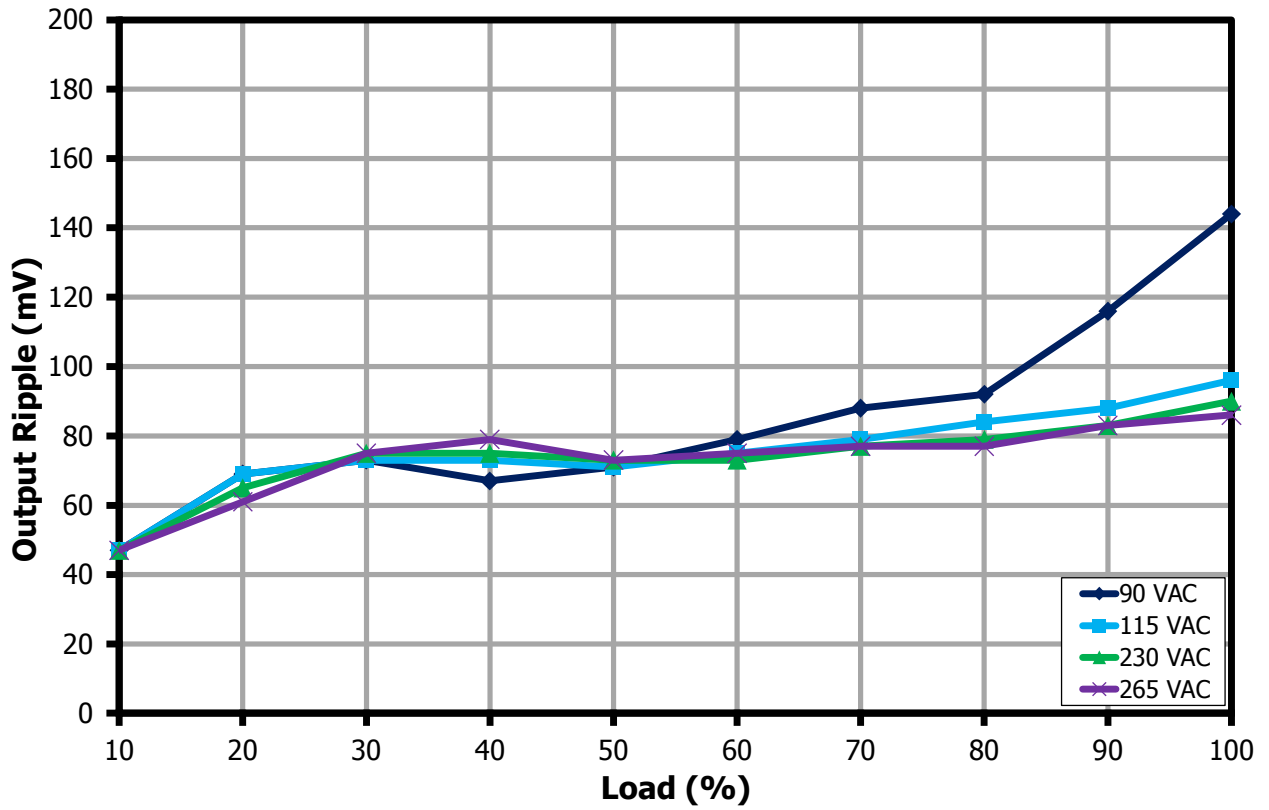


Figure 126 – Peak-to-Peak Output Voltage Ripple Amplitude vs. Load for 20 V Output.



14 CV/CC Profile

Three Programmable Power Supply (PPS) Augmented Power Data Objects (APDO) are supported in this design:

- PDO5: 3.3 V – 11 V / 5 A PPS (45 W power-limited)
- PDO6: 3.3 V – 16 V / 3 A PPS
- PDO7: 3.3 V – 21 V / 2.25 A PPS

CVCC profiles were taken with the output voltage measured on the board.

14.1 *Output: 9 V / 5 A PPS Request, PDO5 (45 W Power-Limited)*

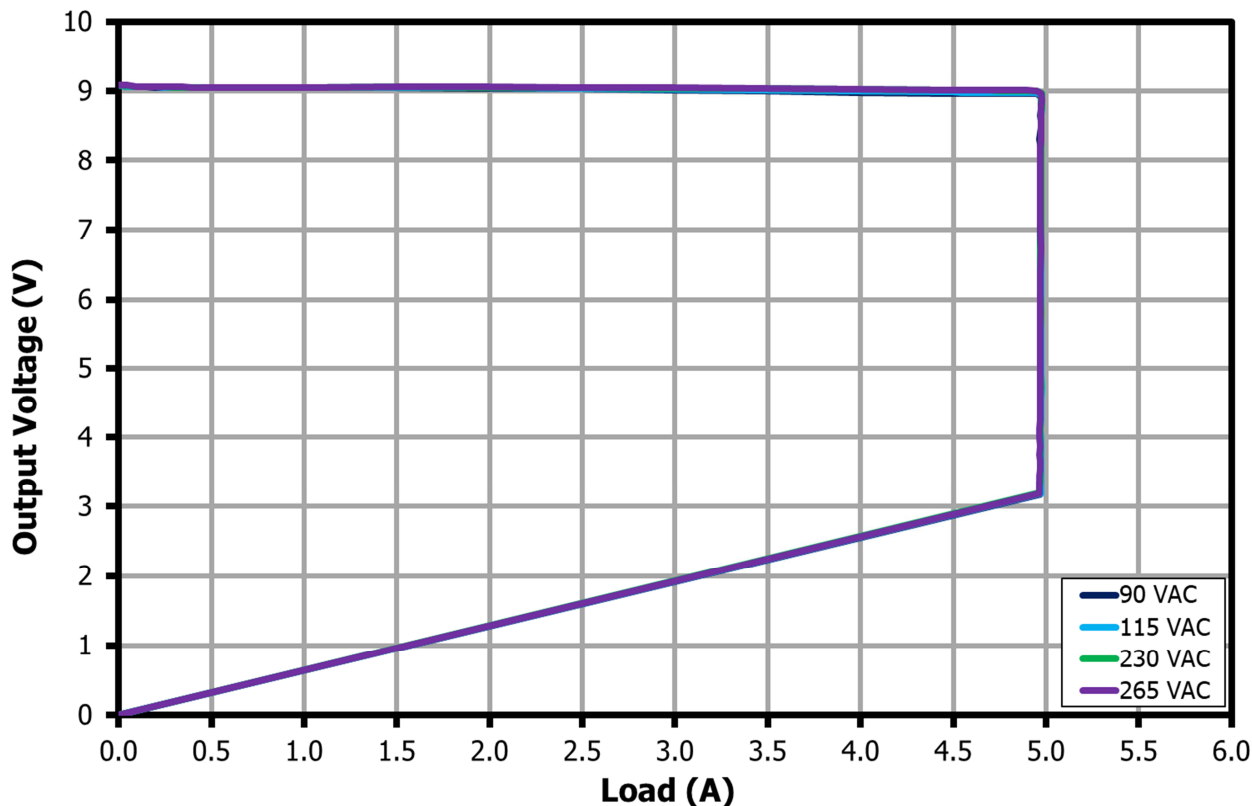


Figure 127 – CV/CC Profile for 9 V / 5 A PPS Request.

14.2 **Output: 11 V / 5 A PPS Request, PDO5 (45 W Power-Limited)**

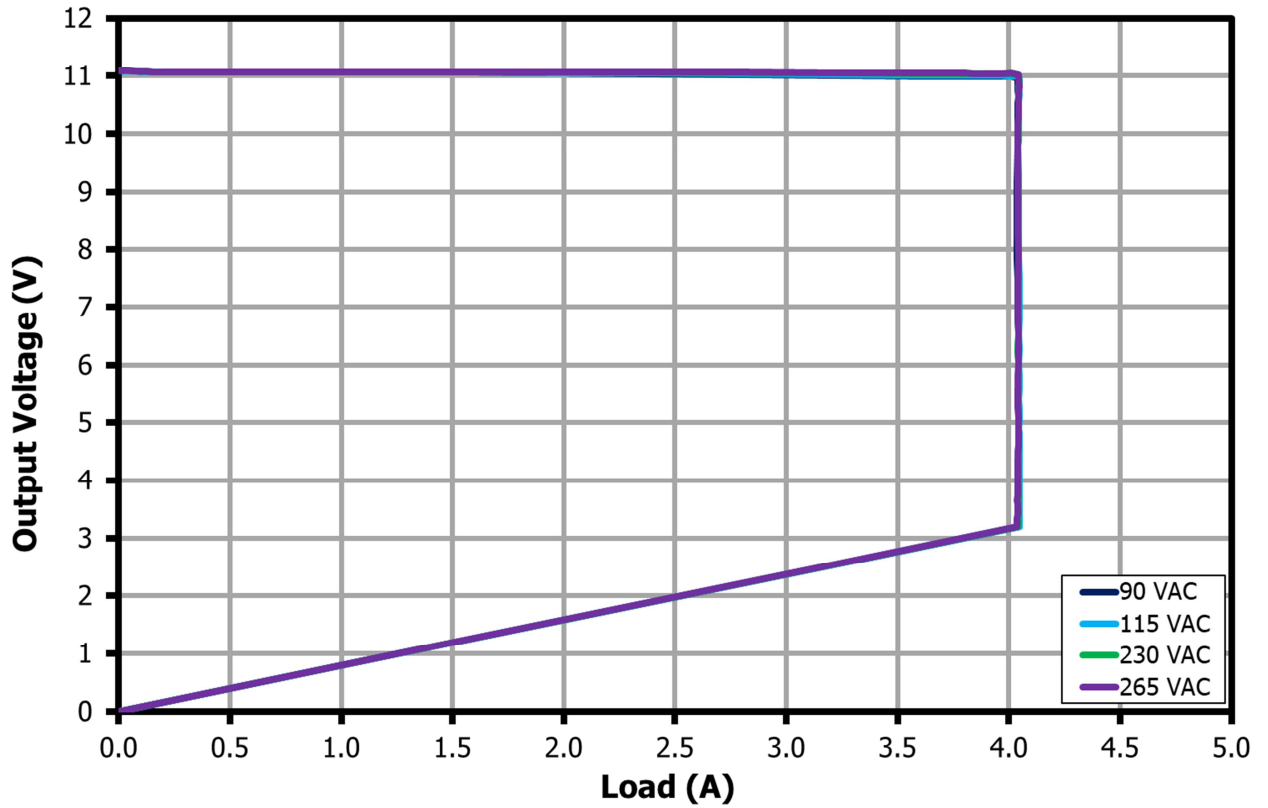


Figure 128 – CV/CC Profile for 11 V / 5 A PPS Request.



14.3 **Output: 16 V / 3 A PPS Request, PDO6**

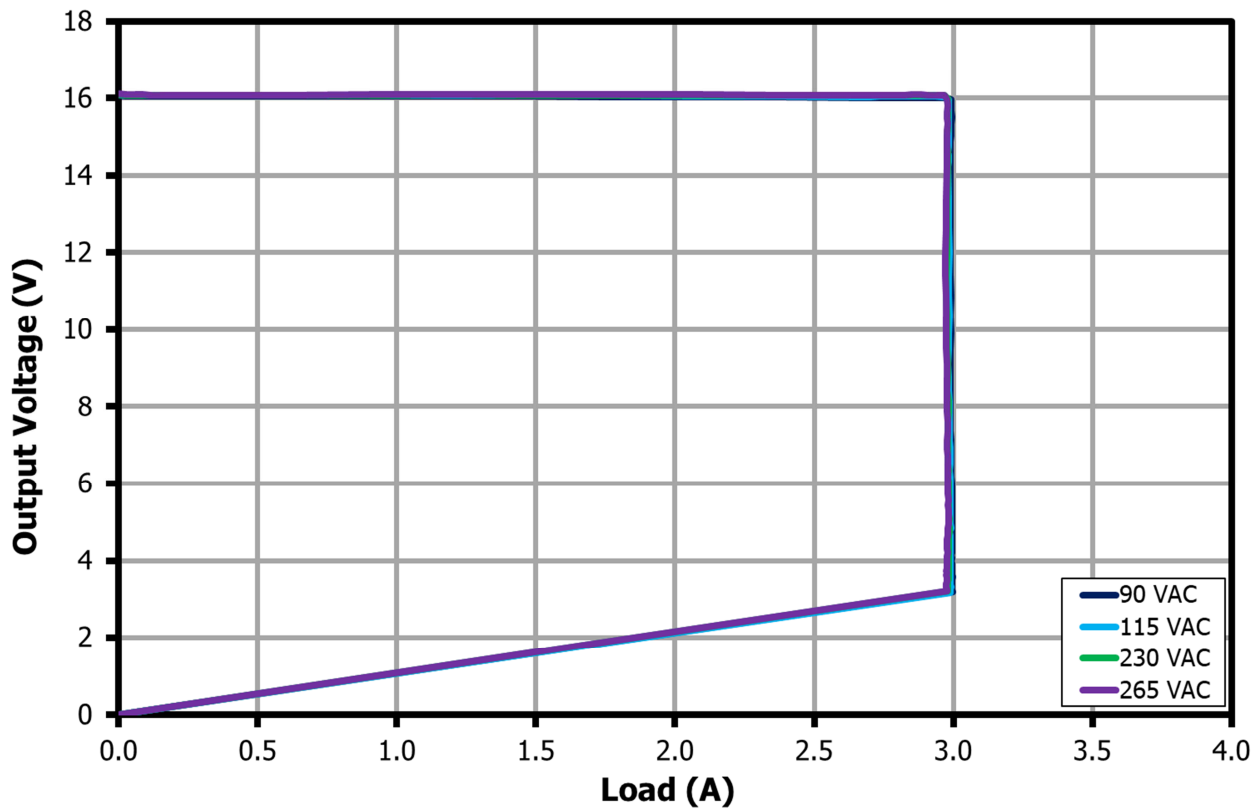


Figure 129 – CV/CC Profile for 16 V / 3 A PPS Request.

14.4 **Output: 21 V / 2.25 A PPS Request, PDO7**

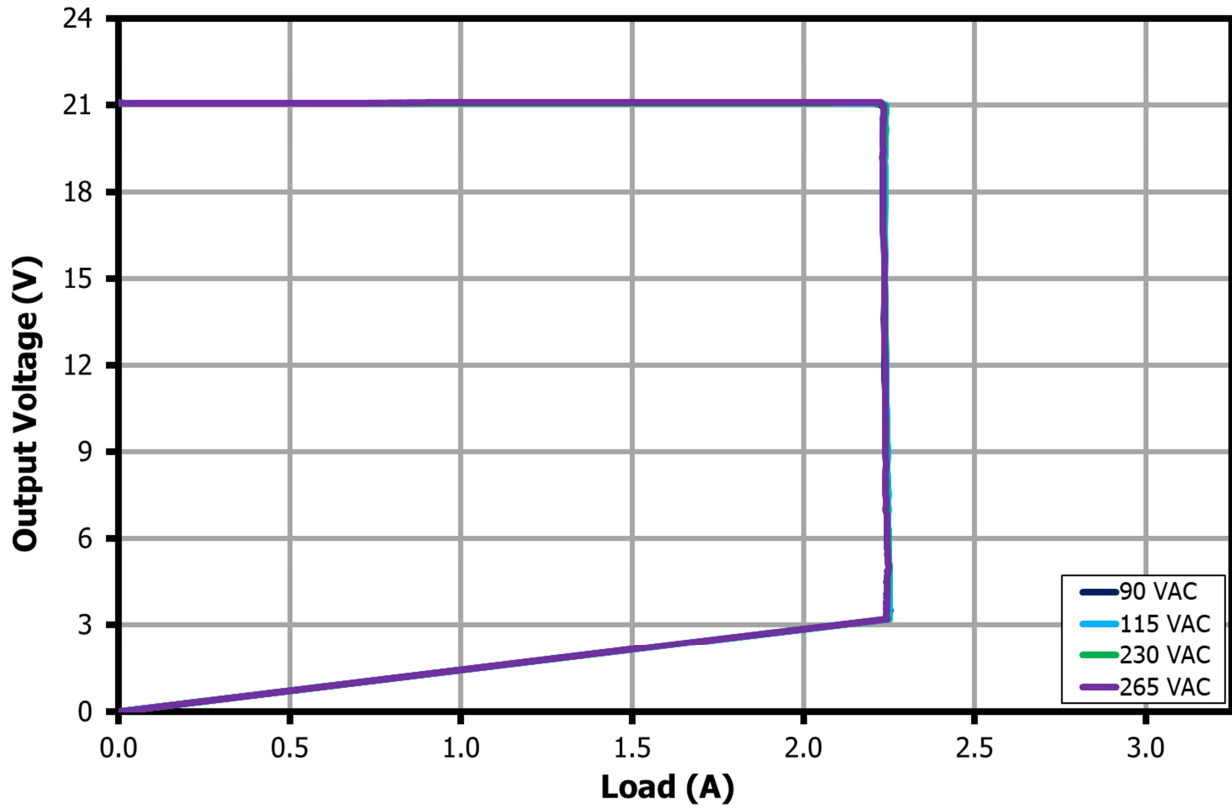


Figure 130 – CV/CC Profile for 21 V / 2.25 A PPS Request.



15 Voltage Step and Current Limit Test using QuadraMAX and Total Phase Analyzer

The power supply was evaluated and passed both QuadraMAX PPS Voltage Step Test (VST) and PPS Current Limit Test (CLT). The output voltage and current during VST and CLT as recorded by the Total Phase Analyzer are presented below.

15.1 Voltage Step Test (VST)

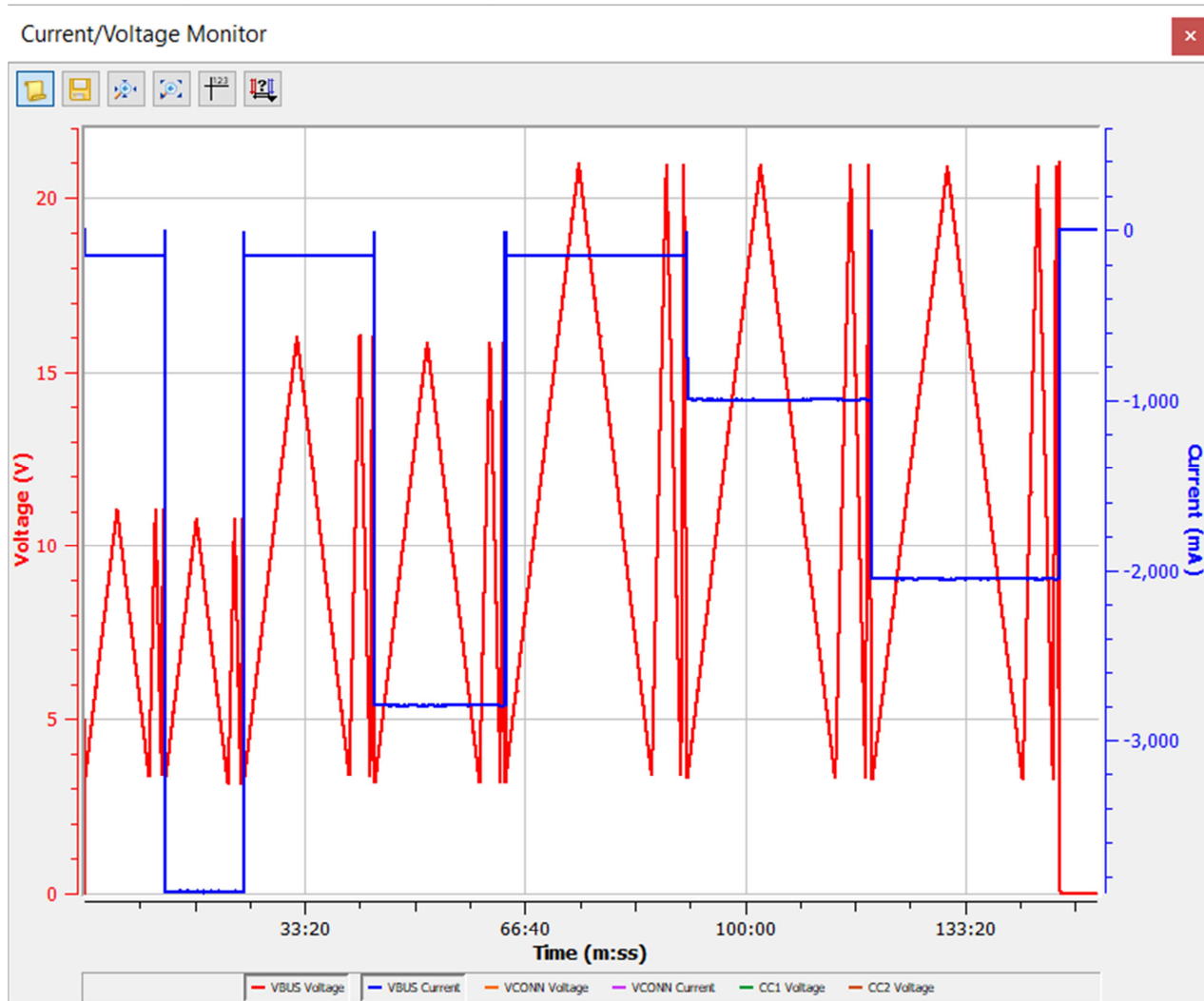


Figure 131 – Plot of SPT.6 VST from Total Phase Analyzer.

15.2 Current Limit Test (CLT)

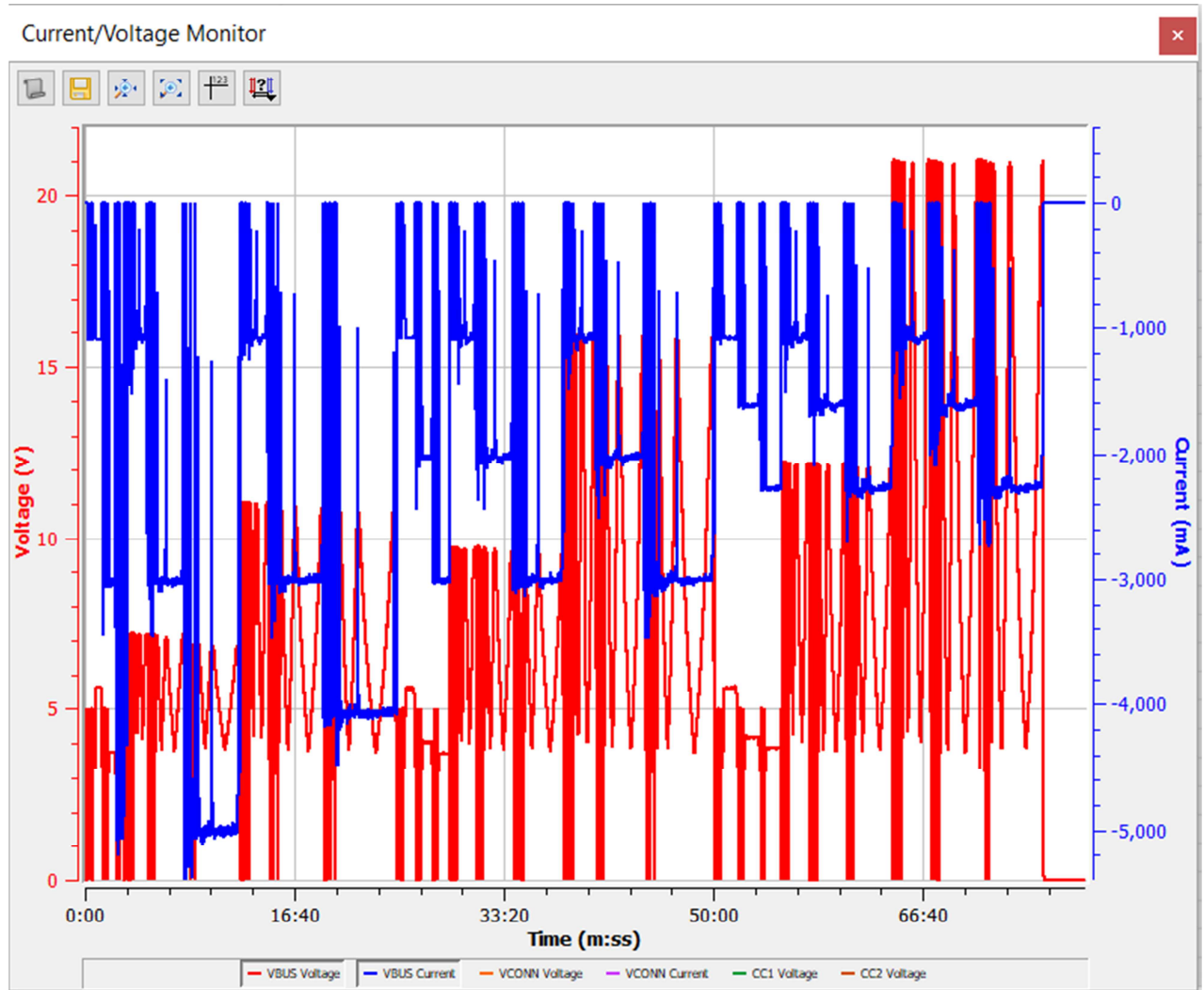


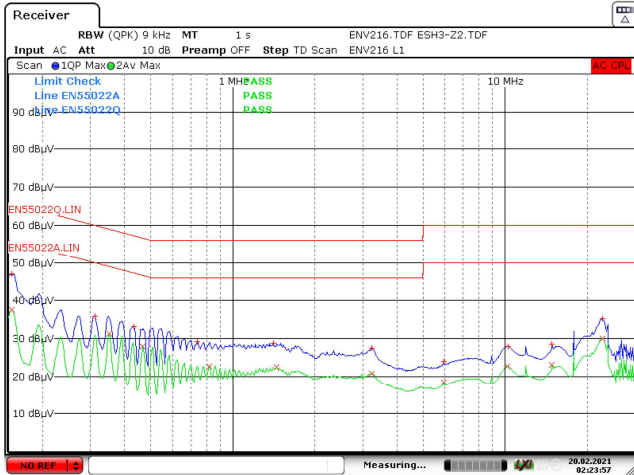
Figure 132 – Plot of SPT.7 CLT from Total Phase Analyzer.



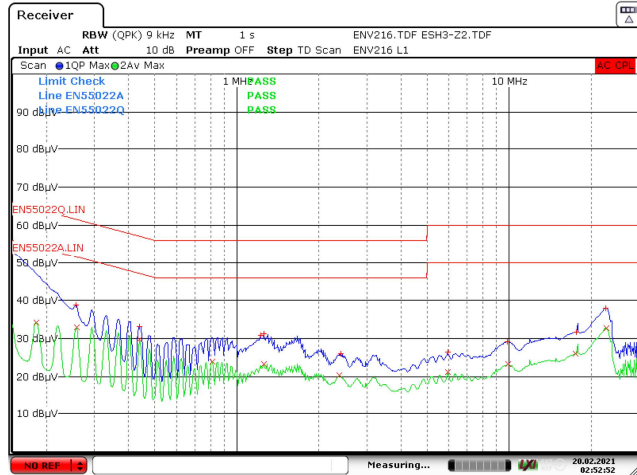
16 Conducted EMI

16.1 Floating Ground (QPK / AV)

16.1.1 Output: 5 V / 5 A

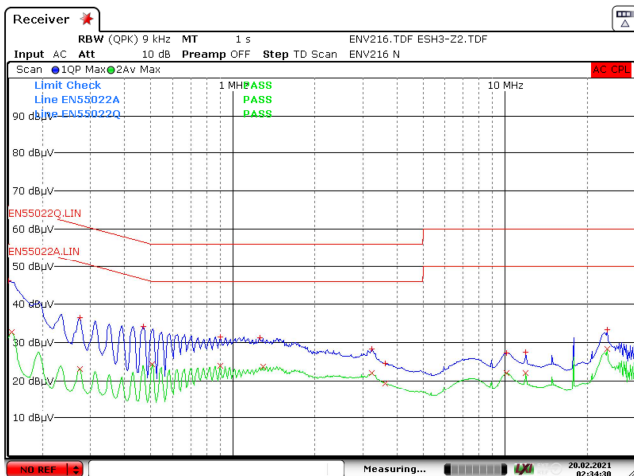


115 VAC.

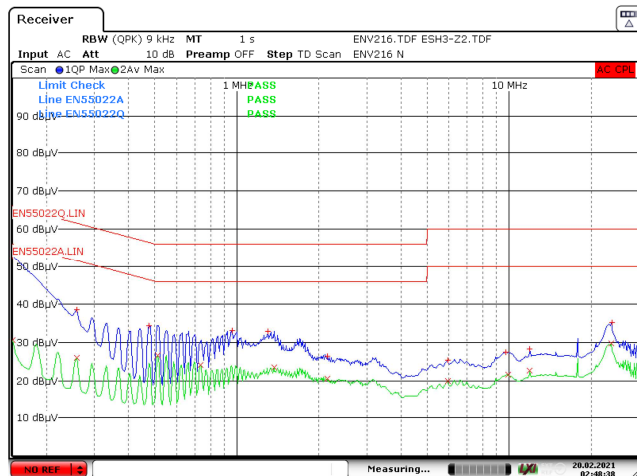


230 VAC.

Figure 133 – Floating Ground EMI, 5 V / 5 A Load [Line Scan].



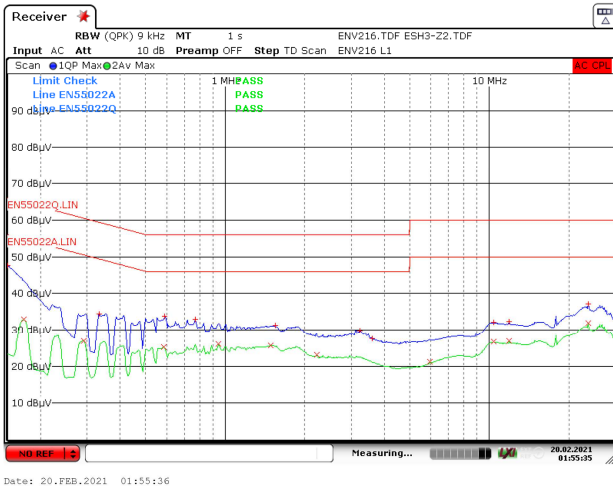
115 VAC.



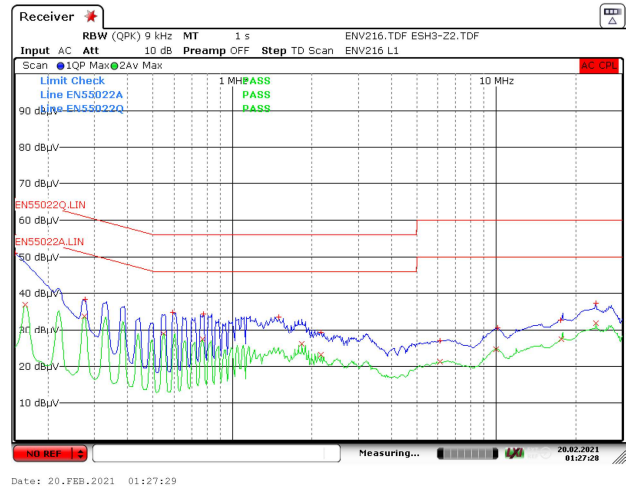
230 VAC.

Figure 134 – Floating Ground EMI, 5 V / 5 A Load [Neutral Scan].

16.1.2 Output: 9 V / 5 A

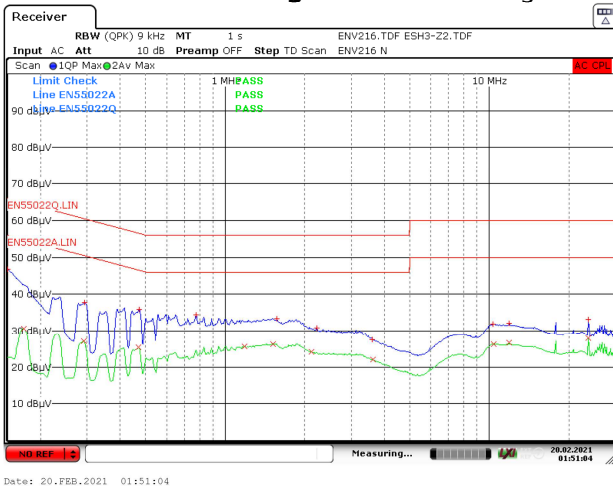


115 VAC.

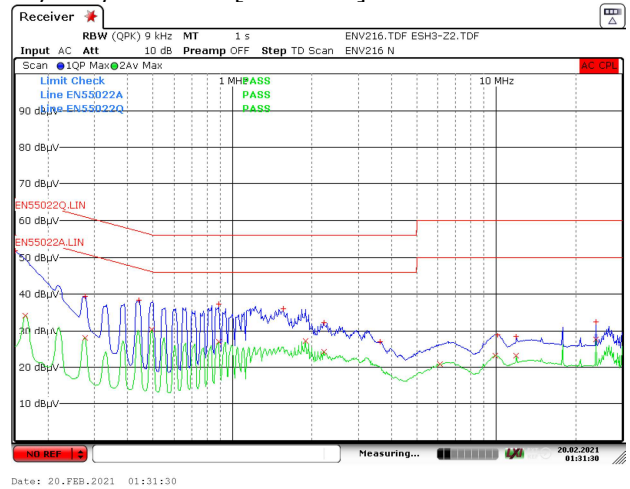


230 VAC.

Figure 135 – Floating Ground EMI, 9 V / 5 A Load [Line Scan].



115 VAC.

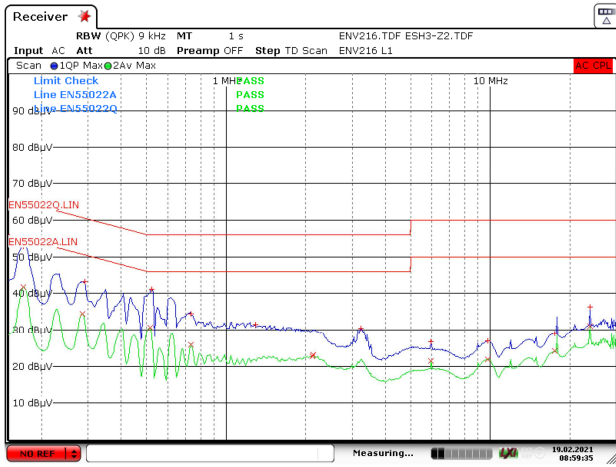


230 VAC.

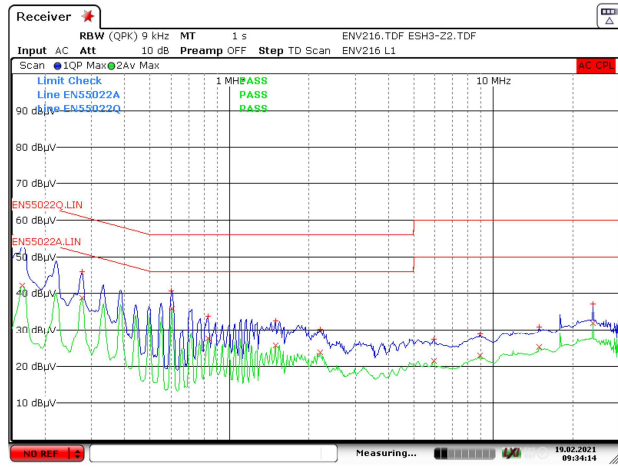
Figure 136 – Floating Ground EMI, 9 V / 5 A Load [Neutral Scan].



16.1.3 Output: 15 V / 3 A

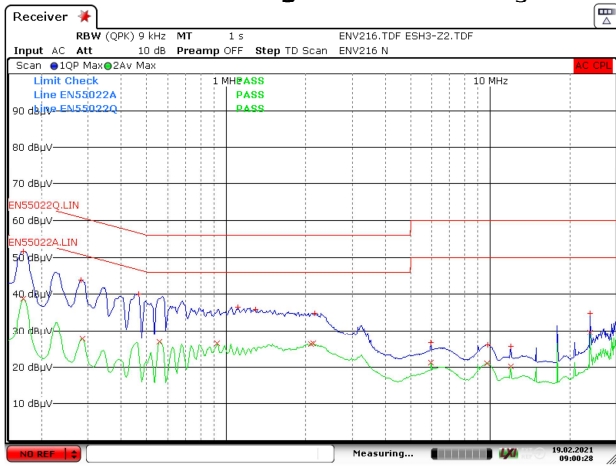


115 VAC.

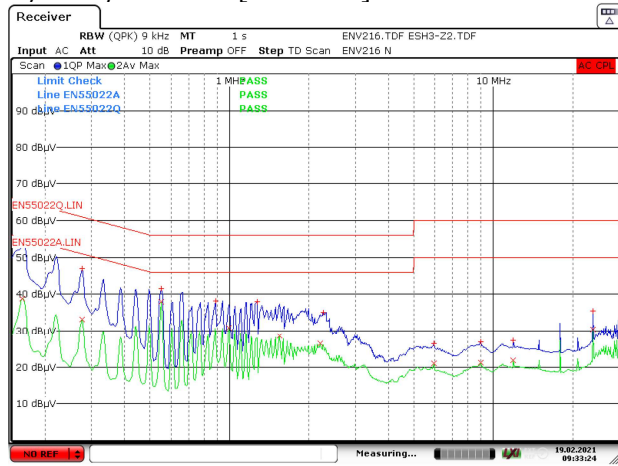


230 VAC.

Figure 137 – Floating Ground EMI, 15 V / 3 A Load [Line Scan].



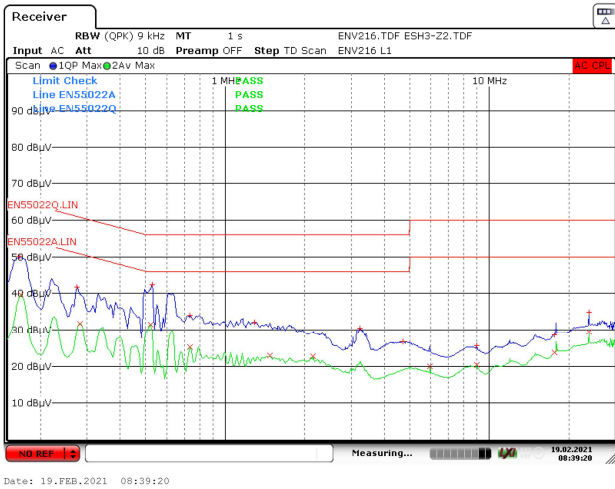
115 VAC.



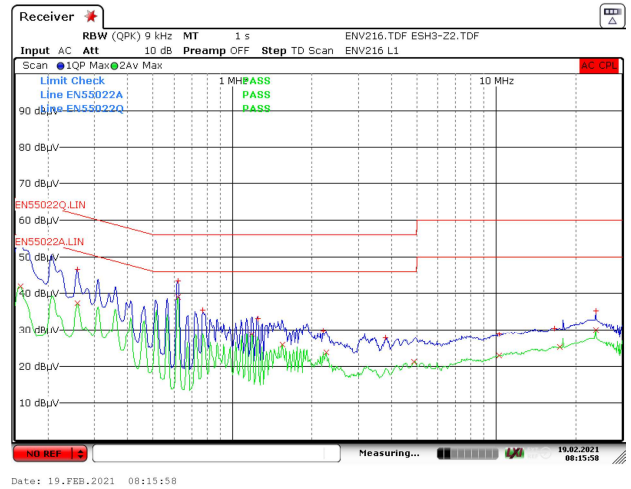
230 VAC.

Figure 138 – Floating Ground EMI, 15 V / 3 A Load [Neutral Scan].

16.1.4 Output: 20 V / 2.25 A

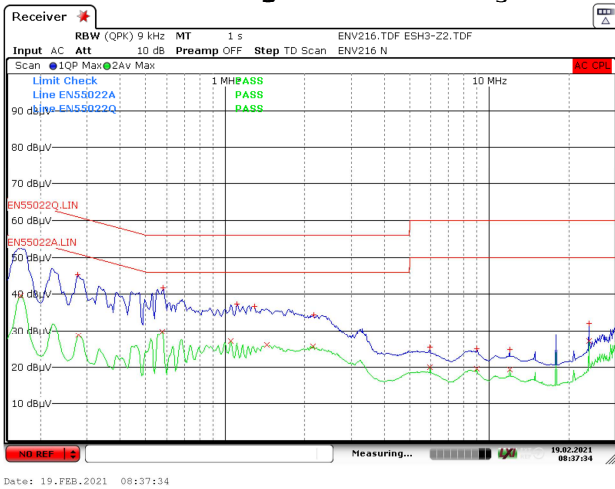


115 VAC.

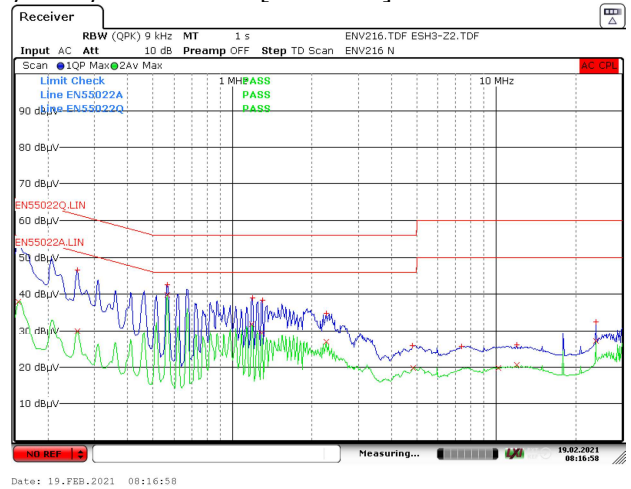


230 VAC.

Figure 139 – Floating Ground EMI, 20 V / 2.25 A Load [Line Scan].



115 VAC.



230 VAC.

Figure 140 – Floating Ground EMI, 20 V / 2.25 A Load [Neutral Scan].



17 Combination Wave Surge

The unit was subjected to ± 1500 V differential mode and ± 2000 V common mode combination wave surge at several line phase angles with 10 strikes for each condition.

A test failure was defined as an output latch-off that needs operator intervention to recover, or a complete loss of function that is not recoverable.

17.1 Differential Mode Surge (L1 to L2), 230 VAC Input

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result 5 V / 0 A without PD Sink	Test Result 20 V / 2.25 A
+1500	L1 to L2	0	Pass ¹	Pass
-1500	L1 to L2	0	Pass ¹	Pass
+1500	L1 to L2	90	Pass ¹	Pass
-1500	L1 to L2	90	Pass ¹	Pass
+1500	L1 to L2	270	Pass ¹	Pass
-1500	L1 to L2	270	Pass ¹	Pass

¹Power supply might initiate Auto-Restart protection due to Line OV condition

17.2 Common Mode Surge (L1, L2 to PE), 230 VAC Input

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result 5 V / 0 A without PD Sink	Test Result 20 V / 2.25 A
+2000	L1, L2 to PE	0	Pass	Pass
-2000	L1, L2 to PE	0	Pass	Pass
+2000	L1, L2 to PE	90	Pass	Pass
-2000	L1, L2 to PE	90	Pass	Pass
+2000	L1, L2 to PE	270	Pass	Pass
-2000	L1, L2 to PE	270	Pass	Pass

17.3 Common Mode Surge (L1 to PE), 230 VAC Input

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result 5 V / 0 A without PD Sink	Test Result 20 V / 2.25 A
+2000	L1 to PE	0	Pass	Pass
-2000	L1 to PE	0	Pass	Pass
+2000	L1 to PE	90	Pass	Pass
-2000	L1 to PE	90	Pass	Pass
+2000	L1 to PE	270	Pass	Pass
-2000	L1 to PE	270	Pass	Pass

17.4 **Common Mode Surge (L2 to PE), 230 VAC Input**

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result 5 V / 0 A without PD Sink	Test Result 20 V / 2.25 A
+2000	L2 to PE	0	Pass	Pass
-2000	L2 to PE	0	Pass	Pass
+2000	L2 to PE	90	Pass	Pass
-2000	L2 to PE	90	Pass	Pass
+2000	L2 to PE	270	Pass	Pass
-2000	L2 to PE	270	Pass	Pass

Note: Surge events might trigger input line OVP Protection and initiate an auto-restart. Auto-restart (AR) is one of the safety features of InnoSwitch3-PD to protect the converter from fault conditions. For applications that require completely no output interruption, the design can be modified to have a higher input line OVP voltage threshold or with the input line OVP completely disabled.

18 Electrostatic Discharge

The unit was tested with ± 8.0 kV to ± 16.5 kV air discharge and ± 8.0 to ± 8.8 kV contact discharge with 10 strikes for each condition at the following locations:

- End of cable +VOUT and GND
- On-board +VOUT and GND
- End of cable USB PD Sink CC Lines
- On-board CC1 and CC2

A test failure was defined as an output latch-off that needs operator intervention to recover, or a complete loss of function that is not recoverable.

- Note:**
1. Fish paper insulator (10 mil thick, 2-layer fold) is inserted into the PCB slot
 2. End of cable discharge points (VOUT, GND, CC1, CC2) located on the USB-C power adapter tester Tiny-PAT
 3. Type-C cable for all test conditions: Passive 3 A cable, 1 meter (Google)

18.1 VOUT and GND ESD Performance

Discharge points were added on the board and at the end of cable on the USB PD Sink (TinyPAT) to test VOUT and GND ESD performance.

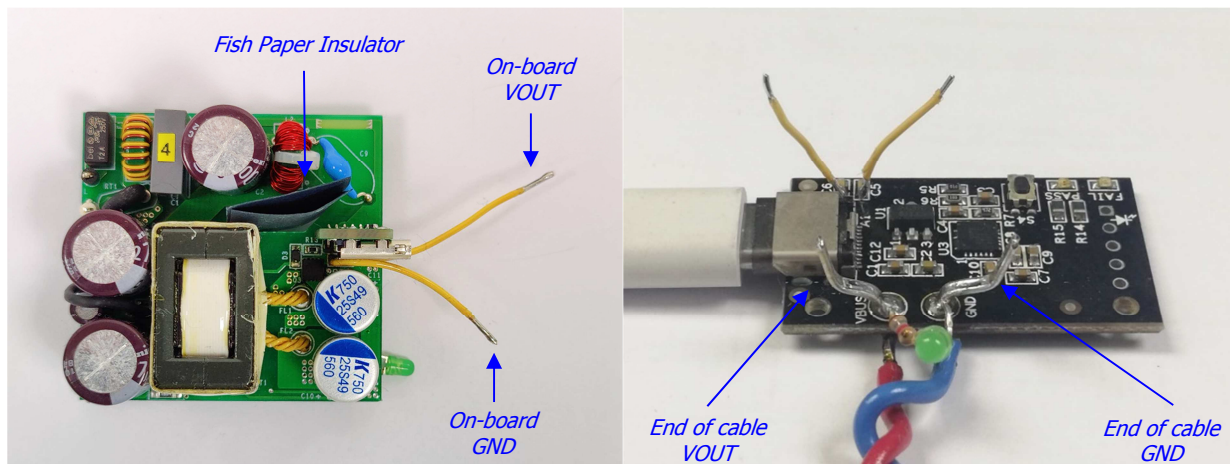


Figure 141 – Fish Paper Insulator and ESD Discharge Points, VOUT and GND.

18.1.1 Air Discharge, End of cable, 230 VAC Input

Discharge Voltage (kV)	ESD Strike Location (10 strikes each)	Test Result 20 V / 2.25 A	Test Result 5 V / 0 A with PD Sink
+8	+VOUT	Pass	Pass
	GND	Pass	Pass
-8	+VOUT	Pass	Pass
	GND	Pass	Pass
+10	+VOUT	Pass	Pass
	GND	Pass	Pass
-10	+VOUT	Pass	Pass
	GND	Pass	Pass
+12	+VOUT	Pass	Pass
	GND	Pass	Pass
-12	+VOUT	Pass	Pass
	GND	Pass	Pass
+14	+VOUT	Pass	Pass
	GND	Pass	Pass
-14	+VOUT	Pass	Pass
	GND	Pass	Pass
+15	+VOUT	Pass	Pass
	GND	Pass	Pass
-15	+VOUT	Pass	Pass
	GND	Pass	Pass
+16.5	+VOUT	Pass	Pass
	GND	Pass	Pass
-16.5	+VOUT	Pass	Pass
	GND	Pass	Pass

18.1.2 Air Discharge, On-board, 230 VAC Input

Discharge Voltage (kV)	ESD Strike Location (10 Strikes Each)	Test Result 20 V / 2.25 A	Test Result 5 V / 0 A with PD Sink	Test Result 5 V / 0 A without PD Sink
+8	+VOUT	Pass	Pass	Pass
	GND	Pass	Pass	Pass
-8	+VOUT	Pass	Pass	Pass
	GND	Pass	Pass	Pass
+10	+VOUT	Pass	Pass	Pass
	GND	Pass	Pass	Pass
-10	+VOUT	Pass	Pass	Pass
	GND	Pass	Pass	Pass
+12	+VOUT	Pass	Pass	Pass
	GND	Pass	Pass	Pass
-12	+VOUT	Pass	Pass	Pass
	GND	Pass	Pass	Pass
+14	+VOUT	Pass	Pass	Pass
	GND	Pass	Pass	Pass
-14	+VOUT	Pass	Pass	Pass
	GND	Pass	Pass	Pass
+15	+VOUT	Pass	Pass	Pass
	GND	Pass	Pass	Pass
-15	+VOUT	Pass ¹	Pass ¹	Pass
	GND	Pass ¹	Pass ¹	Pass
+16.5	+VOUT	Pass	Pass	Pass
	GND	Pass	Pass	Pass
-16.5	+VOUT	Pass ¹	Pass ¹	Pass
	GND	Pass ¹	Pass ¹	Pass

¹Power supply might initiate Auto-Restart or Hard Reset due to either:

- InnoSwitch3-PD protection, or
- USB-C power adapter tester Tiny-PAT protection at the load

18.1.3 Contact Discharge, End of Cable, 230 VAC Input

Discharge Voltage (kV)	ESD Strike Location (10 Strikes Each)		Test Result 20 V / 2.25 A	Test Result 5 V / 0 A with PD Sink
+8.0	End of Cable	+VOUT	Pass	Pass
		GND	Pass	Pass
-8.0		+VOUT	Pass	Pass
		GND	Pass	Pass
+8.8		+VOUT	Pass	Pass
		GND	Pass	Pass
-8.8		+VOUT	Pass	Pass
		GND	Pass	Pass

18.1.4 Contact Discharge, On the Board, 230 VAC Input

Discharge Voltage (kV)	ESD Strike Location (10 Strikes Each)		Test Result 20 V / 2.25 A	Test Result 5 V / 0 A with PD Sink	Test Result 5 V / 0 A without PD Sink
+8.0	On the Board	+VOUT	Pass	Pass	Pass
		GND	Pass	Pass	Pass
-8.0		+VOUT	Pass	Pass	Pass
		GND	Pass	Pass	Pass
+8.8		+VOUT	Pass	Pass	Pass
		GND	Pass	Pass	Pass
-8.8		+VOUT	Pass	Pass	Pass
		GND	Pass	Pass	Pass

18.2 **CC1 and CC2 ESD Performance**

Discharge points were added to CC1 and CC2 on the board for the unit under test. The Type-C cable was connected such that CC2 is the active channel during normal operation.

- Source CC2: Active (~ 1.7 V)
- Source CC1: Low (~ 0.5 V)

Similarly, discharge points were added to the communication lines of the USB PD Sink (TinyPAT) to test CC lines ESD performance. The two CC lines at the end of cable were differentiated by their voltage levels during the normal operation.

- Sink CC Line: Active (~ 1.7 V)
- Sink CC Line: Low (~ 0 V)

For the test condition 5 V / 0 A without USB PD Sink connected, both CC1 and CC2 channels on the board are on standby and are pulled-up to 3.5 V nominal.

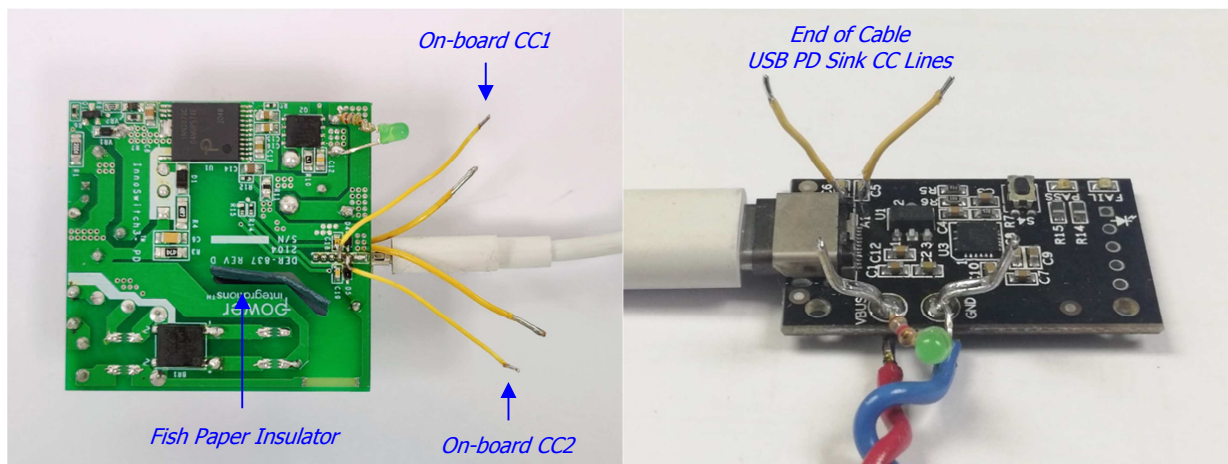


Figure 142 – Fish Paper Insulator and ESD Discharge Points, CC1 and CC2.

18.2.1 Air Discharge, End of cable, 230 VAC Input

Discharge Voltage (kV)	ESD Strike Location (10 Strikes Each)	Test Result 20 V / 2.25 A	Test Result 5 V / 0 A with PD Sink	
+15	End of Cable	CC Line: Active	Pass ¹	Pass ¹
		CC Line: Low	Pass ¹	Pass ¹
-15		CC Line: Active	Pass ¹	Pass ¹
		CC Line: Low	Pass ¹	Pass ¹
+16.5		CC Line: Active	Pass ¹	Pass ¹
		CC Line: Low	Pass ¹	Pass ¹
-16.5		CC Line: Active	Pass ¹	Pass ¹
		CC Line: Low	Pass ¹	Pass ¹

¹Power supply might initiate Auto-Restart or Hard Reset due to either:

- InnoSwitch3-PD protection, or
- USB-C power adapter tester Tiny-PAT protection at the load

18.2.2 Air Discharge, On-board, 230 VAC Input

Discharge Voltage (kV)	ESD Strike Location (10 Strikes Each)	Test Result 20 V / 2.25 A	Test Result 5 V / 0 A with PD Sink	Test Result 5 V / 0 A without PD Sink
+8	CC2: Active	Pass ¹	Pass ¹	Pass
	CC1: Low	Pass	Pass	Pass
-8	CC2: Active	Pass ¹	Pass ¹	Pass
	CC1: Low	Pass	Pass	Pass
+10	CC2: Active	Pass ¹	Pass ¹	Pass
	CC1: Low	Pass	Pass	Pass
-10	CC2: Active	Pass ¹	Pass ¹	Pass
	CC1: Low	Pass	Pass	Pass
+12	CC2: Active	Pass ¹	Pass ¹	Pass
	CC1: Low	Pass	Pass	Pass
-12	CC2: Active	Pass ¹	Pass ¹	Pass
	CC1: Low	Pass	Pass	Pass
+14	CC2: Active	Pass ¹	Pass ¹	Pass
	CC1: Low	Pass	Pass	Pass
-14	CC2: Active	Pass ¹	Pass ¹	Pass
	CC1: Low	Pass	Pass	Pass
+15	CC2: Active	Pass ¹	Pass ¹	Pass
	CC1: Low	Pass ¹	Pass ¹	Pass
-15	CC2: Active	Pass ¹	Pass ¹	Pass
	CC1: Low	Pass ¹	Pass ¹	Pass
+16.5	CC2: Active	Pass ¹	Pass ¹	Pass
	CC1: Low	Pass ¹	Pass ¹	Pass
-16.5	CC2: Active	Pass ¹	Pass ¹	Pass
	CC1: Low	Pass ¹	Pass ¹	Pass

¹Power supply might initiate Auto-Restart or Hard Reset due to either:

- InnoSwitch3-PD protection, or
- USB-C power adapter tester Tiny-PAT protection at the load

18.2.3 Contact Discharge, End of Cable, 230 VAC Input

Discharge Voltage (kV)	ESD Strike Location (10 Strikes Each)	Test Result 20 V / 2.25 A	Test Result 5 V / 0 A with PD Sink
+8.0	CC Line: Active	Pass ¹	Pass ¹
	CC Line: Low	Pass ¹	Pass ¹
-8.0	CC Line: Active	Pass ¹	Pass ¹
	CC Line: Low	Pass ¹	Pass ¹
+8.8	CC Line: Active	Pass ¹	Pass ¹
	CC Line: Low	Pass ¹	Pass ¹
-8.8	CC Line: Active	Pass ¹	Pass ¹
	CC Line: Low	Pass ¹	Pass ¹

¹Power supply might initiate Auto-Restart or Hard Reset due to either:

- InnoSwitch3-PD protection, or
- USB-C power adapter tester Tiny-PAT protection at the load

18.2.4 Contact Discharge, On the Board, 230 VAC Input

Discharge Voltage (kV)	ESD Strike Location (10 Strikes Each)	Test Result 20 V / 2.25 A	Test Result 5 V / 0 A with PD Sink	Test Result 5 V / 0 A without PD Sink
+8.0	CC Line: Active	Pass ¹	Pass ¹	Pass
	CC Line: Low	Pass	Pass	Pass
-8.0	CC Line: Active	Pass ¹	Pass ¹	Pass
	CC Line: Low	Pass	Pass	Pass
+8.8	CC Line: Active	Pass ¹	Pass ¹	Pass
	CC Line: Low	Pass	Pass	Pass
-8.8	CC Line: Active	Pass ¹	Pass ¹	Pass
	CC Line: Low	Pass	Pass	Pass

¹Power supply might initiate Auto-Restart or Hard Reset due to either:

- InnoSwitch3-PD protection, or
- USB-C power adapter tester Tiny-PAT protection at the load

19 Revision History

Date	Author	Revision	Description & Changes	Reviewed
09-Jun-21	DB	1.0	Initial Release.	Apps & Mktg



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